Journal of Power Electronics (2021) 21:1585–1599
https://doi.org/10.1007/s43236-021-00295-9

ORIGINAL ARTICLE

Phase-shifted full-bridge converter with coupled-inductor-based rectifier

Byoung-Gi Choi[1] · Woo-Seok Lee[1] · Jeong-Uk Park[1] · Il-Oun Lee[1]

Received: 15 June 2021 / Revised: 23 July 2021 / Accepted: 26 July 2021 / Published online: 4 August 2021

Abstract
In this paper, a phase-shifted full-bridge (PSFB) converter with a coupled-inductor-based rectifier is presented. The proposed PSFB converter alleviates the circulating-current problem of conventional PSFB converters. As a result, it can operate with a larger effective duty-cycle over a wide range of input voltage or output load conditions. The transformer turn-ratio can be better designed in terms of the primary-side conduction loss and the secondary-rectifier voltage stress. Due to the reduced secondary voltage stress, diodes with a lower forward-voltage drop can be used in the rectifier of the proposed converter, which results in s reduction of the secondary-side conduction and snubber losses. With these advantages, the proposed converter can achieve a higher power-conversion efficiency when compared to conventional converters. To verify the effectiveness of the proposed converter, this paper presents the operating principle, dc analysis, and experimental results of a prototype converter built with the specification of a 1.0 kW, 300–400 V input, a 50 V output, and a 100 kHz switching frequency.

Keywords Circulating current · Duty-cycle loss · Phase-shift full-bridge converter

1 Introduction

Recently, power electronics technology has been focusing on improving power density and power-conversion efficiency. For this, the use of advanced power semiconductor switches like GaNs or SiC MOSFETs has been considered [1–4]. In addition, new circuits that can improve the performance of existing converters have been developed to enhance power-conversion efficiency while improving or maintaining power density [5–7].

The phase-shifted full-bridge (PSFB) converter with a center-tapped transformer shown in Fig. 1 has many advantages such as zero-voltage switching (ZVS) operation without the help of any auxiliary circuits, clamped voltage stress, small RMS current stress of the primary switches, and low secondary-side conduction loss [8–10]. Due to these advantages, it has been one of the most promising topologies for low-voltage and high-current applications such as data-center power supplies, power supplies for communication equipment, and battery chargers for neighborhood electric vehicles [11–13]. Although the PSFB converter in Fig. 1 has been widely used in many applications, there exist many challenges when it comes to improving the performance of the converter. First, the ZVS operation of the lagging-leg switches in the PSFB converter fails under light load conditions. Figure 2 shows key waveforms of the PSFB converter in Fig. 1, where the lagging-leg switches are defined as Q_3 and Q_4 in the converter. The secondary rectifier stage is separated from the transformer primary side before Q_3 or Q_4 turn-off due to the zero-voltage interval of the voltage V_{ab}, as shown in this figure. Therefore, the resonance between the series inductor L_{lk} and the parasitic capacitors C_{oss3} and C_{oss4} occurs at the moment Q_3 or Q_4 turns off, and the zero-voltage switching of Q_3 or Q_4 can be achieved by this resonance. However, since the value of L_{lk} is generally very small which makes the characteristic impedance of the resonant circuit become small, ZVS is not achieved as soon as the load drops even under slightly less than full load conditions. Due to this, its conversion efficiency is severely degraded when the load decreases [14–16]. Secondly, if the converter is suitable for wide operating ranges due to design considerations such as hold-up time requirements or wide output-voltage ranges like battery chargers, the operating duty-cycle becomes small under normal operating conditions and the freewheeling interval lengthens.

✉ Il-Oun Lee
leeiloun@mju.ac.kr

[1] Department of Electrical Engineering, Myongji University, Yongin, Korea

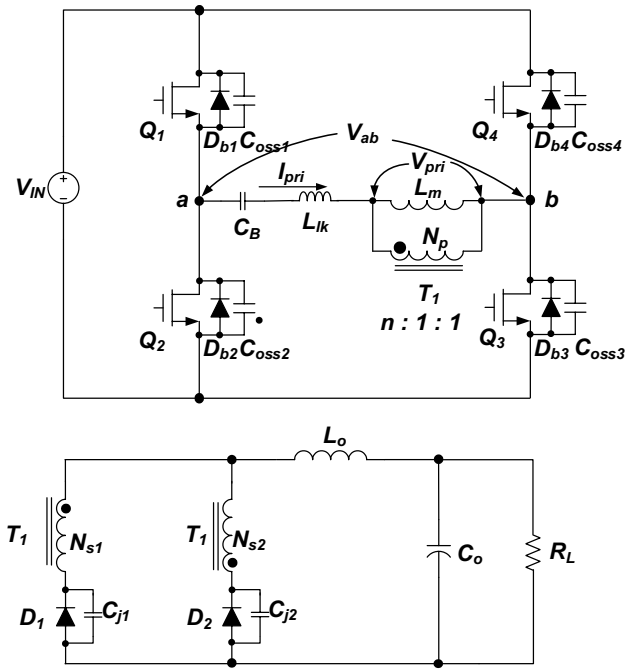


Fig. 1 Phase-shifted full-bridge (PSFB) converter with a center-tapped transformer

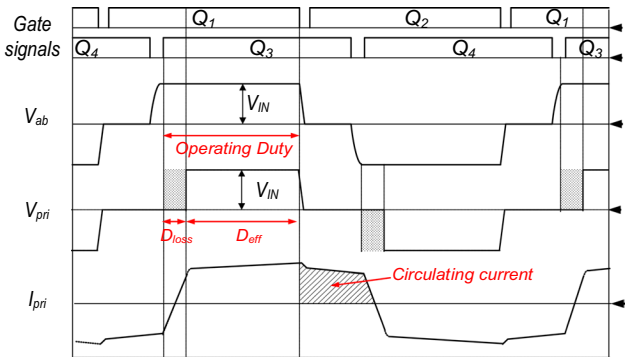


Fig. 2 Key waveforms of the PSFB converter in Fig. 1

As a result, the excessive circulating current appears on the primary side as shown in Fig. 2, which results in increasing the primary-side conduction loss and turn-off switching loss of the lagging-leg switches [17–19]. In addition, although the on-state of the switches Q_1 and Q_3 or Q_2 and Q_4 form a wide operating-duty in the V_{ab} voltage waveform, the circulating current increases the duty loss D_{loss} and decreases the effective duty-cycle D_{eff}, which contributes to the power transmission. As a result, the area of the transformer primary voltage V_{pri}, which is really transmitted to the transformer secondary coils, decreases. Thus, the desired output voltage is not obtained. To overcome this problem, the transformer turn-ratio n should be lower than the case of no circulating current, at which point both the primary-side current and secondary-side voltage stresses significantly increase [20].

Many PSFB converters have been presented to overcome the abovementioned disadvantages. To reduce the circulating current, the PSFB converters in [16, 20–25] require auxiliary circuits consisting of capacitors, diodes, and active switches in the secondary rectification circuit. The PSFB converters in [26, 27] deviate from the problem of circulating current by decreasing the value of a DC (direct current) blocking capacitor in series with a transformer. However, in this case, the voltage drop across the DC blocking capacitor is increased due to its small capacitance. Therefore, the transformer's primary voltage becomes lower. This makes it difficult to regulate the desired output voltage or current without an unfavorable design of the transformer turn-ratio in terms of primary-side current and secondary-side voltage stresses. The PSFB converters in [28–32] are integrated with other DC/DC converters such as half-bridge pulse-width-modulation (PWM) converters or LLC resonant converters to guarantee a wide ZVS range in the presence of load variations without the loss of an effective duty-cycle. As a result, the circulating current is alleviated and the secondary-side voltage stress is significantly reduced. However, they require two or more transformers to highlight their advantages. Although the performance can be improved by replacing the output inductor with a single coupled inductor, this solution is limited to PSFB converters with a full-bridge rectifier that uses four diodes [33].

This paper focuses on the development of new circuits for improving power-conversion efficiency while overcoming the abovementioned challenges of the PSFB converter in Fig. 1. Figure 3 shows the PSFB converter proposed in this paper for improving the performance of the converter in Fig. 1. As can be seen in Fig. 3, the primary-side structure of the proposed converter is the same as that of the conventional PSFB converter. Meanwhile, the rectification circuit is structured by rearranging the secondary circuit shown in Fig. 1, and adding an additional diode D_a after replacing the output inductor with a coupled inductor. This structure reduces the circulating current in Fig. 1 and enables the proposed PSFB converter to operate with larger effective duty-cycles over a wide operating range. Due to this, the transformer turn-ratio can be designed better in terms of primary-side conduction loss and secondary-rectifier voltage stress. Due to the reduction in the secondary-side voltage stress, diodes with a lower forward-voltage drop can be used in the proposed converter, which results in an additional reduction of the power loss on the secondary side. With these advantages, the proposed converter can achieve a higher power-conversion efficiency when compared to the conventional converter in Fig. 1.

The remainder of this paper is organized as follows. In Sect. 2, both a description and the operation principle of the

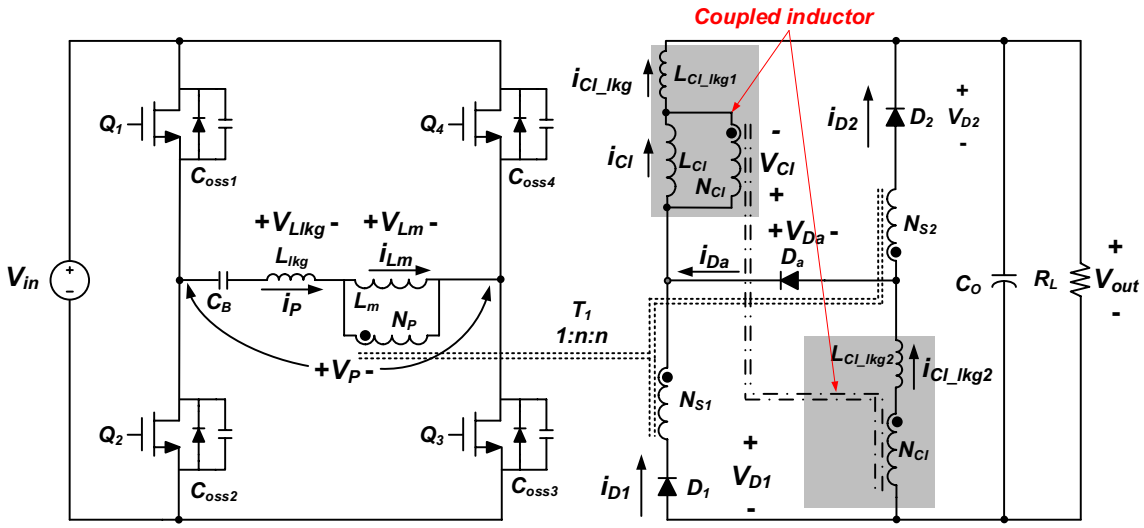


Fig. 3 Proposed converter

proposed converter are presented. Relevant analysis results are given in Sect. 3. In Sect. 4, experimental results and a comparison of the conventional and the proposed converters are presented. Finally, some conclusions are made in Sect. 5.

2 Operation principle

Figure 4 shows key operating waveforms of the proposed converter in the steady-state. The proposed converter has 18 operation modes in one switching cycle. However, only the operation during the first half-switching cycle is analyzed as in Fig. 5 due to symmetry. For analyzing the steady-state operation, the following assumptions are made.

The input and output voltages are constant with respect to V_{in} and V_{out}.
The parasitic capacitors of the switches have the same capacitance as C_{oss}.
The coupled inductor has a turn-ratio of 1:1. In addition, it has turns of N_{CI}, a magnetizing inductance of L_{CI}, and a high coupling-coefficient.
The influence of parasitic capacitors of rectifier diodes is ignored.

Mode 1 [t_0, t_1]: In mode 1, the switches Q_1 and Q_3 are in the on-state. Hence, the primary-winding voltage of the transformer V_P is the input voltage V_{in}, which is transmitted to the secondary windings by the transformer turn-ratio. In addition, the diode D_1 is forward-biased and the diodes D_2 and D_a are reverse-biased. Then, the voltage across the coupled inductor V_{CI} becomes $V_{\text{in}}/n - V_{\text{out}}$, which linearly increases the current flowing via the magnetizing inductance of the coupled inductor. The primary-side current i_P is the sum of the transformer magnetizing currents i_{Lm} and i_{CI} flowing through the coupled inductor. The current and voltage equations in this mode are as follows.

$$V_{\text{CI}} = V_{\text{in}}/n - V_{\text{out}} \tag{1}$$

$$i_{\text{CI}}(t) = i_{\text{CI\_lkg1}}(t) = i_{D1}(t) = i_{\text{CI}}(t_0) + \frac{V_{\text{CI}}}{L_{\text{CI}}}(t - t_0) \tag{2}$$

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_{in}}{L_m}(t - t_0) \tag{3}$$

$$i_P(t) = i_{Lm}(t) + i_{CI}(t)/n \tag{4}$$

Mode 2 [t_1, t_2]: Mode 2 starts when the switch Q_3 is switched off. Then, the parasitic capacitors C_{OSS3} and C_{OSS4} of the leading-leg switches Q_3 and Q_4 are charged or discharged. The voltages across Q_3, Q_4 and V_P can be expressed as follows.

$$V_{Q_3}(t) = \frac{i_P(t_1)}{2C_{\text{OSS}}}(t - t_1) = V_{\text{in}} - V_{Q_4}(t) = V_{\text{in}} - V_P(t) \tag{5}$$

During this mode, the primary-side voltage V_P linearly decreases from the input voltage as in Eq. (5). Under this influence, the coupled inductor voltage V_{CI} linearly decreases toward $-V_{\text{out}}/2$ and the voltage across D_a, V_{Da} also decreases toward 0 V. Then, V_{Da} becomes 0 V at the end of this mode and diode D_a turns on.

Mode 3 [t_2, t_3]: Mode 3 starts with the turn-on of the auxiliary diode D_a in the rectifier circuit. At this time, the

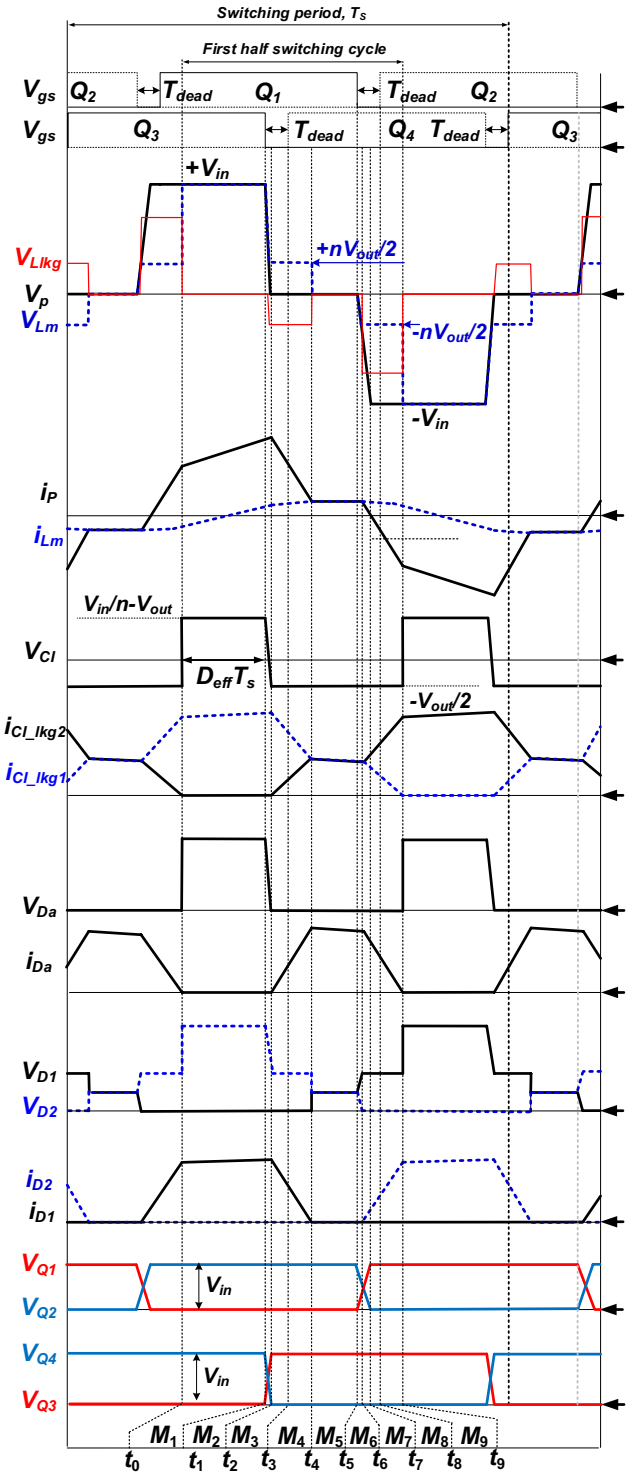


Fig. 4 Key operating waveforms of the proposed converter in the steady-state

voltage V_P is 0 V and the body diode of Q_4 is conducted. Figure 6c shows an equivalent circuit for the analysis of this mode. Assuming that the two leakage inductances in the coupled inductor have the same value, the voltages in the equivalent circuit can be determined as follows:

$$L_{\mathrm{CI\_}lkg1} = L_{\mathrm{CI\_}lkg2} = L_{\mathrm{CI\_}lkg} \tag{6}$$

$$V_{\mathrm{CI\_}lkg1} = -V_{\mathrm{CI\_}lkg2} = -\frac{L_{\mathrm{CI\_}lkg}}{2L_{\mathrm{CI\_}lkg} + \frac{4L_{lkg}}{n^2}} V_{\mathrm{out}} \tag{7}$$

$$V_{Llkg} = -V_{L_m} = -\frac{nV_{\mathrm{out}}L_{lkg}}{n^2 L_{\mathrm{CI\_}lkg} + 2L_{lkg}} \approx -\frac{nV_{\mathrm{out}}}{2} \tag{8}$$

From Eq. (8), it is noted that since the leakage inductance of the coupled inductor is very small due to its high coupling coefficient design, the transformer leakage inductance voltage V_{Llkg} is nearly 50% of the negative output voltage with a turn-ratio. Then, the transformer primary current i_P can be determined as follows:

$$i_P(t) = i_P(t_2) - \frac{nV_{\mathrm{out}}}{2L_{lkg}}(t - t_2) \tag{9}$$

Equation (9) gives the currents of the coupled inductor as follows:

$$i_{\mathrm{CI\_}lkg1}(t) = i_{D1}(t) = i_{\mathrm{CI\_}lkg1}(t_2) - \frac{V_{\mathrm{out}}}{2L_{lkg}}(t - t_2) \tag{10}$$

$$i_{\mathrm{CI\_}lkg2}(t) = \frac{V_{\mathrm{out}}}{2L_{lkg}}(t - t_2) = i_{Da}(t) \tag{11}$$

Mode 4 [t_3, t_4]: Mode 4 starts when Q_4 turns on under zero-voltage switching (ZVS). During this mode, the voltages applied to the leakage inductance of the transformer are the same as the analysis results from Mode 3. Therefore, the currents flowing through the coupled inductor continue to linearly decrease or increase as in Eqs. (10) and (11). The current of the rectifier diode D_1 also decreases linearly.

During the interval from time t_2 to t_4, the primary-side current i_P is not transmitted to the transformer secondary-side since V_P is 0 V. It only circulates through Q_1, Q_4, and the transformer. However, due to the negative output voltage applied to the transformer leakage inductance as in Eq. (9), i_P continues to decrease until it reaches the transformer magnetizing current i_{Lm} as shown in Fig. 4. This mechanism verifies that the proposed converter has smaller circulating currents when compared to the conventional PSFB converter. This fact will be explained in detail in the next section.

Mode 5 [t_4, t_5]: Mode 5 starts when i_P reaches i_{Lm}. At this moment, the diode D_1 is turned off with zero current and the currents via the coupled inductor become the same. In this mode, the voltage V_{Lm} becomes 0 V and i_{Lm} only flows in

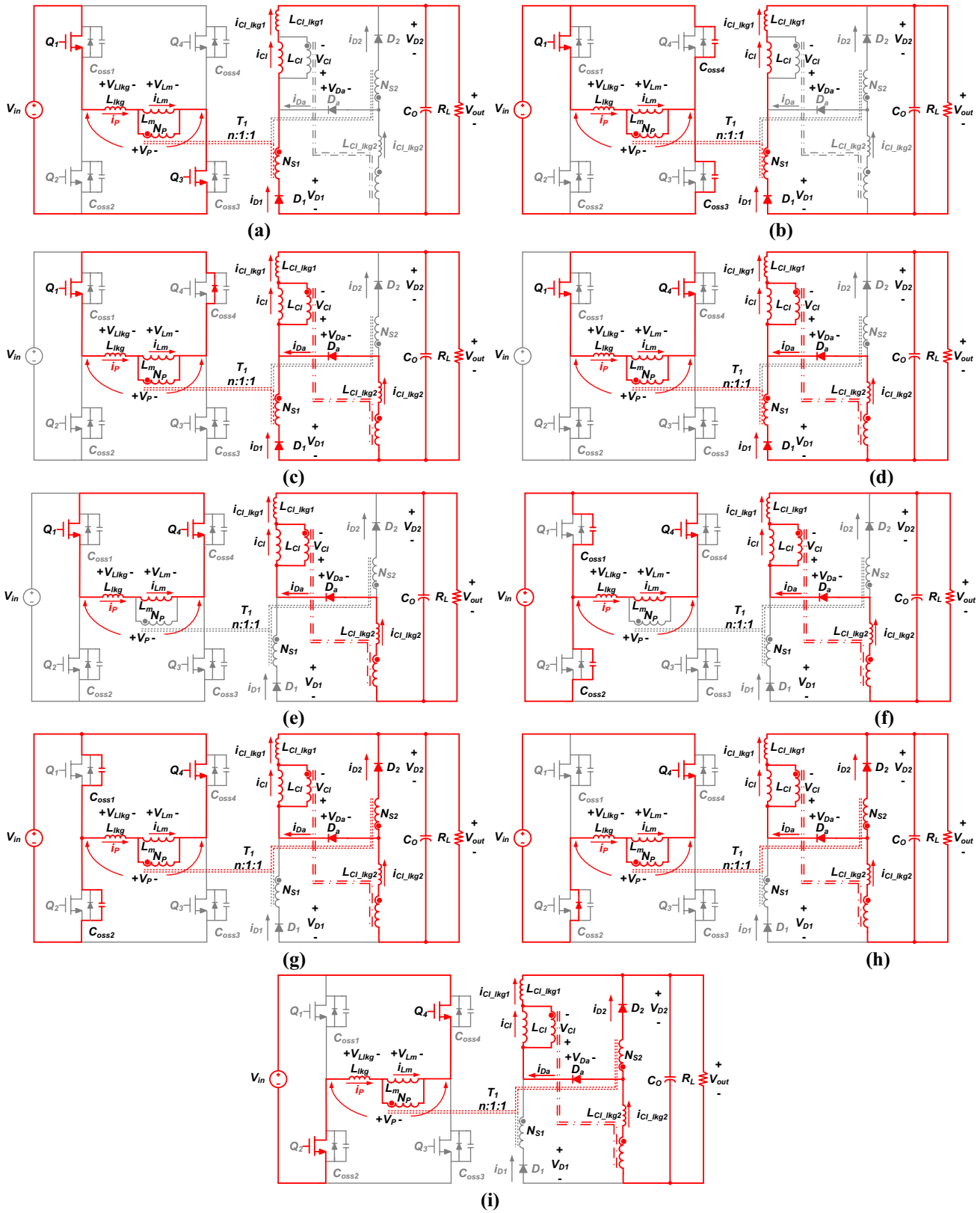


Fig. 5 Operating circuits: **a** Mode 1; **b** Mode 2; **c** Mode 3; **d** Mode 4; **e** Mode 5; **f** Mode 6; **g** Mode 7; **h** Mode 8; **i** Mode 9

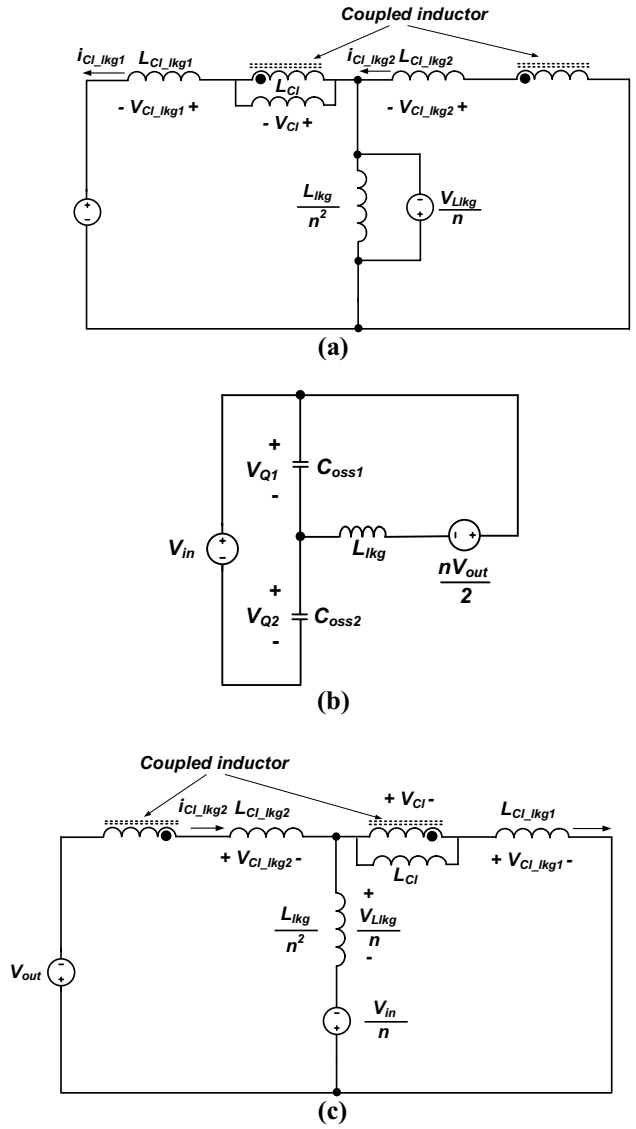


Fig. 6 Equivalent circuits of the proposed converter during: **a** Mode 3; **b** Mode 7; **c** Mode 8

the primary side. The currents of the coupled inductor can be expressed as follows:

$$i_{\mathrm{CI}\_lkg1}(t) = i_{\mathrm{CI}\_lkg2}(t) = i_{Da}(t) = i_{\mathrm{CI}\_lkg1}(t_4) - \frac{V_{\mathrm{out}}}{2L_{\mathrm{CI}}}(t - t_4) \tag{12}$$

Mode 6 [t_5, t_6]: Mode 6 starts when the switch Q_1 is turned off. Then, the parasitic capacitors of the lagging-leg switches Q_1 and Q_2, C_{OSS1} and C_{OSS2} are charged or discharged. The voltages across Q_1 and Q_2 can be expressed as follows:

$$V_{Q1}(t) = \frac{i_{Lm}(t_5)}{2C_{\mathrm{OSS}}}(t - t_5) = V_{\mathrm{in}} - V_{Q2}(t) = -V_P(t) \approx -V_{Lm}(t) \tag{13}$$

In this mode, the primary voltages V_P and V_{Lm} linearly decrease from 0 V to a negative input voltage as shown in Eq. (13). When V_{Lm} reaches $-nV_{\mathrm{out}}/2$, the rectifier diode D_2 voltage becomes 0 V and D_2 conducts.

Mode 7 [t_6, t_7]: Mode 7 starts when the diode D_2 conducts in mode 6. Figure 6g shows an equivalent circuit for the analysis of this mode. From this analysis, the voltages and current in this mode can be determined as follows:

$$V_{Q1}(t) = \frac{nV_{\mathrm{out}}}{2} + \sqrt{\frac{L_{lkg}}{2C_{\mathrm{OSS}}}}\, i_P(t_6) sin \frac{1}{\sqrt{2C_{\mathrm{OSS}}L_{lkg}}}(t - t_6) \tag{14}$$

$$V_{Q2}(t) = V_{\mathrm{in}} - V_{Q1}(t) = V_{\mathrm{in}} + V_P(t) \tag{15}$$

$$V_{L_m}(t) = -nV_{\mathrm{out}}/2 \tag{16}$$

$$i_P(t) = i_P(t_6)\cos\frac{1}{\sqrt{2C_{\mathrm{OSS}}L_{lkg}}}(t - t_6) \tag{17}$$

From Eqs. (14), (15), and (17), it is noted that the voltages of the lagging-leg switches increase or decrease in sinusoidal form due to the resonance between the transformer leakage inductance and the switch parasitic capacitances. This mode ends when the voltage of Q_2 reaches zero.

Mode 8 [t_7, t_8]: Mode 8 starts when the Q_2 voltage becomes 0 V. Figure 6h shows an equivalent circuit for an analysis of mode 8. Analyzing the equivalent circuit gives the voltages in this figure as follows:

$$V_{\mathrm{CI}\_lkg1} = -V_{\mathrm{CI}\_lkg2} = -\frac{L_{\mathrm{CI}\_lkg}}{2L_{\mathrm{CI}\_lkg} + \frac{4L_{lkg}}{n^2}}\left(\frac{2V_{\mathrm{in}}}{n} - V_{\mathrm{out}}\right) \tag{18}$$

$$V_{Llkg} = -\frac{L_{lkg}(2V_{\mathrm{in}} - nV_{\mathrm{out}})}{n^2L_{\mathrm{CI}\_lkg} + 2L_{lkg}} \approx -\left(V_{\mathrm{in}} - \frac{nV_{\mathrm{out}}}{2}\right) \tag{19}$$

In Eq. (19), if the coupling coefficient of the coupled inductor is high and its leakage inductance is exceedingly small, the transformer leakage inductance voltage V_{Llkg} is the sum of the negative input voltage and half of the output voltage with a turn-ratio and is negative. Then, the transformer primary current i_P in this mode can be determined as follows:

$$i_P(t) = i_P(t_7) - \frac{V_{\mathrm{in}} - 0.5nV_{\mathrm{out}}}{L_{lkg}}(t - t_7) \tag{20}$$

Equation (9) gives the currents of the coupled inductor as follows:

$$i_{\mathrm{CI}\_lkg1}(t) = i_{Da}(t) = i_{\mathrm{CI}\_lkg1}(t_7) - \frac{(V_{\mathrm{in}}/n - 0.5V_{\mathrm{out}})}{L_{lkg}}(t - t_2) \tag{21}$$

$$i_{CI\_lkg2}(t) = i_{CI\_lkg2}(t_7) + \frac{(V_{in}/n - 0.5V_{out})}{L_{lkg}}(t - t_7) \quad (22)$$

Mode 9 [t_8, t_9]: Mode 9 starts when Q_2 is turned on under ZVS. Since the equivalent circuit explaining the operation of this mode is the same as that shown in Fig. 6c, the voltage and current equations in this mode are identical to the analysis in mode 8. This mode ends when the auxiliary diode D_a reaches zero, and D_2 supplies all of the load current.

3 Relevant analysis results

3.1 Circulating current

Figure 7 shows a comparison of operation waveforms of the proposed and conventional converters.

Figure 7a shows the circulating current flowing through the transformer and the switches for an interval with a primary-side voltage V_P of 0 V, which is indicated by the shaded areas in the figure. This current, which does not contribute to power transmission, continuously flows through the inverter-stage switches and the transformer primary-winding, which results in additional conduction loss. In addition, this current increases the turn-off switching loss when the lagging-leg switches Q_1 and Q_2 are turned off.

Figure 7b shows the circulating current in the proposed converter, which is indicated by the shaded area in the figure. From a comparison with the conventional converter, it can be clearly seen that the proposed converter features a smaller circulating current when compared to the conventional converter. Its principle can be explained by the following mechanism. In the mode where the primary-side voltage V_P is 0 V, the auxiliary diode D_a is in the on-state. Then, the transformer leakage inductance gets a voltage that resets the current flowing to 0A from the output stage due to the coupled-inductor circuit. As a result, the primary current i_P is reset to the transformer magnetizing current i_{Lm} for an interval of with a primary-side voltage V_P of 0 V. This results in a reduced circulating current and lower current stress when compared to the conventional converter.

3.2 Voltage gain analysis

As shown in Fig. 4, the voltage applied to the coupled inductor V_{CI} is $V_{in}/n - V_{out}$ during the power transmission mode and $-V_{out}/2$ during the freewheeling mode. Then, the

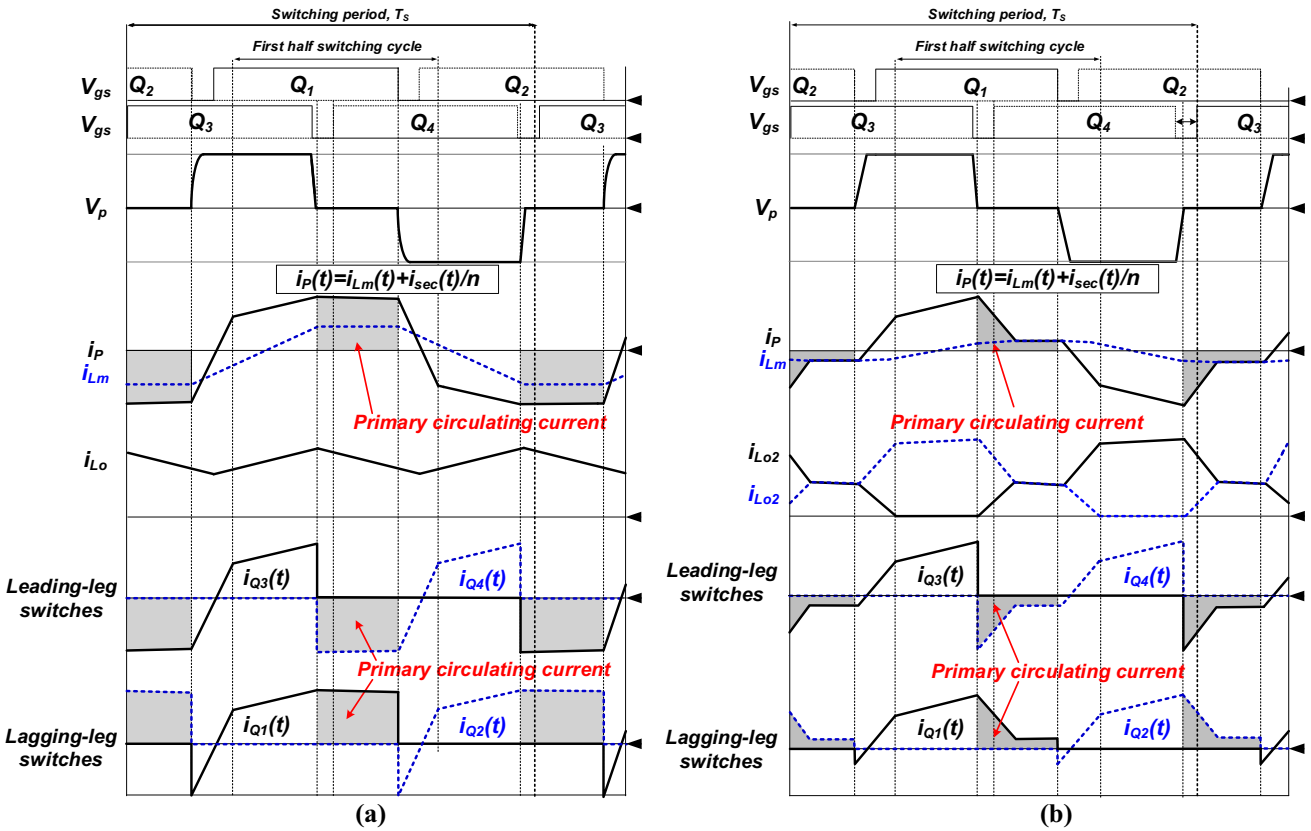


Fig. 7 Comparison of operating waveforms: a conventional converter; b proposed converter

voltage gain of the proposed circuit can be obtained with the voltage-second-balance principle as follows:

$$M = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{4D_{\text{eff}}}{n(1+2D_{\text{eff}})} \tag{23}$$

In Eq. (23), D_{eff} refers to an effective duty-cycle. Figure 8 shows the normalized voltage gain according to the effective duty-cycle. From this analysis, it can be clearly seen that the proposed converter has higher voltage gains when compared to the conventional converter. This advantage enables the proposed converter to have a much better turn-ratio n in terms of primary-side current and secondary-side voltage stresses when compared to the conventional converter.

3.3 Voltage stress analysis

The rectifier diodes in the conventional and proposed converters experience the highest voltage stress in the power transmission mode. In the case of the conventional converter with a center-tap rectifier circuit shown in Fig. 1, the rectifier diode has voltage stress of more than two times the voltage of the secondary-side windings of the transformer when considering that voltage rigging occurred by the parasitic components. This can be expressed as the following equation:

$$V_{D_1 \text{or} D_2} = \frac{2V_{\text{in}}}{n} + V_{\text{ringing}} \tag{24}$$

The voltage stress applied to the rectifier diode in the proposed converter is similar to Eq. (25). However, as explained in the previous part, the proposed converter can be designed with a higher transformer turn-ratio n than the conventional converter under the same duty-cycle due to higher voltage gains. As a result, the voltage stress of the rectifier diodes in the proposed circuit is lower than that of the conventional converter. This means that when an RCD snubber circuit with the same time-constant is used, the snubber loss in the proposed circuit is much lower than that in the conventional converter. In addition, diodes with lower forward-voltage drop can be used for the proposed converter due to its lower voltage stress, which can enable an improvement of the conduction loss at the rectifier stage.

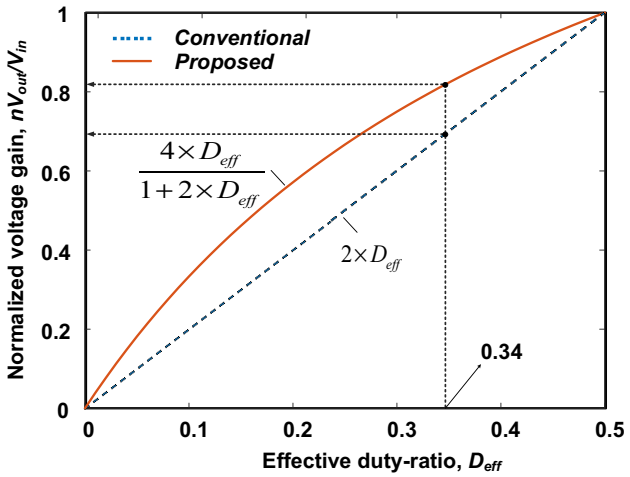


Fig. 8 Normalized voltage gain

3.4 ZVS condition analysis

Zero-voltage switching (ZVS) of the leading-leg switches in the proposed converter can be easily achieved over a wide load variation due to the large magnetizing inductance of the coupled inductor. This principle is similar to that of the leading-leg switches in the conventional converter [16, 28].

The ZVS operation of the lagging-leg switches in the proposed converter was explained in the analysis of mode 7 in the previous section. From Eq. (14) and Fig. 4, the ZVS condition for the lagging-leg switches of the proposed converter can be set up as follows:

$$V_{Q1}(t_7) = \frac{nV_{\text{out}}}{2} + \sqrt{\frac{L_{lkg}}{2C_{\text{OSS}}}} i_P(t_6) sin \frac{1}{\sqrt{2C_{\text{OSS}}L_{lkg}}}(t_7 - t_6) >> V_{\text{in}} \tag{25}$$

The $i_P(t_6)$ in Eq. (14) can be easily obtained as in Eq. (15) by analyzing Fig. 4.

$$i_P(t_6) \approx \frac{D_{\text{eff}} T_S V_{\text{in}}}{2L_m} \tag{26}$$

When assuming the interval of mode 7 with T_{dead}, which is the dead-time between Q_1 and Q_2, the ZVS condition of Eq. (25) can be expressed as follows:

$$\begin{aligned} &\sqrt{\frac{L_{lkg}}{2C_{\text{OSS}}}} i_P(t_6) sin \frac{1}{\sqrt{2C_{\text{OSS}}L_{lkg}}}(T_{\text{dead}}) >> V_{\text{in}} - \frac{nV_{\text{out}}}{2} \\ &\Rightarrow \sqrt{\frac{L_{lkg}}{2C_{\text{OSS}}}} i_P(t_6) \frac{T_{\text{dead}}}{\sqrt{2C_{\text{OSS}}L_{lkg}}} >> V_{in} - \frac{nV_{\text{out}}}{2} \end{aligned} \tag{27}$$

By putting Eq. (26) into Eq. (27), the design equation for the transformer magnetizing inductance guaranteeing the ZVS operation of the lagging-leg switches can be obtained as follows:

$$L_m << \frac{D_{\text{eff}} T_S T_{\text{dead}}}{2C_{\text{OSS}}} \left(2 - \frac{nV_{\text{out}}}{V_{\text{in}}}\right)^{-1} \tag{28}$$

3.5 Duty-cycle loss

The conventional converter in Fig. 1 requires an additional inductor in series with the transformer to extend the ZVS

range of the lagging-leg switches. However, this additional inductor reduces the effective duty-cycle and narrows the power transmission interval. Then, the wanted output voltage or current cannot be achieved. To compensate for this, the transformer turn-ratio n should be lowered, which greatly increases the primary-side current and secondary-side voltage stresses. It also causes an increase in snubber loss and conduction loss.

On the other hand, ZVS of the lagging-leg switches in the proposed converter can be extended by decreasing the transformer magnetizing inductance as in Eq. (28). The transformer magnetizing inductance has the advantage of not generating the problems related to duty-cycle loss since it forms a parallel connection with the output load.

4 Experimental results

To demonstrate the validity of the proposed converter, prototype converters were designed and manufactured with the following specifications. To mitigate voltage overshoots and oscillation, prototype converters were built by adding snubber circuits. The design specifications for the prototypes are as follows:**

Input voltage: $V_{in} = 300–400$ V
Output voltage: $V_{out} = 50$ V
Maximum output current: $I_{out(max)} = 20$ A
Switching frequency: $f_s = 100$ kHz

Table 1 shows a list of the components used to build the prototypes, and Fig. 9 shows photos of the manufactured converters.

The equation for designing the coupled inductor in the proposed converter can be set up from Fig. 4, Eq. (1) and (2).

$$L_{CI} > \frac{D_{eff} T_S}{\Delta I_{L_{CI}}} \left(\frac{V_{in}}{n} - V_{out} \right) \tag{29}$$

For a small core loss, an appropriate current ripple is selected. Then, the magnetizing inductance L_{CI} can be designed with Eq. (29). The size of the core for the coupled inductor can be selected with the required L_{CI} and the magnitude of the current flowing through the coupled inductor. Once the size of the core is determined, the turns of the windings can be determined from Faraday's law from the effective cross-sectional area of the core and the level of the voltage across the coupled inductor in Fig. 4. The proposed converter needs a coupled inductor with a turn-ratio of 1:1 and a high coupling coefficient. For a high coupling coefficient, the coupled inductor for the proposed converter was made with the bifilar winding method in [34].

The prototype converters were regulated with a TMS320F28335-based controller.

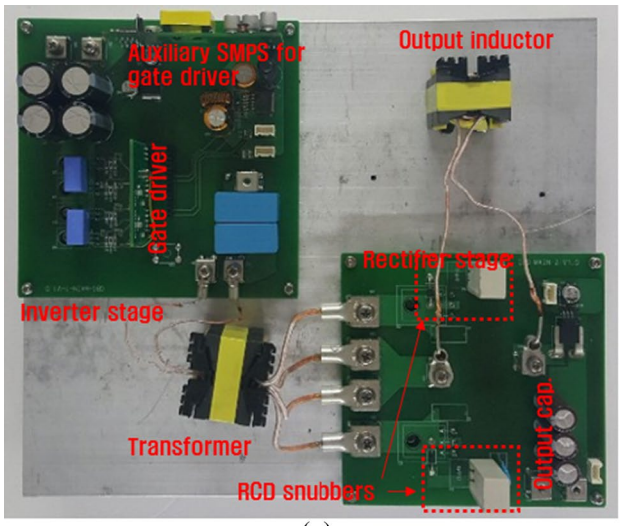
4.1 Waveforms

Figures 10 and 11 show key operating-waveforms of the proposed and conventional converters at a 300 V or 400 V input and 50 V and 20 A outputs. From Figs. 10b and 11b, it is confirmed that all of the measured waveforms follow the operation analyzed in Fig. 4 and Sect. 2 well. It is also confirmed that the proposed converter has a significantly reduced circulating current when compared to the conventional converter. In addition, it is clearly verified from the value of $I_{p(rms)}$ in the figures that the primary RMS (root-mean-square) current stress is decreased due to the reduction of the circulating current.

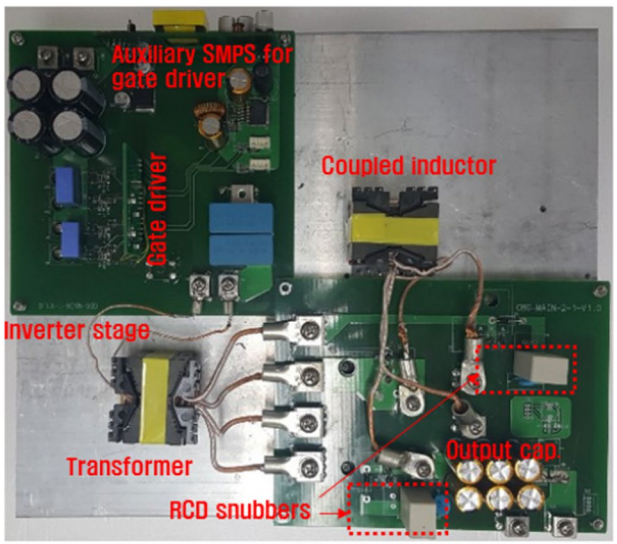
Figures 12, 13, and 14 show the inverter output voltage $V_p(t)$, primary current $i_p(t)$, and rectifier diode voltages of the proposed converter at input voltages of 300 V and 400 V according to the load currents. These experiments verify that the ZVS of the lagging-leg switches in the

Table 1 Prototype converter components

Device	Conventional	Proposed
Input Capacitor	Electrolytic capacitor, 47 μF/450 V/3 parallels	
Switch	NTP082N65S3F (650 V/40 A/82 mΩ)	
Diode	DPG60C300HB(300 V/60 A/1.34 V)	
Output Inductor	Core: PQ4040 20 μH	Core: PQ4040 Turn ratio = 1:1 Lm = 100μH Llk = 1.6μH
Transformer	Core: PQ4040 40 T: 10 T: 10 T $L_m = 300$ μH $L_{lk} = 20$ μH	Core: PQ4040 40 T: 8 T: 8 T $L_m = 300$ μH $L_{lk} = 20$ μH
Output capacitor	Electrolytic capacitor, 47 μF/68 V/6 parallels	
RCD snubber	UF4004, 10 nF/1 kV, 10 kΩ/20 W	



(a)



(b)

Fig. 9 Prototype photos: **a** conventional converter; **b** proposed converter

proposed converter can be effectively achieved over wide load conditions.

4.2 Diode voltage stress

Figure 15 shows the voltage stress of the rectifier diodes at an input voltage of 400 V and an output of 50 V and 1 kW using the same snubber circuit. The snubber circuit design can be seen in Table 1. As shown by the experimental results in Fig. 15, since the proposed converter is made with a higher transformer turn-ratio n due to higher voltage gains than the conventional converter, it is confirmed that the voltage stress is reduced by more than 39 V. The reduced voltage stress means that the proposed converter has a lower snubber loss when compared to the proposed converter.

4.3 Efficiency

Figure 16 shows the efficiency measured using a power analyzer (WT500, YOKOGAWA) under input voltage 300 V and 100% load conditions. As can be seen from these experimental results, the proposed converter achieves a higher power conversion efficiency. Figure 17 shows an efficiency curve according to the output load conditions. As shown in Fig. 17, the proposed converter has a maximum efficiency of 94.7%, and its efficiency is greatly improved when compared to the conventional converter. This is due to the fact that the conduction loss of the proposed converter is reduced as a result of the reduction in the circulating current and the turn-off switching loss. In addition, the reduction in the snubber loss due to lower voltage stress on the secondary-side rectifier diode also contributes to improved efficiency. Figure 18 shows the loss reduction factor of the proposed converter by analyzing the losses for each of the elements in the proposed and conventional converters.

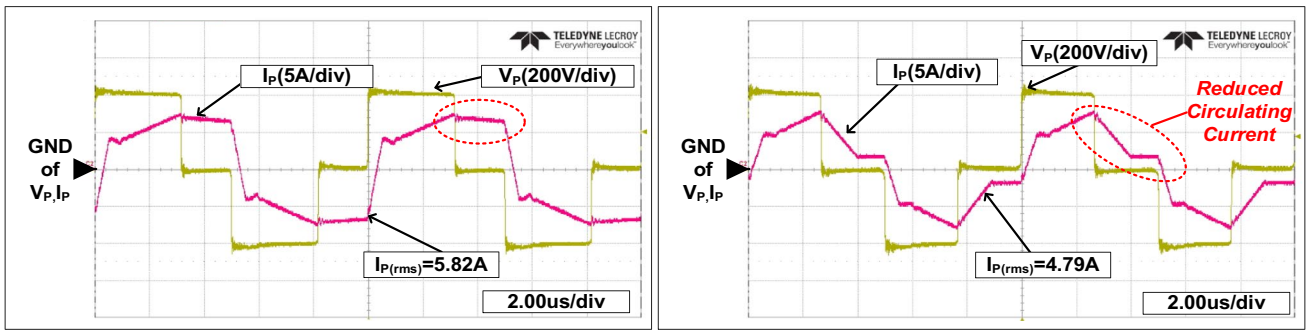


Fig. 10 Key waveforms of the prototype converters at input voltage 300 V and 100% load: **a** conventional converter; **b** proposed converter

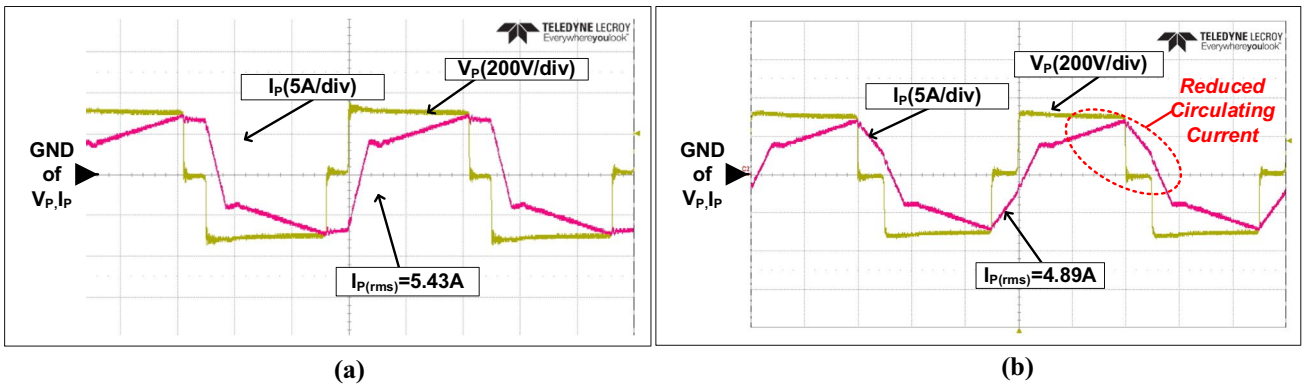


Fig. 11 Key waveforms of the prototype converters at input voltage 400 V and 100% load: **a** conventional converter; **b** proposed converter

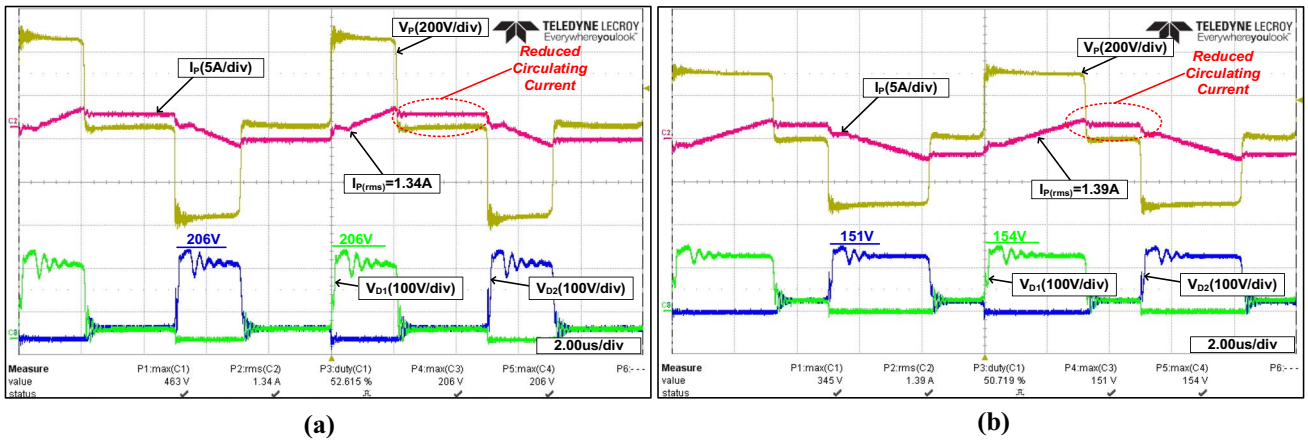


Fig. 12 Key waveforms of the proposed converter at 10% load: **a** input voltage 400 V; **b** input voltage 300 V

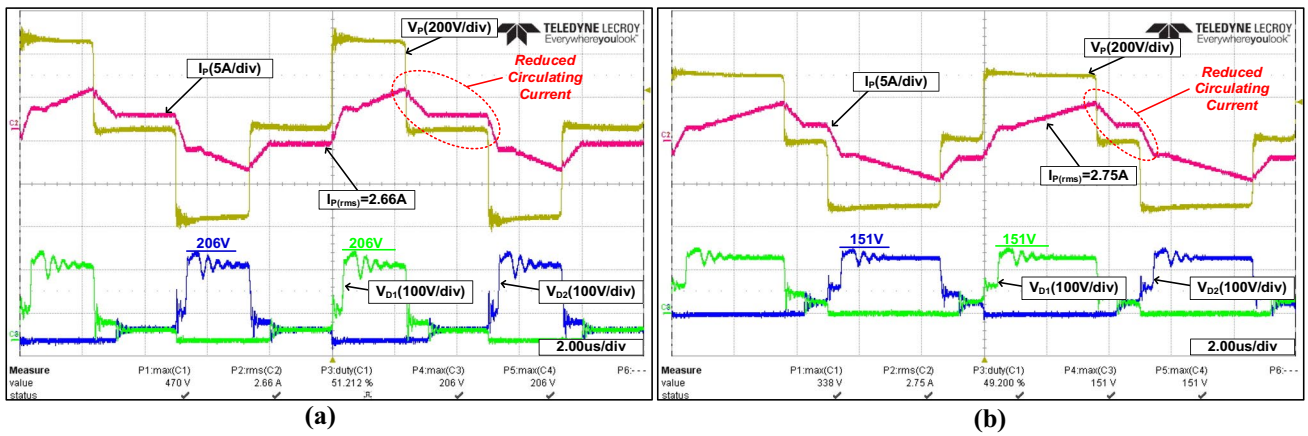


Fig. 13 Key waveforms of the proposed converter at 50% load: **a** input voltage 400 V; **b** input voltage 300 V

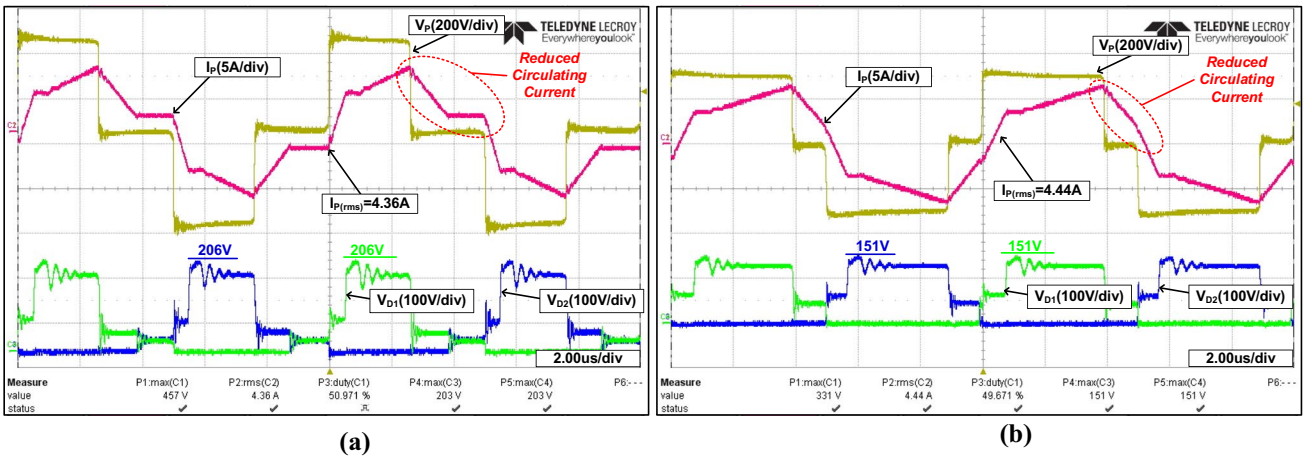


Fig. 14 Key waveforms of the proposed converter at 80% load: **a** input voltage 400 V; **b** input voltage 300 V

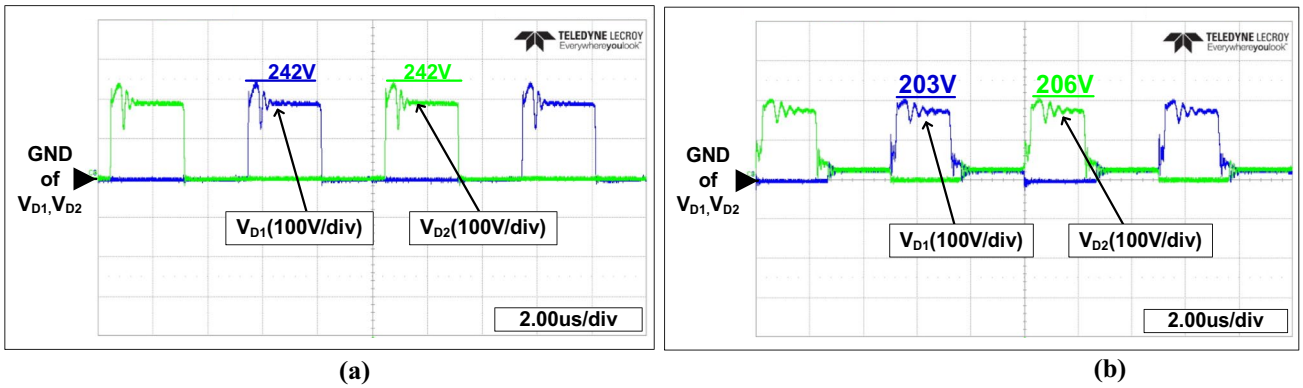


Fig. 15 Rectifier diode voltage stress of the prototype converters at input voltage 400 V and 100% load: **a** conventional converter; **b** proposed converter

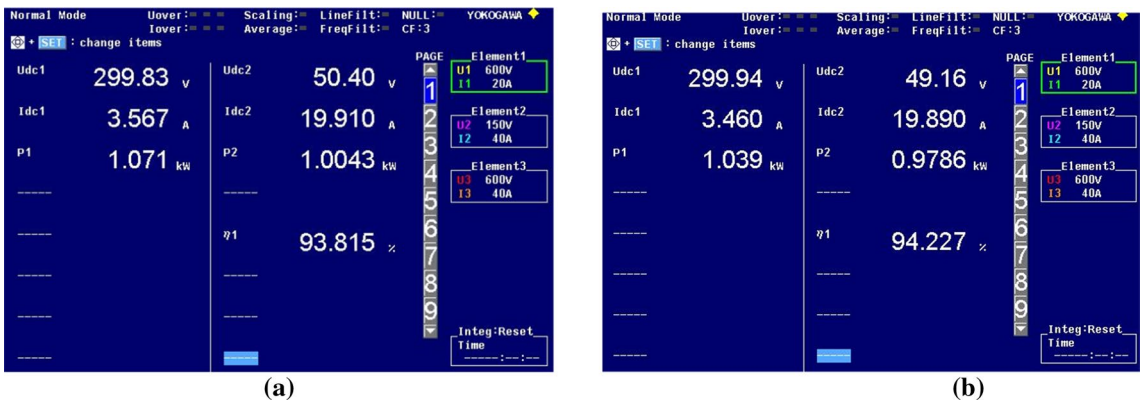


Fig. 16 Measured Efficiency at input voltage 300 V, output voltage 50 V, and output power 1.0 kW: **a** conventional converter; **b** proposed converter

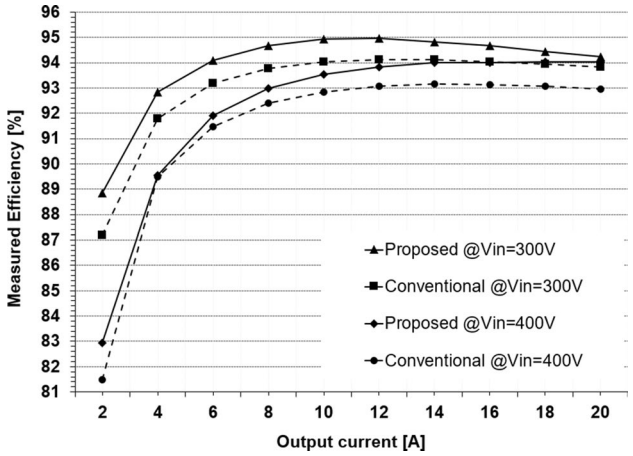


Fig. 17 Measured efficiencies according to the load conditions

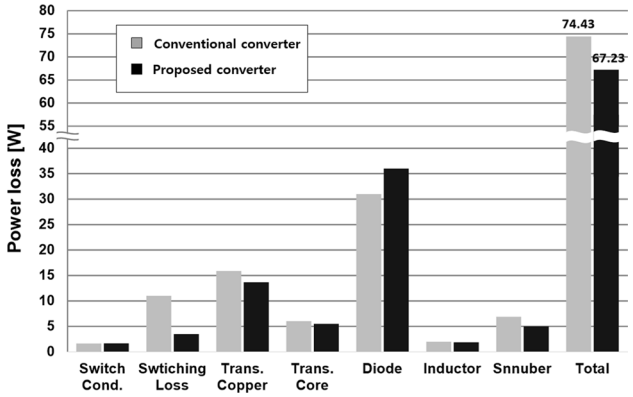


Fig. 18 Loss breakdown of the prototype converters at input voltage 400 V, output voltage 50 V, and output power 1.0 kW

5 Conclusions

This paper presents a PSFB converter that can improve the performance of a PSFB converter with a center-tap rectifier circuit. To achieve this improvement, the proposed converter relaces the output inductor with a single coupled inductor and adds an auxiliary diode. With these structural changes, the proposed converter achieves the following advantages:

(1) Reductions in the conduction loss and turn-off switching loss due to a reduction in the circulating current.
(2) Reductions in the rectifier diode voltage stress and snubber loss by the feature of a higher voltage gain.
(3) Soft-switching of the lagging-leg switches independent of load conditions due to the transformer magnetizing inductance.

Due to the above advantages, the proposed converter can achieve higher efficiency than the conventional converter. To confirm the superiority of the proposed converter, this paper presents the operating principle, steady-state analysis, and experimental results under a 1.0 kW, 300–400 V input voltage, and a 50 V output voltage. From the theoretical analysis and experimental results, it can be concluded that the proposed converter is applicable to low voltage, high current, and wide input or output operating applications such as data-center power supplies, communication equipment power supplies, and battery chargers for neighborhood electric vehicles.

Acknowledgements This paper is the result of a study conducted with the support of the Ministry of Trade, Industry and Energy and the Korea Institute of Trade, Industry and Technology Promotion's National Innovation Cluster Project (P0015364).

References

1. Wang, L., Zhu, Q., Yu, W., Huang, A.Q.: Efficiency and conducted EMI evaluation of a single-phase power factor correction boost converter using stage-of-the-art SiC mosfet and SiC diode. IEEE Trans. Ind. Appl. **55**(6), 7745–7756 (2019)
2. Liu, Z., Li, B., Lee, F.C., Li, Q.: High-efficiency high-density critical mode rectifier/inverter for WBG-device-based on-board charger. IEEE Trans. Ind. Electron. **64**(11), 9114–9123 (2017)
3. Elrajoubi, A.M., Ang, S.S., George, K.: Design and analysis of a new GaN-based AC/DC converter for battery charging application. IEEE Trans. Ind. Appl. **55**(4), 4044–4052 (2019)
4. Whitaker, B., Barkley, A., Cole, Z., Passmore, B., Martin, D., McNutt, T.R., Lostetter, A.B., Lee, J.S., Shiozaki, K.: A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices. IEEE Trans. Power Electron. **29**(5), 2606–26177 (2014)
5. Banaei, M.R., Sani, S.G.: Analysis and implementation of a new SEPIC-based single-switch buck-boost DC-DC converter with continuous input current. IEEE Trans. Power Electron. **33**(12), 10317–10325 (2018)
6. Shi, K., Zhang, D., Zhou, Z., Zhang, M., Zhang, D., Gu, Y.: A novel phase-shift dual full-bridge converter with full soft-switching range and wide conversion range. IEEE Trans. Power Electron. **31**(11), 7747–7760 (2016)
7. Ravi, V., Kanamarlapudi, K., Wang, B., Kandasamy, N.K., So, P.L.: A new ZVS full-bridge DC-DC converter for battery charging with reduced losses over full-load range. IEEE Trans. Ind. Appl. **54**(1), 571–579 (2018)
8. Koo, G.B., Moon, G.W., Youn, M.J.: New zero-voltage-switching phase-shift full-bridge converter with low conduction losses. IEEE Trans. Ind. Electron. **52**(1), 228–235 (2005)
9. Chen, B.Y., Lai, Y.S.: Switching control technique of phase-shift-controlled full-bridge converter to improve efficiency under light-load and standby conditions without additional auxiliary components. IEEE Trans. Power Electron. **25**(4), 1001–1012 (2010)
10. Lin, S.Y., Chen, C.L.: Analysis and design for RCD clamped snubber used in output rectifier of phase-shift full-bridge ZVS converters. IEEE Trans. Ind. Electron. **45**(2), 358–359 (1998)
11. Woo, J., Kim, D., Kim, C., Moon, G.: A simple switching control technique for improving light load efficiency in a phase-shifted full-bridge converter with a server power system. IEEE Trans. Power Electron. **29**(4), 1562–1566 (2014)

12. Kasper, M., Bortis, D., Deboy, G., Kolar, J.W.: Design of a highly efficient (97.7%) and very compact (2.2 kW/dm 3) isolated AC–DC telecom power supply module based on the multicell ISOP converter approach. IEEE Trans. Power Electron **32**(10), 7750–7769 (2017)
13. Kim, Y., Oh, C., Sung, W., Lee, B.: Topology and control scheme of OBC–LDC integrated power unit for electric vehicles. IEEE Trans. Power Electron. **32**(3), 1731–1743 (2017)
14. Dudrik, J., Trip, N.D.: Soft-Switching PS-PWM DC-DC converter for full-load range applications. IEEE Trans. Ind. Electron. **57**(8), 2807–2814 (2010)
15. Mousavi, A., Das, P., Moschopouos, G.: A ZVS pulsewidth modulation full-bridge converter with a low-RMS-current resonant auxiliary circuit. IEEE Trans. Power Electron. **31**(6), 4031–4047 (2016)
16. Lee, I.O., Moon, G.W.: Soft-switching DC/DC converter with a full ZVS range and reduced output filter for high-voltage applications. IEEE Trans. Power Electron. **28**(1), 112–122 (2013)
17. Gu, B., Lai, J., Kees, N., Zheng, C.: Hybrid-switching full-bridge DC–DC converter with minimal voltage stress of bridge rectifier, reduced circulating losses, and filter requirement for electric vehicle battery chargers. IEEE Trans. Power Electron. **28**(3), 1132–1144 (2013)
18. Chen, Z., Chen, Y., Chen, Q.: Isolated series-capacitor-based full-bridge converter with reduced circulating losses and wide soft switching range. IEEE J. Emerg. Sel. Top. Power Electron. **7**(2), 1272–1285 (2019)
19. Wu, X., Xie, X., Zhang, J., Zhao, R., Qian, Z.: Soft switched full bridge DC–DC converter with reduced circulating loss and filter requirement. IEEE Trans. Power Electron. **22**(5), 1949–1955 (2007)
20. Lee, I., Moon, G.: Phase-shifted PWM converter with a wide zvs range and reduced circulating current. IEEE Trans. Power Electron. **28**(2), 908–919 (2013)
21. Song, T.T., Huang, N.: A novel zero-voltage and zero-current-switching full-bridge PWM converter. IEEE Trans. Power Electron. **20**(2), 286–291 (2005)
22. Seok, K., Kwon, B.: An improved zero-voltage and zero-current-switching full-bridge PWM converter using a simple resonant circuit. IEEE Trans. Ind. Electron. **48**(6), 1205–1209 (2001)
23. Kim, E., Kim, Y.: A ZVZCS PWM FB DC/DC converter using a modified energy-recovery snubber. IEEE Trans. Ind. Electron. **49**(5), 1120–1127 (2002)
24. Wu, X., Xie, X., Zhao, C., Qian, Z., Zhao, R.: Low voltage and current stress ZVZCS full bridge DC-DC converter using center tapped rectifier reset. IEEE Trans. Ind. Electron. **55**(3), 1470–1477 (2008)
25. Cha, H., Chen, L., Ding, R., Tang, Q., Peng, F.Z.: An alternative energy recovery clamp circuit for full-bridge PWM converters with wide ranges of input voltage. IEEE Trans. Power Electron. **23**(6), 2828–2837 (2008)
26. Ruan, X., Yan, Y.: A novel zero-voltage and zero-current-switching PWM full-bridge converter using two diodes in series with the lagging leg. IEEE Trans. Ind. Electron. **48**(4), 777–785 (2001)
27. Park, K., Kim, C., Moon, G., Youn, M.: Voltage oscillation reduction technique for phase-shift full-bride converter. IEEE Trans. Ind. Electron. **54**(5), 2779–2790 (2007)
28. Lee, I.O., Moon, G.W.: Half-bridge integrated ZVS full-bridge converter with reduced conduction loss for electric vehicle battery chargers. IEEE Trans. Ind. Electron. **61**(8), 3978–3988 (2014)
29. Ayyanar, R., Mohan, N.: Novel soft-switched DC-DC converter with full ZVS-range and reduced filter requirement–part I: Regulated-output applications. IEEE Trans. Power Electron. **16**(2), 184–192 (2001)
30. Ayyanar, R., Mohan, N.: Novel soft-switched DC-DC converter with Full ZVS-range and reduced filter requirement–part II: constant-input, variable-output applications. IEEE Trans. Power Electron. **16**(2), 193–200 (2001)
31. Lee, I.: Hybrid PWM-resonant converter for electric vehicle on-board battery chargers. IEEE Trans. Power Electron. **31**(5), 3639–3649 (2016)
32. Dao, L.A., Dao, N.D., Lee, D.C.: High-efficiency hybrid LLC resonant converter for on-board chargers of plug-in electric vehicles. IEEE Trans. Power Electron. **35**(8), 8324–8334 (2020)
33. Han, J., Moon, G.: High-efficiency phase-shifted full-bridge converter with a new coupled inductor rectifier (CIR). IEEE Trans. Power Electron. **34**(9), 8468–8480 (2019)
34. Jung, J.H.: Bifilar winding of a center-tapped transformer including integrated resonant inductance of LLC resonant converter. IEEE Trans. Power Electron. **28**(2), 615–620 (2013)

Byoung-Gi Choi received his B.S. degree in Electronics Engineering from Gangneung-Wonju National University, Gangneung, South Korea, in 2015; and his M.S. degree in Electrical Engineering from Myongji University, Yongin, South Korea, in 2021. His current research interests include the control and design of high-power DC-to-DC converters.

Woo-Seok Lee received his B.S. and M.S. degrees in Electronics Engineering from Keimyung University, Daegu, South Korea, in 2015 and 2017, respectively. He is presently working towards his Ph.D. degree at Myongji University, Yongin, South Korea. His current research interests include high efficiency and high power-density battery chargers for electric vehicles, power-factor correction topologies, and digital control.

Jeong-Uk Park received his B.S. degree in Electrical Engineering from Myongji University, Yongin, South Korea, in 2020, where he is presently working towards his M.S. degree. His current research interests include inductive wireless electric vehicle battery charging systems.

Il-Oun Lee received his B.S. degree in Electrical and Electronic Engineering from Kyungpook National University, Daegu, South Korea, in 2000; his M.S. degree in Electrical Engineering from Seoul National University, Seoul, South Korea, in 2002; and his Ph.D. degree from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2013. From 2003 to 2008, he was a Manager in the Plasma Display Panel Development Group, Samsung SDI, Cheonan, South Korea. From 2008 to 2013, he was a Senior Engineer in the Power Advanced Development Group, Samsung Electro-Mechanics Co. Ltd., Suwon, South Korea. From 2013 to 2015, he was a Senior Researcher in the Energy Saving Lab., Korea Institute of Energy Research (KIER), Daejeon, South Korea. From 2015 to 2017, he was an Associate Professor in the School of Electrical and Electronics Engineering, Keimyung University, Daegu, South Korea. In 2017, he joined the Department of Electrical Engineering, Myongji University, Yongin, South Korea, as an Associate Professor. His current research interests include DC-DC converters, power factor correction (PFC) AC-DC converters, LED drivers, battery chargers for electric vehicles, digital display power systems, and digital control approaches for DC-DC converters. Dr. Lee is a member of the Korea Institute of Power Electronics, the IEEE Industrial Electronics Society, and the IEEE Power Electronics Society.