Journal of Power Electronics (2021) 21:1123–1134
https://doi.org/10.1007/s43236-021-00259-z

ORIGINAL ARTICLE

SVPWM algorithm for five-level active-neutral-point-clamped H-bridge inverters

Linfei Jiang[1] · **Fei Xiao**[1] · **Liangdeng Hu**[1] · **Yingjie Jia**[1]

Received: 16 December 2020 / Revised: 21 April 2021 / Accepted: 24 April 2021 / Published online: 19 May 2021

Abstract
When compared with the three-level H-bridge inverter, the five-level active-neutral-point-clamped (5L-ANPC) H-bridge inverter has high output voltage level, high output power, and lower current harmonic content. Thus, it has the potential to be applied to the vessel integrated power systems. This paper proposes a method of space vector pulse width modulation (SVPWM) for the 5L-ANPC H-bridge inverter. First, the selection of the available switching vectors is based on an analysis of the switching constraints, switching times, and common-mode voltage. Then, according to the control requirements of the neutral-point potential and the floating capacitor voltage of the inverter, the action time of each switching vector is calculated. The sequence of the switching vectors in different intervals is determined based on the principle of reducing the switching times. Finally, a hardware-in-loop (HIL) real-time simulation experimental platform is established to verify the proposed method.

Keywords Five-level active-neutral-point-clamped (5L-ANPC) · H-bridge · SVPWM · Multilevel inverter

1 Introduction

To adapt to load power increases and to meet the needs of vessel propulsion, the DC voltage of the vessel integrated power system (IPS) will be upgraded to a higher voltage level in the future. Due to limitations imposed by the circuit topology and power device voltage-proof capability, the existing three-level topology cannot be applied to the higher voltage level if the power devices are not connected in series [1].

In recent years, many types of medium–high voltage converter topologies have been developed. However, they are not suitable for vessel propulsion systems due to various shortcomings. The diode-clamped multilevel converter requires many clamping diodes, which makes the capacitor voltage difficult to balance. The flying-capacitor multilevel converter needs a lot of clamping capacitors, which leads to an increase in the system cost and volume. The cascaded H-bridge converter requires a lot of independent DC power supplies or phase-shifting transformers. Thus, it becomes bulky and cannot easily fulfil energy feedback. Modular multilevel converters have attracted a great deal of attention in recent years. The overall structure of these systems is flexible and simple. However, the capacitor voltage of the submodule tends to fluctuate sharply at low frequencies. At present, there is no perfect solution. Therefore, its application is limited to vessel propulsion [2]. In 2005, Swiss scholars presented the topology of a five-level active-neutral-point-clamped-converter (5L-ANPC). Due to its advantages of being supplied by the DC bus and performing energy feedback easily, the 5L-ANPC topology has become a research hotspot in terms of medium–high voltage variable frequency speed regulation [3].

A medium–high voltage multi-phase motor with open windings can meet the requirements of large capacity, high reliability, and high torque density of vessel electric propulsion systems. A multi-phase multilevel H-bridge topology inverter that matches the motor has become an optimal option for the large-capacity propulsion systems in vessels due to its simple main circuit, good frequency-doubling effect, and high fault-tolerant capability [4]. Depending on the demand for propulsion power by a large vessel, the propulsion motor adopts the multi-phase and multi-channel open winding scheme, and the inverter can adopt

✉ Linfei Jiang
1039346186@qq.com

[1] National Key Laboratory of Science and Technology on Vessel Integrated Power System, Naval University of Engineering, Wuhan, China

a multi-phase H-bridge topology scheme based on the 5L-ANPC [5].

A great deal of research has been carried out on the 5L-ANPC inverter. In [6–9], carrier pulse width modulation methods have been used to control the 5L-ANPC inverter. These methods are simple. However, there is a coupling in the control of the neutral-point potential (NPP) and the floating capacitor voltage (FCV). When carrier PWM is applied to the 5L-ANPC H-bridge topology to double the equivalent switching frequency, the difference in the carrier phase between the right and left arms of the H-bridge is 180°, which leads to a difference between the peak and valley of the triangular carrier wave of the other arm as well as the sampling moment of the modulation wave. At this time, a narrow pulse is apt to appear, which threatens the operation of the device. In [10–12], SHE-PWM was used to control the 5L-ANPC. However, the calculation complexity makes it impossible to control the system in real-time. In [13], the space vector modulation algorithm was used to control a three-phase 5L-ANPC to balance the NPP and the FCV. However, due to the low switching frequency of the 5L-ANPC H-bridge inverter, this algorithm leads to large fluctuations in the capacitor voltage. Therefore, this algorithm is not applicable to the 5L-ANPC H-bridge inverter. In [14], a hybrid SVPWM modulation algorithm was proposed to reduce the control complexity when compared with the conventional 5L-SVPWM. However, it is not suitable for the 5L-ANPC H-bridge inverter. In [15], to reduce the calculation amount, an optimal model predictive control (O-MPC) method was proposed to control a 5L-ANPC converter. However, the 5L-ANPC H-bridge inverter has more output levels, which results in a larger calculation amount. This method is not suitable for the 5L-ANPC H-bridge inverter. In [16], a model predictive control was proposed to eliminate common-mode voltages (CMVs) of a three-phase 5L-ANPC converter. However, the 5L-ANPC H-bridge inverter is different from the three-phase 5L-ANPC. Thus, the method is not suitable for the 5L-ANPC H-bridge inverter. In [17–19], based on a detailed analysis of the traditional single-phase multilevel algorithm, the process of the single-phase SVPWM algorithm was simplified. However, this is only applicable to the multi-level topology of the two-level H-bridge cascading topology. It is not applicable to the 5L-ANPC H-bridge topology due to switching state constraints. In [20], the SVPWM algorithm was optimized on the principle of minimizing the switching times for the single-phase neutral-point clamped cascaded H-bridge inverter. However, the 5L-ANPC H-bridge inverter has more coupling floating capacitors. However, the algorithm cannot be directly used for the 5L-ANPC H-bridge inverter.

With the 5L-ANPC H-bridge inverter as an object of study, this paper proposes a space vector modulation algorithm to solve the problems of the narrow pulse in the carrier phase-shift modulation, and the coupling in the control of the NPP and the FCV. It also discusses how to select the switching vectors and how to balance the NPP and the FCV.

The remainder of this paper is organized as follows. Section 2 discusses the basic principle of the 5L-ANPC H-bridge inverter and the definitions of voltage vector and switching vector. Section 3 presents the composition of voltage vectors, the selection of switching vectors, and the control of the NPP and the FCV. Section 4 explains the algorithm. Section 5 describes real-time simulation experiments. Finally, Sect. 6 gives some conclusions.

2 5L-ANPC H-bridge inverter

A 5L-ANPC H-bridge inverter is shown in Fig. 1a. The inverter consists of two 5L-ANPC bridge arms sharing a DC bus. Both of the bridge arms are connected to one phase winding of the motor (the resistance inductance load is equivalent). For the sake of simplicity, one bridge arm is taken as an example, as shown in Fig. 1b. Suppose 4E is the DC bus voltage and NP is the neutral point of the DC supporting capacitors C_{d1} and C_{d2}. Under ideal conditions, the voltages of C_{d1} and C_{d2} should be kept equal to 2E, and the voltage of $C_{fx}(x=\mathrm{a,b})$ should be stabilized at E. It follows that the neutral-point current i_{NP} from the NP is positive, the output current i_x from the bridge is positive, the floating capacitor current i_{Cfx} from the positive pole of the floating capacitor is positive, V_{xo} is the output voltage, and the load current $i_{out}=i_a=-i_b$.

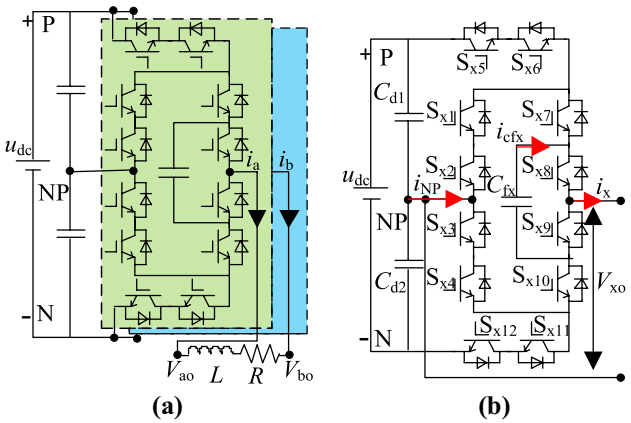


Fig. 1 Topology of a 5L-ANPC H-bridge inverter: **a** H-bridge; **b** bridge arm

Table 1 Switching states of 5L-ANPC bridge arms

S_5	S_7	S_8	V_O	i_{NP}	i_{Cf}	Switching state
0	0	0	$-2E$	0	0	V0
0	0	1	$-E$	0	i_{out}	V1
0	1	0	$-E$	i_{out}	$-i_{out}$	V2
0	1	1	0	i_{out}	0	V3
1	0	0	0	i_{out}	0	V4
1	0	1	E	i_{out}	i_{out}	V5
1	1	0	E	0	$-i_{out}$	V6
1	1	1	$2E$	0	0	V7

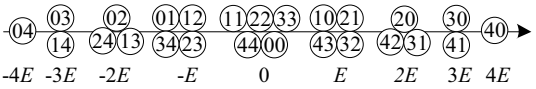


Fig. 2 Space voltage vector diagram of a 5L-ANPC H-bridge inverter

For the switches $S_{x1} - S_{x12}$, 0 indicates 'off" and 1 indicates 'on'. S_{x1}, S_{x3}, S_{X5}, S_{x11} and S_{x2}, S_{x4}, S_{x6}, S_{x12} are connected in series, respectively. The switching states of S_{x3}, S_{x4}, S_{x6}, and S_{x5} are the same; the switching states of S_{x1}, S_{x2}, S_{x11}, and S_{x12} are complementary to that of S_{x5}; the switching states of S_{x9} and S_{x8} are complementary, and the switching states of S_{x10} and S_{x7} are complementary. Therefore, the switching states of all the switches of the bridge arm are determined by those of S_{x5}, S_{x7}, and S_{x8}. Under normal operating conditions, the bridge arm has eight types of switching states, as shown in Table 1. If the NP is taken as the zero-potential reference, the five output levels corresponding to the bridge arm are: $+2E$, $+E$, 0, $-E$, and $-2E$.

The switching variables S_{ao} and S_{bo} are defined as the output voltage states of each bridge arm. The output voltage can be expressed as:

$$\begin{cases} V_{ao} = S_{ao} \cdot E \\ V_{bo} = S_{bo} \cdot E \end{cases} \tag{1}$$

where $S_{xo} = -2$, $S_{xo} = -1$, $S_{xo} = 0$, $S_{xo} = 1$, and $S_{xo} = 2$, which represent (V0), (V1,V2), (V3,V4), (V5,V6), and (V7), respectively.

It can be seen from Fig. 2 that in different combinations (such as 04), the two elements from left to right represent the switching states of the bridge arms a and b, respectively. The voltage levels ($-2E$, $-E$, 0, E, and $2E$) are numbered as 0, 1, 2, 3, and 4, respectively. According to the above definition, 25 output voltage states of the inverter are shown in Fig. 2, which are known as the space voltage vector.

The voltage vector of the inverter is defined as:

Table 2 Relationships between switching and voltage vectors

Voltage vector	Switching vector
4E	70
3E	72,71,60,50
2E	73,74,61,62,51,52,40,30
E	75,76,63,64,53,54,41,42,31,32,20,10
0	00,11,12,21,22,33,34,4344,55,56,65,66,77
− E	01,02,13,14,23,24,35,36,45,46,57,67
− 2E	03,04,15,16,25,26,37,47
− 3E	05,06,17,27,
− 4E	07

Table 3 Common-mode voltages of switching vectors

Switching vector	Common-mode voltage
70,61,62,51,52,33,34,43,44,15,16,25,26,07	0
72,71,60,50,63,64,53,54,41,42,31,32 13,14,23,24,35,36,45,46,05,06,17,27	$E/2$
73,74,40,30,11,12,21,22,55,56,65,66 03,04,37,47	E
75,76,20,10,01,02,57,67	$3E/2$
00,77	$2E$

$$\boldsymbol{V} = \boldsymbol{V}_{ao} + \boldsymbol{V}_{bo} \cdot e^{j\pi} \tag{2}$$

The maximum output voltage of the inverter is $+4E$ and the minimum output voltage is $-4E$. The inverter can output a total of nine levels.

The switching vector xy is used to represent the switching states of the bridge arms a and b, which are Vx and Vy (x,y = 0,1,…,7), as shown in Table 2.

Some of the switching vectors that do not meet certain conditions are eliminated according to the following principles:

1) The common-mode voltage of the H-bridge is defined as $V_{com}=(V_{ao}+V_{bo})/2$. V_{com} is as small as possible. The common-mode voltages of all the switching vectors are shown in Table 3. Any switching vector whose common-mode voltage is greater than $E/2$ is excluded.
2) The switchings between the switching vectors should be easy to perform. Undesirable output voltage jumps should be avoided during the switching process, and the switching times should be minimized. According to the state of the switches connected in series, V0–V7 are divided into two groups: G1{V0, V1, V2, V3} and G2{V4, V5, V6, V7}. According to these two groups, all of the switching process can be divided into two types. The first type is the switching process between G1 and G2. At this time, all of the switches connected in series and some of the non-series switches are required to act. The second type is the switching process within G1 or G2. At this time, there is only some non-series switches are required to act, and the switching loss is obviously lower. From an analysis of the switching process, it is known that when the switching states of two bridge arms belong to G1 or G2 at the same time, it is more possible for the first switching process to appear. Therefore, eight switching vectors such as G1G1 and G2G2 need to be eliminated. In addition, the first switching process only appears when the modulation wave crosses zero.

The expected output voltage is defined as $\boldsymbol{V}^*(n)$. Like three-phase SVPWM, the fundamental voltage vectors are selected according to the interval where $\boldsymbol{V}^*(n)$ is located. The voltage space is divided into eight linear modulation intervals by nine fundamental voltage vectors. As shown in Fig. 3, $\boldsymbol{V}^{-4}$, $\boldsymbol{V}^{-3}$, $\boldsymbol{V}^{-2}$, $\boldsymbol{V}^{-1}$, $\boldsymbol{V}^{0}$, $\boldsymbol{V}^{1}$, $\boldsymbol{V}^{2}$, $\boldsymbol{V}^{3}$, and $\boldsymbol{V}^{4}$ represent $-4E$, $-3E$, $-2E$, $-E$, 0, E, $2E$, $3E$, and $4E$, respectively.

Twenty-eight effective switching vectors are listed in Table 4. $\boldsymbol{V}^{4}$ and $\boldsymbol{V}^{-4}$ correspond to only one vector. $\boldsymbol{V}^{0}$ corresponds to two vectors. The remaining voltage vectors correspond to four vectors.

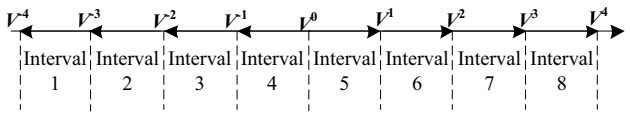


Fig. 3 Voltage space vector divisions

Table 4 Effective switching vectors of a 5L-ANPC H-bridge inverter

Fundamental voltage vector	Switching vector
$\boldsymbol{V}^{4}$ ($4E$)	70
$\boldsymbol{V}^{3}$ ($3E$)	72,71,60,50
$\boldsymbol{V}^{2}$ ($2E$)	61,62,51,52
$\boldsymbol{V}^{1}$ (E)	63,53,41,42
$\boldsymbol{V}^{0}$ (0)	34,43
$\boldsymbol{V}^{-1}$ ($-E$)	14, 24,35,36
$\boldsymbol{V}^{-2}$ ($-2E$)	15,16,25,26
$\boldsymbol{V}^{-3}$ ($-3E$)	05,06,17,27,
$\boldsymbol{V}^{-4}$ ($-4E$)	07

3 SVPWM algorithm

3.1 Composition principle of $\boldsymbol{V}^*$(n)

For the sake of a simplified analysis, $\boldsymbol{V}^*(n)$ is composed of two fundamental voltage vectors.

As shown in Fig. 4, the red line indicates $\boldsymbol{V}^*(n)<0$ and the blue line indicates $\boldsymbol{V}^*(n)>0$. The horizontal axis is the time axis, which is divided into several control cycles. The vertical axis represents the output voltage, and T_s is the control cycle. Two adjacent fundamental voltage vectors $\boldsymbol{V}_{low}$ and $\boldsymbol{V}_{high}$ can be used to compose $\boldsymbol{V}^*(n)$, whose action times are T_1 and T_2 in turn.

$\boldsymbol{V}_{low}$ and $\boldsymbol{V}_{high}$ are defined as:

$$\begin{cases} V_{low}(n) = \begin{cases} \text{floor}(V^*(n)) & V^*(n) \geq 0 \\ \text{ceil}(V^*(n)) & V^*(n) < 0 \end{cases} \\ V_{high}(n) = \begin{cases} \text{ceil}(V^*(n)) & V^*(n) \geq 0 \\ \text{floor}(V^*(n)) & V^*(n) < 0 \end{cases} \end{cases} \tag{3}$$

where floor is the round down function, and ceil is the round up function.

According to the 'Volt-Second', T_1 and T_2 can be calculated as follows:

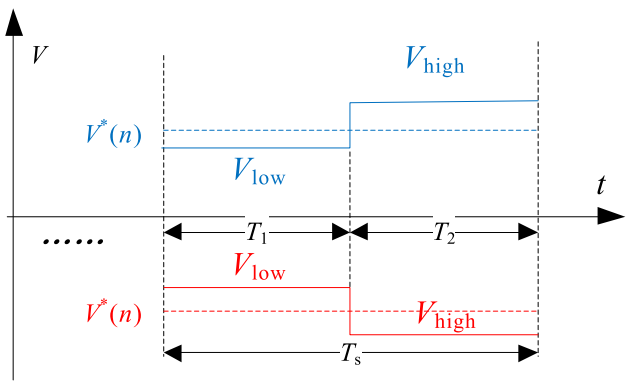


Fig. 4 Composition of two fundamental voltage vectors

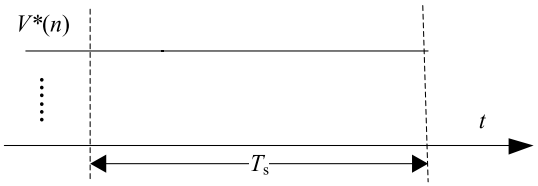


Fig. 5 Single voltage vector diagram

$$\begin{cases} T_1 = \left| \dfrac{V^*(n) - V_{\text{low}}(n)}{V_{\text{high}}(n) - V_{\text{low}}(n)} \right| T_{\text{s}} \\ T_2 = \left| \dfrac{V^*(n) - V_{\text{high}}(n)}{V_{\text{low}}(n) - V_{\text{high}}(n)} \right| T_{\text{s}} \end{cases} \tag{4}$$

The range of $V^*(n)$ is $-4E \le V^*(n) \le 4E$. Generally, $V^*(n)$ is composed of two fundamental voltage vectors. However, when $V^*(n)$ is equal to one of $\{-4E, -3E, -2E, -E, 0, E, 2E, 3E, 4E\}$, there is no need to use two fundamental voltage vectors to compose $V^*(n)$. Only the fundamental voltage vector equal to $V^*(n)$ is used, and its action time is T_{s}, as shown in Fig. 5.

3.2 Balanced control of the NPP and the FCV

During the operation of the inverter, many non-ideal effects cause the capacitor voltage to deviate from its set value.

By assigning different action times to the switch vectors, NPP can be controlled. When T_{s} is much smaller than the fundamental period, the neutral-point current can be regarded as constant in a control cycle. At this time, the additional average neutral-point current required in a control cycle can be calculated according to the NPP deviation as follows:

$$\bar{i}_{\text{NP}} = -C_{\text{d}} \Delta u_{\text{cd}} / T = -C_{\text{d}} \frac{(u_{\text{cd1}} - u_{\text{cd2}})}{T_{\text{s}}} \tag{5}$$

where Δu_{cd} is the deviation of the NPP, and C_{d} is the capacitance of the DC capacitors.

The control algorithm of the FCV is similar to that of the NPP. Its calculation is as follows:

$$\bar{i}_{\text{cfx}} = C_{\text{f}} \Delta u_{\text{cfx}} / T_{\text{s}} = C_{\text{f}} \frac{(u_{\text{cfx}} - u_{\text{dc}}/4)}{T_{\text{s}}} \tag{6}$$

where Δu_{cfx} is the voltage deviation of the FCV, C_{f} is the capacitance of the floating capacitor, and u_{cfx} is the voltage of the floating capacitor.

3.3 Composition of the switching vectors

3.3.1 *V**(n) is composed of two voltage vectors

$V^*(n)$ is composed of V_{high} and V_{low}. Suppose V_{high} is composed of switching vectors S_i ($i = 1,2\ldots,m$). Their action time is $t_{\text{h}i}$ ($i = 1,2\ldots,m$). Suppose V_{low} is composed of switching vectors S_j ($j = 1,2\ldots,n$). Their action time is $t_{\text{l}j}$($i = 1,2\ldots,n$).

$$\begin{cases} \sum_{i=1}^{m} t_{\text{h}i} = T_2 \\ \sum_{i=1}^{n} t_{\text{l}i} = T_1 \end{cases} \tag{7}$$

For each interval, the sequence of the switching vectors of $V^*(n)$ is analyzed below.

(1) V^*(n) in interval 1, 4, 5, or 8

For example, when $V^*(n)$ is located in interval 8, V_{low} and V_{high} correspond to V^3 and V^4, respectively. V_{high} corresponds to switching vector 70 and its action time is T_2. V_{low} corresponds to switching vectors 50, 71, 60, and 72, and their action times are t_1, t_3, t_5, and t_7, which satisfy $t_1 + t_3 + t_5 + t_7 = T_1$.

According to the control method of the NPP and the FCV, the equation for t_1, t_3, t_5, and t_7 is as follows:

$$\begin{cases} t_1 + t_3 + t_5 + t_7 = T_1 \\ i_{\text{a}} t_1 - i_{\text{a}} t_7 = -(u_{\text{cd1}} - u_{\text{cd2}}) C_{\text{d}} \\ -i_{\text{a}} t_5 + i_{\text{a}} t_1 = (u_{\text{cfa}} - u_{\text{dc}}/4) C_{\text{f}} \\ -i_{\text{a}} t_3 + i_{\text{a}} t_7 = (u_{\text{cfb}} - u_{\text{dc}}/4) C_{\text{f}} \end{cases} \tag{8}$$

For simplicity:

$$\begin{cases} T_1 = t_{\text{A}} \\ -(u_{\text{cd1}} - u_{\text{cd2}}) C_{\text{d}} / i_{\text{a}} = t_{\text{C}} \\ (u_{\text{cfa}} - u_{\text{dc}}/4) C_{\text{f}} / i_{\text{a}} = t_{\text{D}} \\ (u_{\text{cfb}} - u_{\text{dc}}/4) C_{\text{f}} / i_{\text{a}} = t_{\text{E}} \end{cases} \tag{9}$$

There are four variables t_1, t_3, t_5, and t_7 in Eq. (8), which are written as a vector equation with vector $\boldsymbol{X}$ as an unknown element:

$$\boldsymbol{AX} = \boldsymbol{b} \tag{10}$$

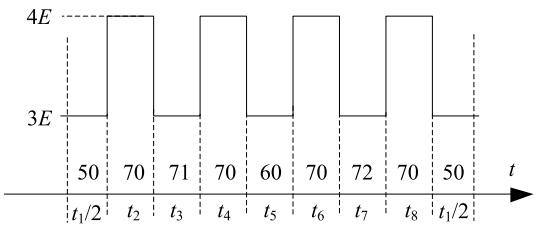


Fig. 6 Switching vectors when $\boldsymbol{V}^*(n)$ is in interval 8

where:

$$\boldsymbol{A}=\begin{bmatrix}1&1&1&1\\1&0&0&-1\\1&0&-1&0\\0&-1&0&1\end{bmatrix},\ \boldsymbol{X}=\begin{bmatrix}t_1\\t_3\\t_5\\t_7\end{bmatrix},\ \boldsymbol{b}=\begin{bmatrix}t_{\mathrm{A}}\\t_{\mathrm{C}}\\t_{\mathrm{D}}\\t_{\mathrm{E}}\end{bmatrix} \tag{11}$$

It is found that the rank of matrix $\boldsymbol{A}$ and the augmented matrix $\boldsymbol{A}|\boldsymbol{b}$ satisfy $\mathrm{R}(\boldsymbol{A})=\mathrm{R}(\boldsymbol{A}|\boldsymbol{b})$. Equation (10) has a unique solution, which is:

$$\begin{cases}t_1=(t_{\mathrm{A}}+2t_{\mathrm{C}}+t_{\mathrm{D}}+t_{\mathrm{E}})/4\\t_3=(t_{\mathrm{A}}-2t_{\mathrm{C}}+t_{\mathrm{D}}-3t_{\mathrm{E}})/4\\t_5=(t_{\mathrm{A}}+2t_{\mathrm{C}}-3t_{\mathrm{D}}+t_{\mathrm{E}})/4\\t_7=(t_{\mathrm{A}}-2t_{\mathrm{C}}+t_{\mathrm{D}}+t_{\mathrm{E}})/4\end{cases} \tag{12}$$

If three or fewer switching vectors corresponding to $\boldsymbol{V}_{\mathrm{low}}$ are used, then $\mathrm{R}(\boldsymbol{A})<\mathrm{R}(\boldsymbol{A}|\boldsymbol{b})$. There is no solution to the vector equation, which indicates that the decoupling cannot be controlled. In order to control the decoupling, four switching vectors 50, 71, 60, and 72 must be involved in $\boldsymbol{V}_{\mathrm{low}}$.

According to the action time of the switching vectors corresponding to $\boldsymbol{V}_{\mathrm{low}}$ and $\boldsymbol{V}_{\mathrm{high}}$, it is possible to derive the sequence of the switching vectors, as shown in Fig. 6. Among them, the first switching vector agrees with the last, where their action time is $t_1/2$. Thus, it is possible to connect with the next control cycle. Switching vector 70 is divided into four pulses by 60, 50, 71, and 72. The action time of each switching vector is $t_i(i=1,2,3,\ldots,8)$. To make the action times of the switching vectors uniform, let $t_2=t_4=t_6=t_8=t_{\mathrm{B}}/4$. In this control cycle, the series switches of the inverter do not act, and the non-series switches turn on and off only once.

When $\boldsymbol{V}^*(n)$ is located in interval 1, 4 or 5, the solution for the action time of switching vectors is similar.

(2) $\boldsymbol{V}^*$(n) in interval 2, 3, 6, or 7

When $\boldsymbol{V}^*(n)$ is located in interval 7, $\boldsymbol{V}_{\mathrm{low}}$ and $\boldsymbol{V}_{\mathrm{high}}$ correspond to $\boldsymbol{V}^{\mathbf{2}}$ and $\boldsymbol{V}^{\mathbf{3}}$, respectively. $\boldsymbol{V}_{\mathrm{low}}$ corresponds to the switching vectors 52, 62, 61, and 51, and their action times are t_1, t_3, t_5, and t_7, respectively. This satisfies the formula $t_1+t_3+t_5+t_7=T_1$. $\boldsymbol{V}_{\mathrm{high}}$ corresponds to the switching vectors 72, 60, 71, and 50, and their action times are t_2, t_4, t_6, and t_8, respectively. This satisfies the formula $t_2+t_4+t_6+t_8=T_2$.

According to the control method of the NPP and the FCV Eq. (13) can be obtained as follows:

$$\begin{cases}t_1+t_3+t_5+t_7=t_{\mathrm{A}}\\t_2+t_4+t_6+t_8=t_{\mathrm{B}}\\-t_3+t_7+t_8-t_2=t_{\mathrm{C}}\\-t_3-t_4-t_5+t_7+t_8+t_1=t_{\mathrm{D}}\\t_3-t_5-t_6-t_7+t_1+t_2=t_{\mathrm{E}}\end{cases} \tag{13}$$

Equation (13) is turned into a vector equation with vector $\boldsymbol{Y}$ as an unknown element.

$$\boldsymbol{CY}=\boldsymbol{d} \tag{14}$$

where:

$$\begin{cases}\boldsymbol{C}=\begin{bmatrix}1&0&1&0&1&0&1&0\\0&1&0&1&0&1&0&1\\0&-1&-1&0&0&0&1&1\\1&0&-1&-1&-1&0&1&1\\1&1&1&0&-1&-1&-1&0\end{bmatrix}\\ \boldsymbol{Y}=\begin{bmatrix}t_1\\t_2\\t_3\\t_4\\t_5\\t_6\\t_7\\t_8\end{bmatrix},\boldsymbol{d}=\begin{bmatrix}t_{\mathrm{A}}\\t_{\mathrm{B}}\\t_{\mathrm{C}}\\t_{\mathrm{D}}\\t_{\mathrm{E}}\end{bmatrix}\end{cases} \tag{15}$$

It can be found that $\mathrm{R}(\boldsymbol{C})=\mathrm{R}(\boldsymbol{C}|\boldsymbol{d})<8$. There are infinite solutions for Eq. (14). A group of solutions is as follows:

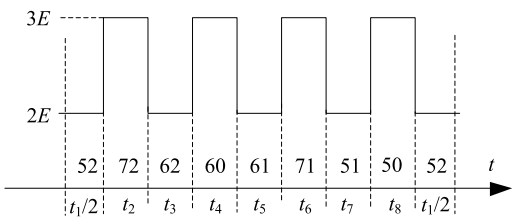


Fig. 7 Switching vector sequences of $\boldsymbol{V}^*(n)$ in interval 7

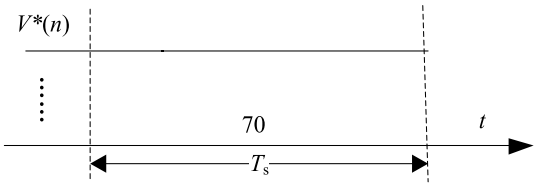


Fig. 8 Switching vector diagram when $\boldsymbol{V}^*(n)=\boldsymbol{V}^{\mathbf{4}}$

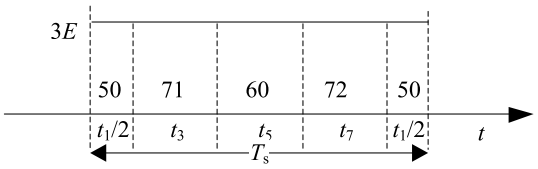


Fig. 9 Switching vector diagram when $\boldsymbol{V}^*(n)=\boldsymbol{V}^{\mathbf{3}}$

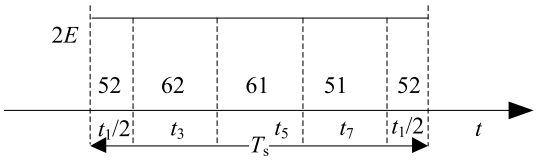


Fig. 10 Switching vector diagram when $\boldsymbol{V}^*(n)=\boldsymbol{V}^{\mathbf{2}}$

In Eq. (16), the absolute values of the coefficients of t_C are all 1/2, and those of t_D and t_E are all 1/4. This means that the action time of the switching vectors can be applied to more working conditions. It should be noted that this group of solutions cannot make the NPP or the FCV up to the maximum regulation capability under any working condition. However, it can ensure that the action time of each switching vector is uniform in a control cycle. The series arrangements of switching vectors 52, 72, and 62; 62, 60, and 61; 61, 71, and 51; and 51, 50, and 52 aim to reduce the switching times. Figure 7 shows the sequence of the switching vectors.

When $\boldsymbol{V}^*(n)$ is located in interval 2, 3, or 6, the solution for the action times of switching vectors is almost the same.

3.3.2 $\boldsymbol{V}^*(n)$ consisting of a single voltage vector

For the sake of simplicity, when $\boldsymbol{V}^*(n)$ consists of a single fundamental voltage vector, the selection of the switching vectors refers to the following three cases.

When $\boldsymbol{V}^*(n)=\boldsymbol{V}^{\mathbf{4}}$, the action time of switching vector 70 is T_s, as shown in Fig. 8.

When $\boldsymbol{V}^*(n)=\boldsymbol{V}^{-\mathbf{4}}$, the situation is similar.

When $\boldsymbol{V}^*(n)=\boldsymbol{V}^{\mathbf{3}}$, the action time can be considered to be $t_2=t_4=t_6=t_8=0$ in interval 8, while the others remain unchanged. At this time, the NPP and the FCV can be decoupled, as shown in Fig. 9.

When $\boldsymbol{V}^*(n)=\boldsymbol{V}^{-\mathbf{3}}$, the situation is similar.

When $\boldsymbol{V}^*(n)=\boldsymbol{V}^{\mathbf{2}}$, the action times of the switching vectors can be regarded as $t_2=t_4=t_6=t_8=0$ and $t_1=t_3=t_5=t_7=T_s/4$ in interval 7, while the rest remain unchanged. At this time, the variables cannot be decoupled. However, during this control cycle, the average neutral-point current and the average floating capacitor current are 0. This does not result in deterioration in the NPP or the FCV as shown in Fig. 10.

Table 5 Switching process in interval 8

Process	V5→V7	V7→V6	V6→V7	V7→V5
Bridge arm a				
Turn on	S_{a7}	S_{a9}	S_{a8}	S_{a10}
Turn off	S_{a10}	S_{a8}	S_{a9}	S_{a7}
Process	V0→V1	V0→V1	V0→V1	V0→V1
Bridge arm b				
Turn on	S_{b8}	S_{b8}	S_{b8}	S_{b8}
Turn off	S_{b9}	S_{b9}	S_{b9}	S_{b9}

$$\begin{cases} t_1=(t_A+2t_C+t_D+t_E)/4 \\ t_2=(t_B-2t_C+t_D-t_E)/4 \\ t_3=(t_A-2t_C-t_D+t_E)/4 \\ t_4=(t_B+2t_C-t_D+t_E)/4 \\ t_5=(t_A+2t_C-t_D-t_E)/4 \\ t_6=(t_B-2t_C+t_D-t_E)/4 \\ t_7=(t_A-2t_C+t_D-t_E)/4 \\ t_8=(t_B+2t_C-t_D+t_E)/4 \end{cases} \tag{16}$$

When $\boldsymbol{V}^*(n)=\boldsymbol{V}^{\mathbf{1}}$, $\boldsymbol{V}^{\mathbf{0}}$, $\boldsymbol{V}^{-\mathbf{1}}$, or $\boldsymbol{V}^{-\mathbf{2}}$, the situation is similar.

The sequence and action time of switching vectors in each interval are shown in the Appendix.

3.3.3 Analysis of the switching times

Interval 8 is taken as an example to analyze the actions of the switches. The sequence of the switching vectors in interval 8 is shown in Fig. 6. The switching process of the switching states of bridge arm a is V5 → V7 → V6 → V7 → V5. The switching process of the switching states of bridge arm b is V0 → V1 → V0 → V2 → V0. The non-series switches only turn on and turn off once in a control cycle, as shown in Table 5.

The switching times of the non-series switches when $\boldsymbol{V}^*(n)$ is in the other intervals are similar. In the conventional phase-shifted pulse width modulation, the non-series switches turn on and off once in a control cycle. In addition, the series switches only act when the modulation wave crosses zero both in the proposed modulation and in the conventional phase-shifted pulse width modulation. Thus, the losses of the proposed modulation and conventional phase-shifted pulse width modulation are almost the same.

4 Algorithm flow

The procedures of the proposed 5L-ANPC H-bridge inverter SVPWM include.

Determine the interval in which $\boldsymbol{V}^*(n)$ is located.

Calculate the action time of the fundamental voltage vectors that are combined into $\boldsymbol{V}^*(n)$.

Determine the switching vectors and their output sequence in a control cycle based on the constraints of the switching vectors and the minimum common-mode voltage.

Calculate the action time of each switching vector according to the action time of the fundamental voltage vectors and the deviation in the NPP and the FCV. If the calculated action time is less than the minimum pulse width, the maximum of $|t_C|$, $|t_D|$, and $|t_E|$ is divided by 2 for recalculation. If the calculated results still cannot meet the minimum pulse width limit, repeat the above process.

Send the generated pulses to the inverter according to the sequence and action time of the switching vectors in a control cycle.

Table 6 HIL real-time simulation experimental parameters

Parameter	Value	Parameter	Value
DC link voltage u_{dc}	10 kV	Load inductance L	11.34 mH
Output frequency f	20 Hz	Load resistance R	9.68 Ω
C_{fa},C_{fb}	2.5 mF	Modulation ratio m	0.85
T_s	1 ms	C_{d1},C_{d2}	1.5 mF

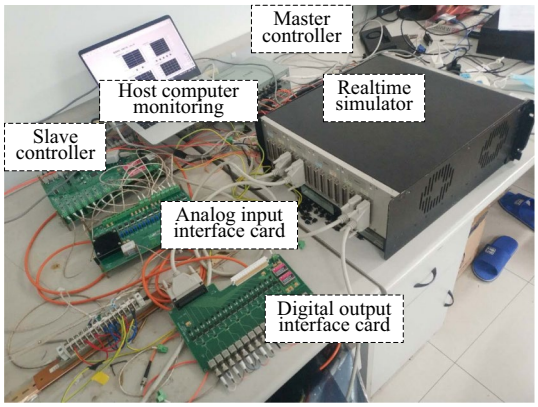


Fig. 11 Real-time simulation experimental platform

5 HIL verification

To verify the SVPWM of the 5L-ANPC H-bridge inverter proposed in this paper, a HIL real-time simulation experiment of the system has been carried out. The parameters for the real-time simulation experiment are listed in Table 6.

In terms of the proposed technique, an offline simulation may not fully reveal all of the features. In addition, the design of a system prototype and hardware experiments are expensive and time-consuming due to their high-power and high-voltage ratings. Therefore, the hardware-in-the-loop method provides an effective method for verifying the control strategy and converter performance due to its low cost, low risk, high flexibility, and fast implementation [21]. A 5L-ANPC H-bridge inverter HIL real-time simulation system was built in the laboratory. It includes a master controller, a slave controller, an analog output interface card, a digital input interface card, a simulator, and a host computer for monitoring.

Verification of the proposed control algorithm is based on the platform in Fig. 11. The master controller receives feedback analog signals from the real-time simulator via the analog output interface card. Then, it sends the reference signals to the slave controller. After that, PWM signals are produced in the slave controller. These PWM pulses are received by the model simulated in the real-time digital simulator (RTDS) via the digital input interface card. With the 5L-ANPC H-bridge model running in the RTDS at a time step of 5 μs, the system voltage and current are measured

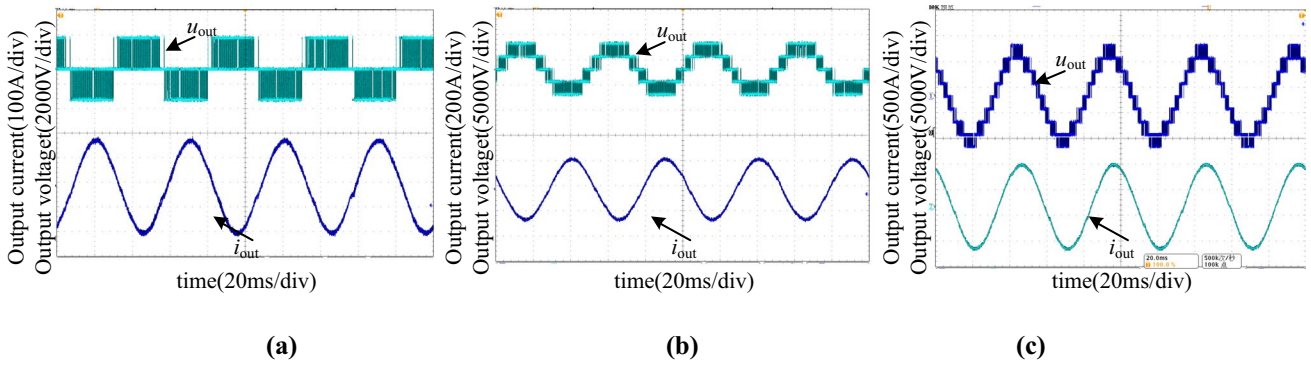


Fig. 12 Output current and voltage waveforms: **a** $m=0.2$; **b** $m=0.5$; **c** $m=0.85$

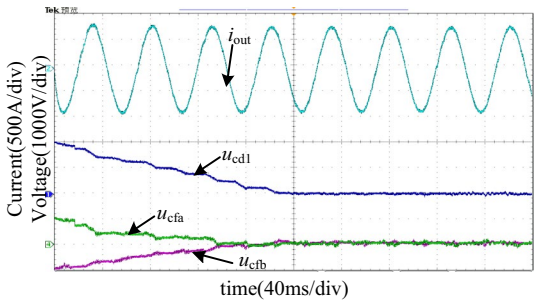


Fig. 13 NPP and FCV waveforms

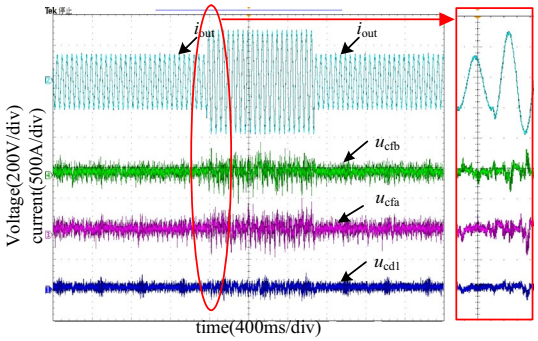


Fig. 14 Waveforms when the load changes

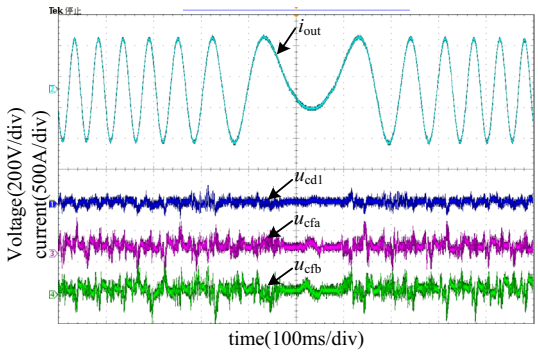


Fig. 15 Waveforms when the frequency varies

and transmitted through the A/D conversion interface card to the slave controller and the host computer. Real-time simulation experiment waveforms are shown in Figs. 12, 13, 14, 15, 16 and 17.

Output current and voltage waveforms of the 5L-ANPC H-bridge inverter can be seen in Fig. 12. These results show the proposed SVPWM algorithm to be correct.

When the voltage difference between C_{d1} and C_{d2} is 4 kV, the FCV of bridge arm a is 1 kV higher, and the FCV of bridge arm b is 1 kV lower. In this case, the waveforms are shown in Fig. 13. Since $u_{Cd1}+u_{Cd2}=10$ kV, only u_{Cd1} is shown in Fig. 13. These results show that both the NPP and the FCV reached a balance within 0.2 s. These results show that the proposed control strategy can be effectively used for the decoupling control of the NPP and the FCV. Thus, the proposed strategy is both feasible and useful.

Figure 14 shows waveforms when the load dynamically changes. It can be seen that the NPP and the FCV remain stable when the load changes. When the load current increases, the amplitude of the fluctuations of the NPP and the FCV increase slightly but stably.

When the output frequency f varies from $+20$ to -20 Hz, the output current and capacitor voltages are shown in Fig. 15. These results show that both the NPP and the FCV are balanced and that the output current is smooth when the frequency varies.

The common-mode voltage of the conventional phase-shifted pulse width modulation and the proposed modulation are shown in Fig. 16. The maximum common-mode voltage of the conventional phase-shifted pulse width modulation is 5000 V. Meanwhile, the maximum common-mode voltage

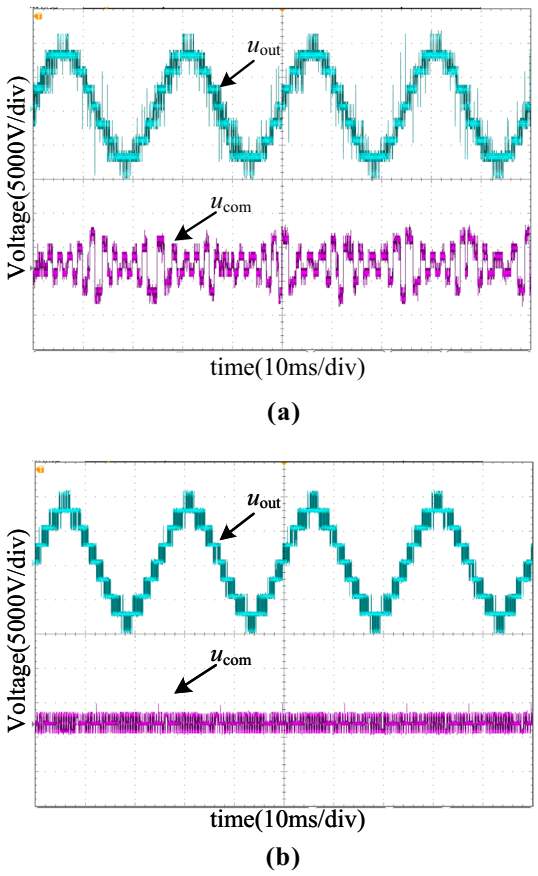


Fig. 16 Common-mode voltage waveforms: **a** conventional modulation; **b** proposed modulation

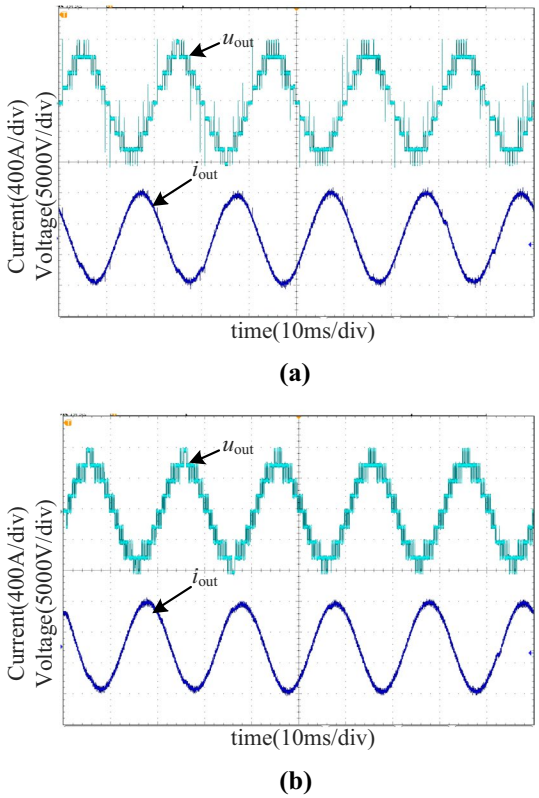


Fig. 17 Output current and output voltage waveforms: **a** conventional modulation; **b** proposed modulation

of the proposed modulation is within 1250 V. The proposed modulation has a lower common-mode voltage.

Experimental waveforms of the proposed modulation and the conventional phase-shifted pulse width modulation are provided in Fig. 17, where the voltage THD values are 17.5% and 17.84%. The proposed modulation has a lower voltage THD than the conventional phase-shifted pulse width modulation.

6 Conclusion

This paper proposes a new SVPWM for the 5L-ANPC H-bridge inverter. Twenty-eight available switching vectors are obtained based on the constraints of the switching and the minimized common-mode voltage. The fundamental voltage vectors are selected according to the expected output voltage. The action time of the switching vectors is calculated based on the action time of the fundamental voltage vectors as well as the deviations of the neutral point potential and the floating capacitor voltage. The sequence of the switching vectors in a control cycle is determined by the principle of the minimized switching times. Hardware-in-loop real-time simulation experimental results show that the control of the neutral point potential and the floating capacitor voltage can be decoupled with the proposed SVPWM algorithm and that the inverter has good dynamic performance.

Appendix

See Tables 7 and 8.

Acknowledgements This work was supported by the National Natural Science Foundation of China (51907200) and the Natural Science Foundation of Hubei Province of China (2019CFB249).

Declarations

Conflict of interest The authors declared that they have no conflicts of interest to this work.

Table 7 Action times of the switching vectors in each vector interval

Action time	Vector interval 8	Vector interval 7	Vector interval 6	Vector interval 5
t_1	$(t_A+2t_C+t_D+t_E)/4$	$(t_A+2t_C+t_D+t_E)/4$	$(t_A-2t_C+t_D-t_E)/4$	$t_A/4$
t_2	$t_B/4$	$(t_B-2t_C+t_D-t_E)/4$	$(t_B-2t_C+t_D+t_E)/4$	$(t_B-2t_C+3t_D-t_E)/4$
t_3	$(t_A-2t_C+t_D-3t_E)/4$	$(t_A-2t_C-t_D+t_E)/4$	$(t_A+2t_C-t_D+t_E)/4$	$t_A/4$
t_4	$t_B/4$	$(t_B+2t_C-t_D+t_E)/4$	$(t_B+2t_C-t_D+t_E)/4$	$(t_B-2t_C-t_D-t_E)/4$
t_5	$(t_A+2t_C-3t_D+t_E)/4$	$(t_A+2t_C-t_D-t_E)/4$	$(t_A-2t_C+t_D-t_E)/4$	$t_A/4$
t_6	$t_B/4$	$(t_B-2t_C+t_D-t_E)/4$	$(t_B-2t_C-t_D-t_E)/4$	$(t_B+2t_C-t_D-t_E)/4$
t_7	$(t_A-2t_C+t_D+t_E)/4$	$(t_A-2t_C+t_D-t_E)/4$	$(t_A+2t_C-t_D+t_E)/4$	$t_A/4$
t_8	$t_B/4$	$(t_B+2t_C-t_D+t_E)/4$	$(t_B+2t_C+t_D-t_E)/4$	$(t_B+2t_C-t_D+3t_E)/4$
Action time	Vector interval 1	Vector interval 2	Vector interval 3	Vector interval 4
t_1	$(t_A-2t_C-t_D-t_E)/4$	$(t_A-2t_C-t_D-t_E)/4$	$(t_A+2t_C+t_D-t_E)/4$	$t_A/4$
t_2	$t_B/4$	$(t_B+2t_C+t_D-t_E)/4$	$(t_B+2t_C-t_D-t_E)/4$	$(t_B+2t_C+t_D-3t_E)/4$
t_3	$(t_A+2t_C+3t_D-t_E)/4$	$(t_A+2t_C-t_D+t_E)/4$	$(t_A-2t_C-t_D+t_E)/4$	$t_A/4$
t_4	$t_B/4$	$(t_B-2t_C-t_D+t_E)/4$	$(t_B-2t_C-t_D+t_E)/4$	$(t_B+2t_C+t_D+t_E)/4$
t_5	$(t_A-2t_C-t_D+3t_E)/4$	$(t_A-2t_C+t_D+t_E)/4$	$(t_A+2t_C+t_D-t_E)/4$	$t_A/4$
t_6	$t_B/4$	$(t_B+2t_C+t_D-t_E)/4$	$(t_B+2t_C+t_D+t_E)/4$	$(t_B-2t_C+t_D+t_E)/4$
t_7	$(t_A+2t_C-t_D-t_E)/4$	$(t_A+2t_C+t_D-t_E)/4$	$(t_A-2t_C-t_D+t_E)/4$	$t_A/4$
t_8	$t_B/4$	$(t_B-2t_C-t_D+t_E)/4$	$(t_B-2t_C+t_D-t_E)/4$	$(t_B-2t_C-3t_D+t_E)/4$

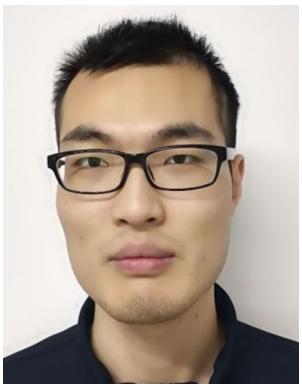
Table 8 Switching vector sequences in each vector interval

Action time	Vector interval							
	8	7	6	5	4	3	2	1
t_1	50	52	53	43	34	35	25	05
t_2	70	72	52	42	35	25	27	07
t_3	71	62	42	43	34	24	26	17
t_4	70	60	62	63	36	26	06	07
t_5	60	61	63	43	34	36	16	06
t_6	70	71	61	41	14	16	17	07
t_7	72	51	41	43	34	14	15	27
t_8	70	50	51	53	24	15	05	07

References

1. Sun, C., Ai, S., Hu, L.: The development of a 20MW PWM driver for advanced fifteen-phase propulsion induction motors. J. Power Electron. **15**(1), 149–159 (2015)
2. Marzoughi, A., Burgos, R., Boroyevich, D., Xue, Y.: Design and comparison of cascaded H-bridge, modular multilevel converter, and 5-L active neutral point clamped topologies for motor drive applications. IEEE Trans. Ind. Appl. **54**(2), 1404–1413 (2018)
3. Barbosa, P., Steimer, P., Steinke, J., Meysenc, L., Winkelnkemper, M., Celanovic, N.: Active neutral-point-clamped (ANPC) multilevel converter technology. In: Proceedings of European conference on power electronics and applications, CDROM, pp. 1–10 (2005)
4. Sun, D., Lin, B., Zhou, W.: An overview of open winding electric machine system topology and control technology. Trans. China Electrotech. Soc. **32**(4), 76–84 (2017)
5. Wang, D., Ma, W., Guo, Y., Liu, D., Chen, J.: Modelling of multiphase induction motor with non-sinusoidal supply. Trans. China Electrotech. Soc. **25**(2), 6–14 (2010)
6. Wang, K., Zheng, Z., Li, Y., Liu, K., Shang, J.: Neutral-point potential balancing of a five-level active neutral-point-clamped inverter. IEEE Trans. Ind. Electron. **60**(5), 1907–1918 (2013)
7. Yao, W., Hu, H., Lu, Z.: Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter. IEEE Trans. Power Electron. **23**(1), 45–51 (2008)
8. Wang, K., Xu, L., Zheng, Z., Li, Y.: Capacitor voltage balancing of a five-level ANPC converter using phase-shifted PWM. IEEE Trans. Power Electron. **30**(3), 1147–1156 (2015)
9. Wang, F., Dou, S., Fu, H., Zheng, D., Du, C., Liu, F.: An optimized decoupling control algorithm between flying capacitor voltage and neutral-point potential in ANPC-5L inverter. Proc. CSEE. **39**(4), 1150–1161 (2019)
10. Pulikanti, S.R., Agelidis, V.G.: Five-level active NPC converter topology: SHE-PWM control and operation principles. In: Proceedings of Australasian universities power engineering conference, Perth, WA, pp. 1–5 (2007)
11. Pulikanti, S.R., Agelidis, V.G.: Control of neutral point and flying capacitor voltages in five-level SHE-PWM controlled ANPC converter. In: Proceedings of 4th IEEE conference on industrial electronics and applications, Xi'an, pp. 172–177 (2009)

12. Pulikanti, S.R., Dahidah, M.S.A., Agelidis, V.G.: SHE-PWM switching strategies for active neutral point clamped multilevel converters. In: Proceedings of Australasian universities power engineering conference, Sydney, NSW, pp. 1–7 (2008)
13. Liu, Z., Wang, Y., Tan, G., Li, H., Zhang, Y.: A novel SVPWM algorithm for five-level active neutral-point-clamped converter. IEEE Trans. Power Electron. **31**(5), 3859–3866 (2016)
14. Chen, H., He, Y., Liu, J., Chen, X., Xiao, H., Zhi, W., Chen, R.: A novel hybrid SVPWM modulation algorithm for five level active neutral-point-clamped converter. In: Proceedings of IEEE applied power electronics conference and exposition, Anaheim, CA, USA, pp. 2494–2498 (2019)
15. Liu, Z., Xia, Z., Li, D., Wang, Y., Li, F.: An optimal model predictive control method for five-level active NPC inverter. IEEE Access. **8**, 221414–221423 (2020)
16. Wang, K., Zheng, Z., Xu, L., Li, Y.: An optimized carrier-based PWM method and voltage balancing control for five-level ANPC converters. IEEE Trans. Ind. Electron. **67**(11), 9120–9132 (2020)
17. Leon, J.I., Portillo, R., Vazquez, S., Padilla, J.J., Franquelo, L.G., Carrasco, J.M.: Simple unified approach to develop a time-domain modulation strategy for single-phase multilevel converters. IEEE Trans. Ind. Electron. **55**(9), 3239–3248 (2008)
18. Leon, J.I., et al.: Conventional space-vector modulation techniques versus the single-phase modulator for multilevel converters. IEEE Trans. Ind. Electron. **57**(7), 2473–2482 (2010)
19. Leon, J.I., Vazquez, S., Kouro, S., Franquelo, L.G., Carrasco, J.M., Rodriguez, J.: Unidimensional modulation technique for cascaded multilevel converters. IEEE Trans. Ind. Electron. **56**(8), 2981–2986 (2009)
20. Li, W., Ma, W., Wang, G., Lin, C., Nie, S., Guo, D.: A novel SVPWM method for single-phase cascaded NPC H-bridge inverter. Proc. CSEE. **34**(30), 5313–5319 (2014)
21. Burbank, J.L., Kasch, W., Ward, J.: Hardware-in-the-loop simulations. In: Hoboken, N.J. (ed.) An introduction to network modeling and simulation for the practicing engineer, 1st edn., pp. 114–142. Wiley (2011)



Linfei Jiang was born in Jiangsu, China, in 1992. He received his M.S. degree from the Military Transportation University, Tianjin, China, in 2017. His current research interests include power electronic topologies, high-voltage converters and motor drives.

Fei Xiao was born in Hubei, China, in 1977. He received his Ph.D. degree from Zhejiang University, Hangzhou, China, in 2012. His current research interests include renewable energy generation, the modeling and control of power electronics systems, and high-voltage large-capacity power electronics equipment.

Liangdeng Hu was born in Hunan, China, in 1986. He received his Ph.D. degree from the Naval University of Engineering, Wuhan, China, in 2015. His current research interests include high capacity power electronic transformations, high voltage auxiliary power supply designs, and digital active gate drive technology.

Yingjie Jia was born in Shandong, China, in 1990. He received his Ph.D. degree from the Naval University of Engineering, Wuhan, China, in 2020. His current research interests include the modeling and reliability of the multi-physics couplings of power semiconductor devices.