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ORIGINAL ARTICLE

Online monitoring of IGBT junction temperature based on V_{ce} measurement

Han Cao[1,2,3,4] · Puqi Ning[1,2,3,4] · Xiaoguang Chai[1,2,3,4] · Dan Zheng[1,2,4] · Yuhui Kang[1,2,4] · Xuhui Wen[1,2,3,4]

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Abstract

In this paper, an online junction temperature monitoring method based on the on-state voltage under high collector current density measurements for IGBT power modules is proposed. Unlike the conventional junction temperature monitoring method, the presented method can extract the junction temperature during operation without altering the modulation strategy or topology of the converter. The proposed method is verified by simulations and the JEDEC-51 standard recommended approach. To accurately extract the on-state voltage during operation, a measurement circuit that combines the advantages of both the active MOSFET clamp and the diode clamp is designed and tested. It has been shown to have good accuracy and a rapid response time. After the calibration results are obtained, the presented method is applied to a three-phase voltage source converter controlled by a closed-loop SVPWM modulation strategy.

Keywords IGBT modules · Online junction temperature monitoring · On-state voltage measurement circuit

Abbreviations

C_{OX}	Oxide capacitance (nF)
D_a	Ambipolar diffusivity (cm^2 /s)
J_C	Collector current density (A/cm^2)
k	Boltzmann constant (J/K)
K_T	Threshold voltage temperature coefficient (V/K)
L_a	Ambipolar diffusivity length (μm)
L_{CH}	Channel length (μm)
n_i	Intrinsic carrier concentration (cm^{-3})
p	Cell pitch (μm)
q	Unit charge (c)
S	Relative thermal sensitivity factor (%/℃).
T	Temperature (K)
T_0	Room temperature (K)
t_{d_off}	Turn-off delay time (ns)
μ_{ni}	Channel mobility (cm/s)
$V_{ce(LC)}$	On-state voltage under a low current (mV)
$V_{ce(HC)}$	On-state voltage under a high current (mV)
V_G	Gate–emitter voltage (V)
V_{TH}	Threshold voltage of an elemental MOSFET (V)
V_{TH0}	Threshold voltage at room temperature (V)
W_N	Drift region width of an IGBT (um)

✉ Puqi Ning
npq@mail.iee.ac.cn

[1] Key Laboratory of Power Electronics and Electric Drive, Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China

[2] Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China

[3] University of Chinese Academy of Sciences, Beijing, China

[4] Collaborative Innovation Center of Electric Vehicles in Beijing, Beijing, China

1 Introduction

Junction temperature is an important design and operation parameter. It is also a key factor in terms of lifetime estimation [1–3], reliability evaluation [4, 5], active thermal control [6–11] and over temperature protection [12] for semiconductor power devices. Junction temperature is also very important for power module [13, 14] and power converter [15] design. Power device lifetime estimation methods predict lifetime using evaluation models, where junction temperature is the most important indicator. Other than the lifetime prediction, power module reliability evaluation focuses on module failures caused by material degradation. Figure 1 illustrates a typical multilayer structure and the relative materials in IGBT modules. Most failures occur around the semiconductor chips due to the large difference coefficients of the thermal expansion between different layers, especially bond wires, semiconductor chips and solder

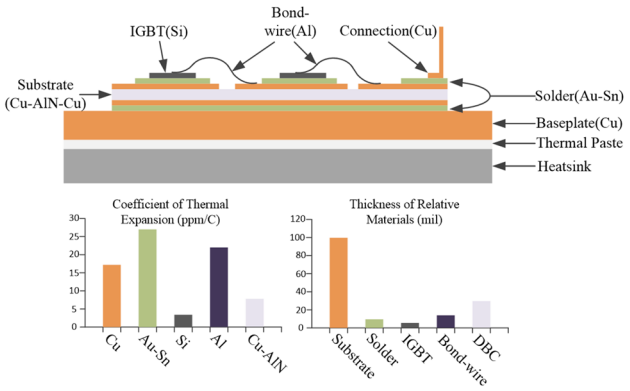

Fig. 1 Typical multilayers structure for IGBT modules

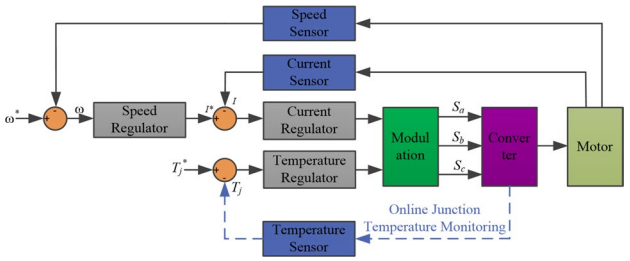

Fig. 2 Active thermal control implementation

joints, which are the inducements of bond-wire liftoff and solder joint degradation, respectively.

More importantly, for semiconductor devices, especially MOSFETs, special attention should be paid to the negative bias temperature instability (NBTI) issue [16, 17]. NBT stress-induced threshold voltage shifts for n-channel power VDMOSFETs are presented in [18]. Once n-channel devices are exposed to a negative gate bias and the temperature is evaluated at any stage of their operation, the related instabilities can actually be more serious than those found in p-channel devices. Hence, the junction temperature needs to be monitored synchronously and accurately to evaluate reliability. This is especially true for n-channel power devices.

A thermal analysis of power systems reveals that some of the power semiconductor devices in the same converter can be more stressed than others [19]. Consequently, it is necessary to modify the modulation strategy according to the junction temperature as shown in Fig. 2. In addition to conventional closed loop control strategies, an additional junction temperature loop is set as a feedback to regulate thermal stress by adjusting the switching frequency and current limit.

In [20], S. Yang defined three categories of junction temperature extraction methods: electro-thermal model based junction temperature estimation methods [21, 22], sensor-based junction temperature monitoring methods [23, 24] and temperature sensitive electrical parameters (TSEPs)-based methods [25–27]. C. Sintamarean estimated the junction temperature rise of an IGBT module using a power device losses model and a thermal impedance network in [21]. However, it does not take the materials degradation into account. An adaptive method to update the thermal impedance model was proposed to calibrate the error caused by aging effects [22]. Nevertheless, it is hard to extract an accurate thermal impedance network under different operation conditions. Therefore, an electro-thermal model-based method is not appropriate for online junction temperature monitoring.

Other commonly used approaches to monitor junction temperature are the sensor-based methods, which include physical and optical measurement methods. Optical methods, such as infrared cameras and optical fibers, have high measurement accuracy. However, they are prevented by power module packaging and dielectric gel. Physics-based junction temperature monitoring methods are widely used in commercial power modules. Thermal sensitive resistors and thermocouples are installed on the surface of a substrate, which is the nearest available location to chips. Due to the thermal impedance between the semiconductor chip and the substrate, there exists a non-negligible error between measured temperature and real junction temperature. Although thermal test chips (TTC) [23] can be applied to extract the online junction temperature by the polysilicon sensors set in the metallization layer of a semiconductor chip, it is only a local measurement and the peak of the chip temperature caused by the void of solder is hard to obtain. More importantly, sensors are installed through power loops which means special attentions need to be paid to insulation problems and electro-magnetic interference (EMI) problems.

Using the TSEPs of a chip is a feasible approach to monitor junction temperature accurately without modifying the active surface of a device. In [24], Z. Zhang presented a junction temperature monitoring method based on turn-off delay time t_{d_off} measurement, and applied it to a half-bridge invertor. To obtain t_{d_off} accurately, the turn-off gate resistor was enlarged to 300 Ω which increases the additional turn-off losses. H. Chen analyzed the temperature variation of threshold voltage V_{th} and proposed a junction temperature measurement method based on it in [25]. However, the chosen gate resistor is 265 kΩ to ensure the accuracy. More importantly, the threshold voltage is hard to measure during operation.

Z. Xu used short-circuit current I_{SC} as a TSEP and applied it to dc–dc and dc–ac converter applications in [26]. Although, it has good linearity, an additional pass-by IGBT is required to generate short-circuit conditions, which increases total power losses of a converter. In [27], D. Bergogne proposed a saturation current I_{sat} based IGBT junction temperature measurement method. The foremost problem is

that the saturation current rises exponentially with junction temperature increases. In addition, hundreds of milliamps of saturation currents are difficult to measure.

In [28], Y. Zhu used an on-state voltage drop under a low current as a TSEP and applied it to a H-bridge invertor. The foremost problem is that a very low measurement current can be easily interfered with. Moreover, an additional current source is required in parallel with the device under test. Each TSEP has its advantages and disadvantages in terms of sensitivity, linearity, complexity of additional circuits and possibility of online measurements. Among these assessment criteria, special attention should be paid to the sensitivity of the TSEPs. A method of comparing the accuracy of different TSEPs was proposed in [29] using the relative thermal sensitivity factor:

$$S = \frac{|s|}{|val\,\max|} \times 100(\%/^{\circ}C) \tag{1}$$

where s and val max are the temperature sensitive and maximum measured values of the TSEP, respectively. A comparisons of TSEPs for online temperature monitoring are listed in Table 1.

This paper aims at developing an accurate and compact online junction temperature monitoring method for IGBT power modules that are the most widely used in industry applications. On-state voltage at a high current is chosen as a TSEP due to its good linearity, freedom from converter normal operation interference, and measurement under the conduction state, which is extremely appropriate for over temperature protection applications. Existing $V_{ce(HC)}$-based IGBT junction temperature monitoring methods [30–33] are mostly empirical. They do not analyze the relationship between the on-state voltage drop $V_{ce(HC)}$, the collector current I_c, the gate driver voltage V_{ge} and the junction temperature T_j in principle. More importantly, these methods are mainly applied to thermal impedance tests under the steady state. They are seldom used in a converter under operating condition. Additionally, for high-power semiconductor devices with high blocking voltages, special attention need to be paid to the on-state voltage measurement circuits. Compared with the method proposed in [30], this paper presents a faster and more accurate on-state voltage measurement circuit. The relationships between the on-state voltage drop $V_{ce(HC)}$, the collector current Ic, the gate driver voltage V_{ge} and the junction temperature T_j are analyzed in principle and simulated in MATLAB. More importantly, the temperature monitoring method is verified under both offline and online conditions.

2 Sensitivity analysis of on-state voltage under a high current

In [34] and [35], a compact model that can be used to simulate the on-state characteristic of an IGBT consists of a PiN rectifier connected in series with a MOSFET operating in its linear region as shown in Fig. 3. The PiN rectifier part of the IGBT model can be simplified as a one-dimensional structure thanks to the uniform distribution of the current flowing through the N-region.

Table 1 Comparisons of TSEPs for temperature monitoring

TSEPs	Sensitive	Linearity
Short-circuit current I_{SC}	0.166/℃	Good Linearity
Saturation current I_{sat}	0.432/℃	Exponential
On-state voltage at low current $V_{ce(LC)}$	0.377/℃	Good Linearity
On-state voltage at high current $V_{ce(HC)}$	0.136/℃	Good Linearity
Turn-off delay time t_{d_off}	0.089/℃	Good Linearity
Complexity	Possibility	Reference
Additional pass-by IGBT	Inadequacy	[20]
Low current measurement equipment	Inadequacy	[21]
Voltage measurement equipment	Inadequacy	[22]
Voltage measurement equipment	Adequacy	[24]
Additional designed measurement circuit	Adequacy	[18]

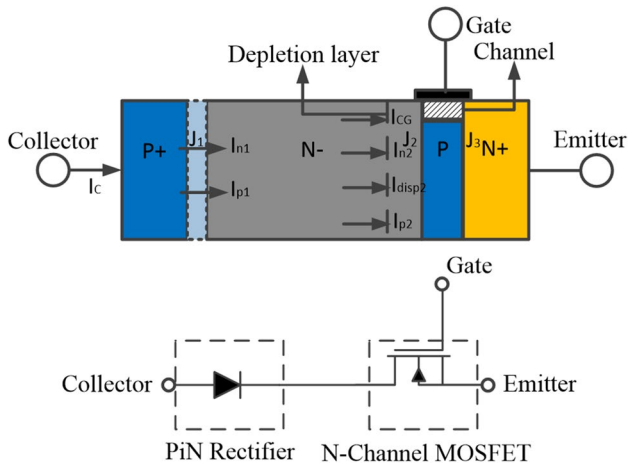

Fig. 3 IGBT on-state model implementation

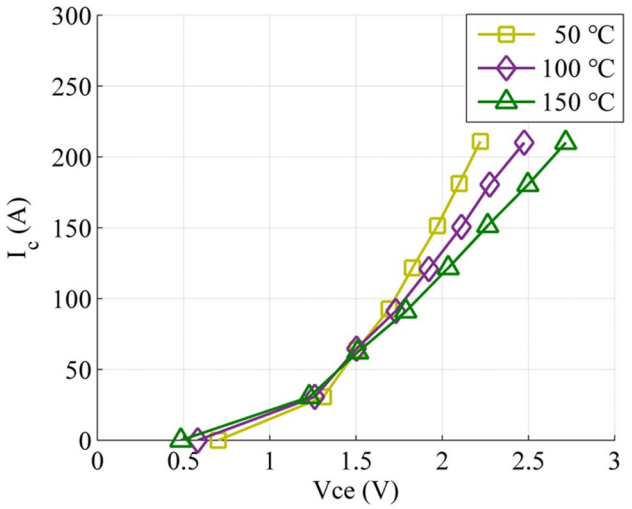

Fig. 4 Typical IGBT output characteristics with different junction temperatures

The IGBT on-state voltage consists of two parts: PiN rectifier part voltage and MOSFET part voltage, as can be seen in (2).

$$V_{\mathrm{ce(on)}} = \frac{2kT}{q}\ln\left[\frac{J_{\mathrm{C}}W_{\mathrm{N}}}{4qD_{\mathrm{a}}n_iF(W_{\mathrm{N}}/2L_{\mathrm{a}})}\right] + \frac{pL_{\mathrm{CH}}J_{\mathrm{C}}}{\mu_{\mathrm{ni}}C_{\mathrm{ox}}V_{\mathrm{G}} - V_{\mathrm{TH}}} \tag{2}$$

$$F(x) = \frac{x\tanh x}{\sqrt{1-0.25\tanh^4(x)}}e^{-qV_M/2kT} \tag{3}$$

where k is the Boltzmann constant, T is the junction temperature, q is the unit charge, J_{C} is the collector current density, W_{N} is drift region width of the IGBT, D_{a} is the ambipolar diffusivity, n_i is the intrinsic carriers concentration, L_{a} is the ambipolar diffusivity length, p is the cell pitch, L_{CH} is the channel length, μ_{ni} is the channel mobility, C_{ox} is the oxide capacitance, and V_{G} and V_{TH} are gate voltage and threshold voltage, respectively.

When the on-state collector current density is low, the first term in the above equation becomes dominant. In this regime of operation, the collector current increases exponentially with an increasing on-state voltage. When the collector current density is larger, the second term becomes significant, which adds a resistance in series with the PiN rectifier voltage drop [36]. Therefore, the knee voltage can be observed in output characteristics curves as depicted in Fig. 4.

Due to different manufacturing processes, it is extremely difficult to obtain accuracy values of the semiconductor parameters of an IGBT chip, such as the cell pitch p and the channel length L_{CH}. To analyze the sensitivity of the proposed TSEP, these unmeasurable parameters are listed hypothetically in Table 2.

For a certain IGBT chip, the cell pitch, channel length and oxide capacitance are constants, and the channel mobility and threshold voltage are temperature relative parameters and can be described in (4) and (5), respectively.

$$\mu_{rmni} = 1360\left(\frac{300}{T}\right)^{2.42} \tag{4}$$

$$V_{TH} = V_{TH0} - K_T(T - T_0) \tag{5}$$

The value of the threshold voltage V_{TH} decreases with an increase of the junction temperature due to changes of intrinsic carrier concentration. To extract K_{T} and V_{TH0}, the V_{TH} of a Starpower GD400FFT65P3H IGBT module is measured offline under different junction temperatures from 50 to 125 ℃. The results are illustrated in Fig. 5. The threshold voltage at room temperature and the slope of this linear fitting equation are 6.4 V and − 0.0242 V/℃, respectively.

With all of the above parameters and equations, the on-state voltage under a high current $V_{\mathrm{ce(HC)}}$ is calculated under different junction temperatures T and collector current densities J_{C} as shown in Fig. 6.

As illustrated in Fig. 6, the IGBT on-state voltage has a positive linear correlation with junction temperature under

Table 2 Simulation parameters

Parameters	Expression	Unit
Cell pitch p	7	μm
Channel length L_{CH}	1.5	μm
Channel mobility μ_{ni}	(3)	cm/s
Oxide capacitance C_{ox}	20	μF
Gate driver voltage V_{G}	15	V
Threshold voltage V_{TH}	(4)	V

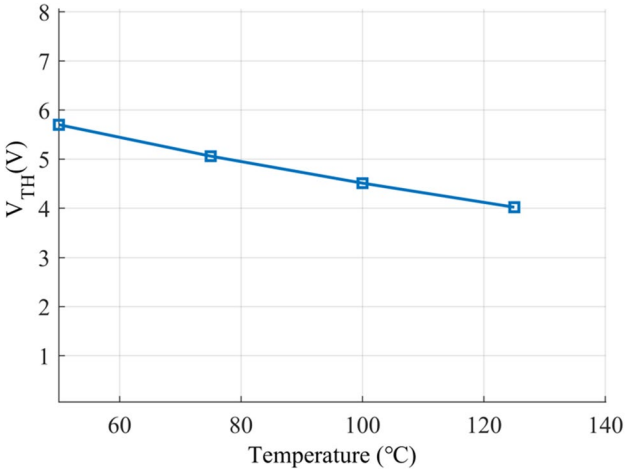

Fig. 5 Threshold voltage under different junction temperatures

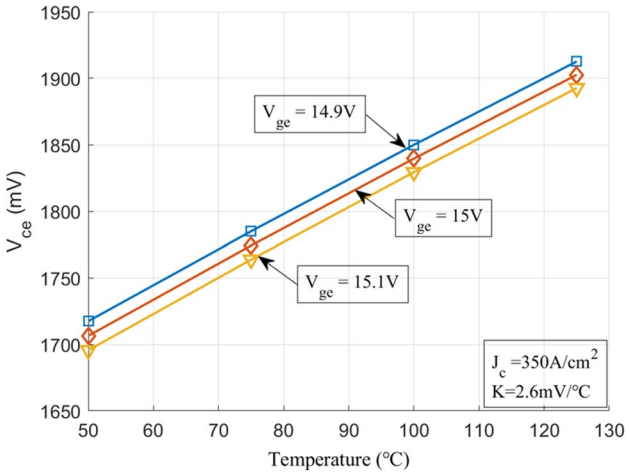

Fig. 7 On-state voltage under different junction temperatures and gate voltages

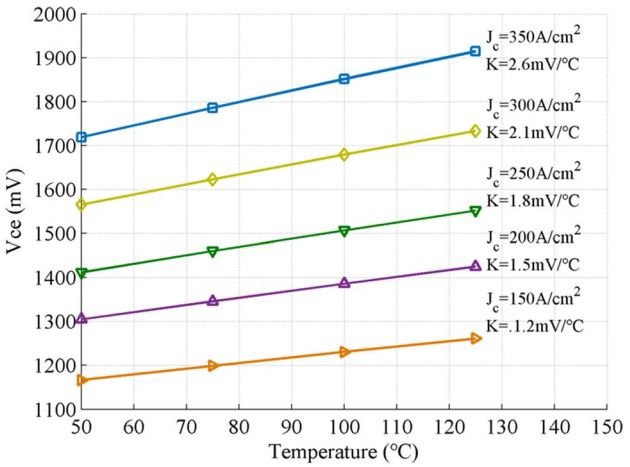

Fig. 6 On-state voltage under different junction temperatures and collector current densities

certain gate driver conditions and collector current densities. It should be noticed that sensitivity increases with the collector current density, which shows great potential in power electronics device junction temperature monitoring applications.

With the converter operating, both the power module and driver circuit are heated. Since the parasitic parameters in gate loop and components on driver circuit vary with junction temperature, the gate voltage experiences a tiny change after long operating time. Supposing the variation range of the gate voltage is ± 0.1 V, the on-state voltage under different junction temperatures can be seen in Fig. 7. The maximum voltage deviation is around 12 mV which leads to a measurement error of less than than 5℃.

3 Formatting *Vce* measurement method implementation

To monitor the junction temperature based on V_{ce} measurements, a simultaneously on-state voltage extraction circuit with a high measurement accuracy (Mv range), a high blocking capability (kV range) and a fast dynamic response (us range) are demanded. Unlike power device current measurement solutions, it is extremely difficult to obtain the on-state voltage directly using a conventional oscilloscope due to the limits of its measurement resolution. As an example, the blocking voltage is set to 800 V and a conventional 12-bit Tektronix MSO44 oscilloscope [37] is employed as measurement equipment. Consequently, the minimum significant measurement value corresponds to $800/2^{12} \approx 195$ mV, which is nearly one tenth of the on-state voltage of a typical IGBT. In this case, the voltage waveform captured by the oscilloscope is difficult to analyze, as shown in Fig. 8.

The three most commonly used on-state voltage measurement circuits are depicted in Fig. 9 [38], Fig. 10 [39] and Fig. 11 [40], respectively. The on-state voltage measurement circuit illustrated in Fig. 9 uses the active MOSFET *S1* to block DC link voltage during the DUT off-state. When the DUT is under the conducting state, the output of the measurement circuit can be calculated as (6). Due to the extremely low on-state resistance, the measurement value of output voltage $V_{o,1}$ is almost equal to the on-state voltage of the DUT.

$$V_{o,1} = \frac{R_1 V_{ce}}{R_1 + R_{S1}} \tag{6}$$

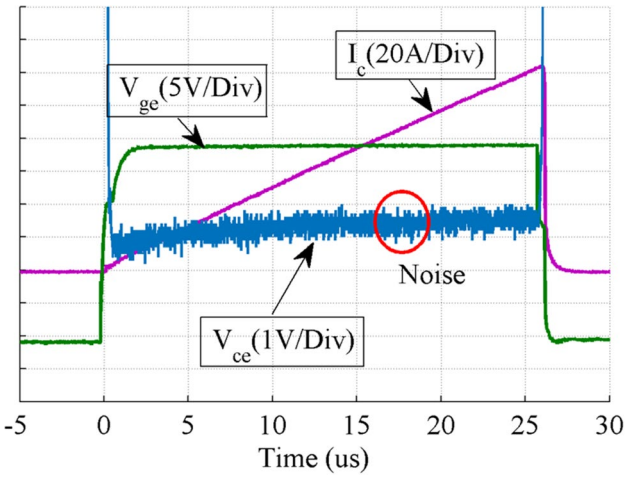

Fig. 8 Noise in the direct voltage measurement method

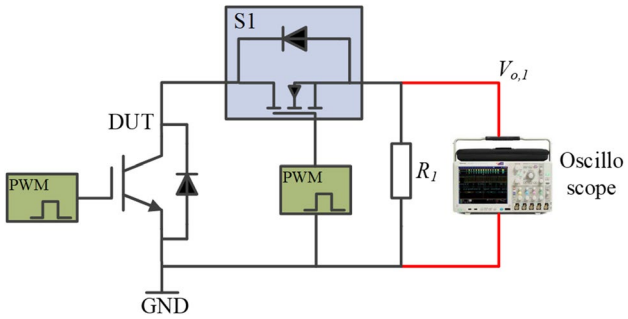

Fig. 9 On-state voltage measurement circuit based on an active MOSFET clamp

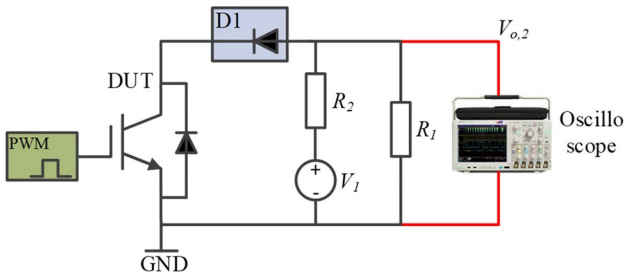

Fig. 10 On-state voltage measurement circuit based on a diode clamp

Regarding the transition between the on and off states, an active control strategy is adopted and applied to clamp MOSFET *S1*, which increases the complexity of this measurement circuit. More importantly, the clamp MOSFET should be selected as a power MOSFET and a complex gate driver circuit must be integrated into the on-state voltage measurement circuit.

As shown in Fig. 10, a high-voltage diode *D1* is chosen as the clamp component. During the DUT off-state, the clamp diode *D1* blocks the DC link voltage and protects the measurement circuit. When the DUT is conducting, the measurement value is shown as (7).

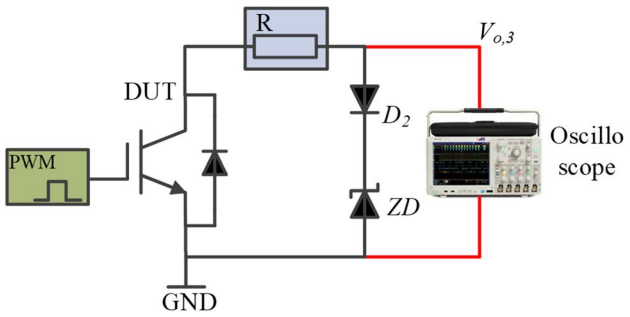

Fig. 11 On-state voltage measurement circuit based on an R-D clamp

$$V_{o,2} = V_{ce} + V_{D1} \tag{7}$$

where V_{D1} is the on-state voltage of the clamp diode, which is relevant to the diode junction temperature and the forward bias current generate by V_1. When compared to a clamp MOSFET, this clamp circuit is more compact. However, the output value involves a temperature dependent variable V_{D1} that makes it difficult to extract the real on-state voltage of the DUT.

Another approach to blocking DC link voltage is the use of an R–D clamp circuit, as depicted in Fig. 11. A high-voltage resistor accompanied by a zener diode *ZD* is employed to clamp the voltage during the DUT off-state, and *D2* is used to prevent discharge of the Zener diode junction capacitance. However, this measurement circuit cannot be used under high frequency conditions due to the frequency limitation of the zener diode ZD.

In [41], S. Beczkowski presented an IGBT on-state voltage measurement circuit (OVMC). However, it cannot work well especially during IGBT switching transients. Firstly, the bias current I_{Bias} is generated by a voltage regulator. During the IGBT off-state, the DC voltage is blocked by D_1 and D_2 equally. Hence, the input voltage of the amplifier exceeds its power supply voltage which destroys the amplifier. Second, during the IGBT off-state, the output of the voltage regulator induces invalid measurement data, which reduces the resolution of the measurement circuit.

To measure the on-state voltage of IGBT modules simultaneously and accurately, a clamp diode-based voltage measurement circuit is proposed as shown in Fig. 12 and Fig. 13.

D_1, D_2 and D_3 are fast recovery diodes (MA4P7470F-1072 T) with an 800 V blocking voltage. D_1 and D_2 are used to block the DC link voltage. To eliminate the measurement error, D_2 (which is the same as D_1) is set in series with D_1 and the output of amplifier OPA320 can be described as (8). The anti-parallel diode D_3 is set to

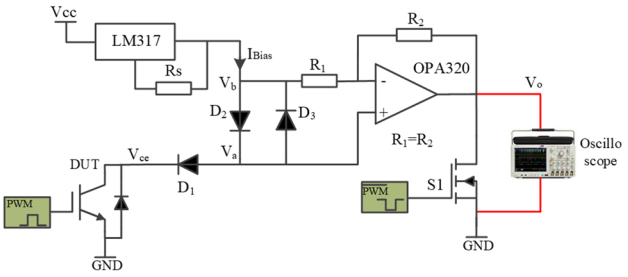

Fig. 12 Proposed on-state voltage measurement circuit

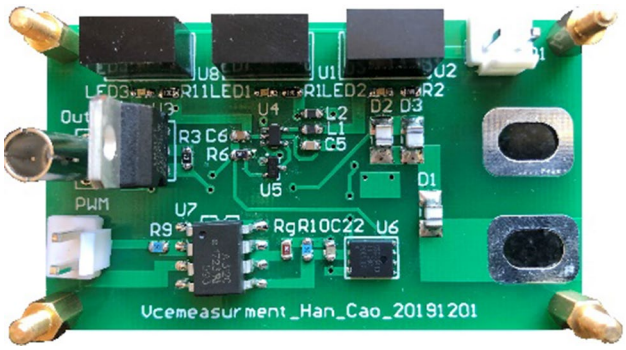

Fig. 13 Prototype of the proposed circuit

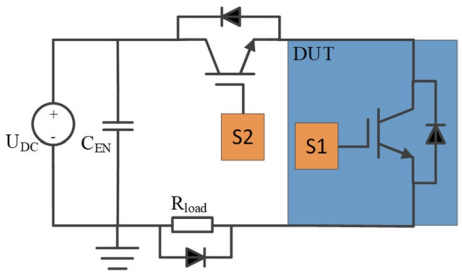

Fig. 14 Circuit for validating the accuracy of the proposed circuit

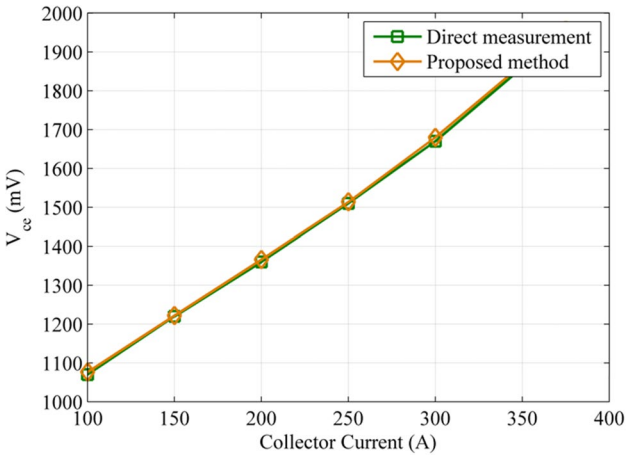

Fig. 15 Comparison of direct measurement and the proposed circuit measurement results

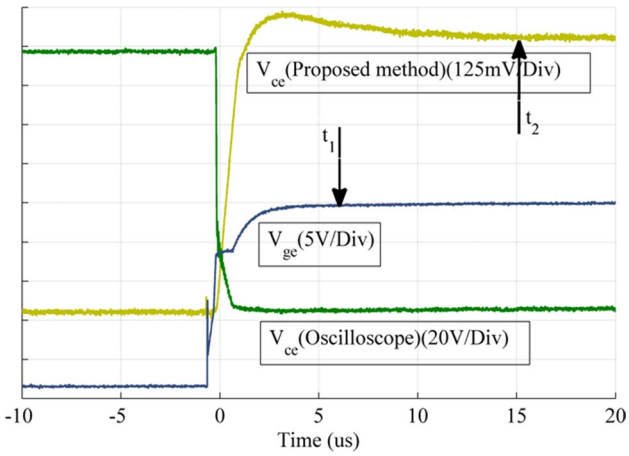

Fig. 16 Response time of the proposed measurement circuit

eliminate the reverse voltage of D_2 to protect the amplifier. A 3-Terminal adjustable voltage regulator LM317 is chosen to generate the bias current for D_1 and D_2. A signal MOSFET CSD16413Q5A is adopt to filter invalid measurement data during the DUT off-state and to provide a discharge loop for I_{Bias}.

$$V_{\text{o}} = V_{\text{ce}} = 2V_{\text{a}} - V_{\text{b}}. \tag{8}$$

To validate the accuracy of the proposed on-state voltage measurement circuit, a single-pulse test platform was built as shown in Fig. 14. DUT *S1* is in the conducting state, while *S2* is driven by a single pulse. During the off-state of *S2*, the DC link voltage is blocked only by *S2*, and the voltage across *S1* is almost 0. Hence, the on-state voltage of the DUT can be directly detected by an oscilloscope and the results are depicted in Fig. 15.

Apart from measurement accuracy, another indicator that needs to be concentrated on is the response time of the measurement circuit. As shown in Fig. 16, due to a rise of the gate voltage, the IGBT module is operated from its linear region to its saturation region. Consequently, there exists a voltage overshoot at the beginning of the measurement circuit operation, and it can be restrained by increasing the value of the driver resistance of *S1*. The results are illustrated in Fig. 17.

The response time can be defined as the delay time between the effective input and output of the measurement circuit. At the moment t_1, the gate voltage rises to its positive steady-state value. Because the voltage overshoot occurred in the turn-on transient, the on-state voltage measured by the proposed method is not stable until t_2. Hence, the response time can be described as the time interval between t_1 and t_2. When compared to the switching period under PWM

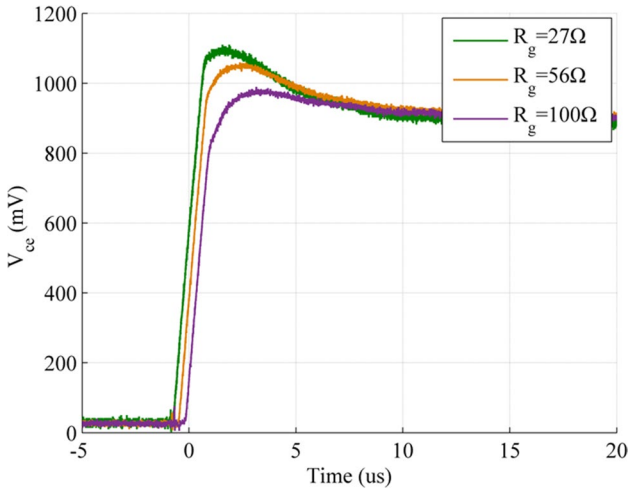

Fig. 17 Voltage overshoot with different driver resistances of S_1

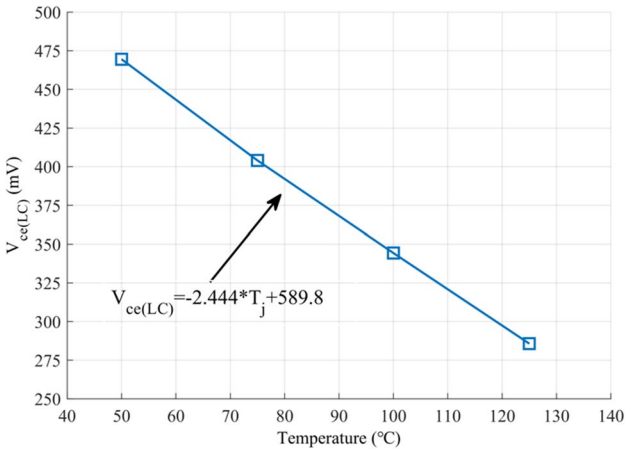

Fig. 18 Calibration results of on-state voltage under a low current density

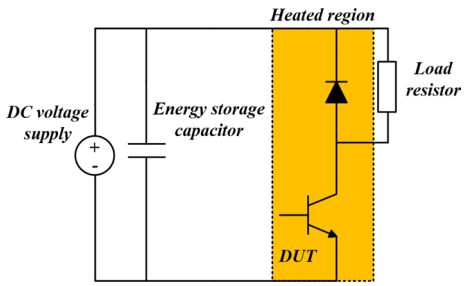

Fig. 19 Calibration circuit of on-state voltage under a high current density

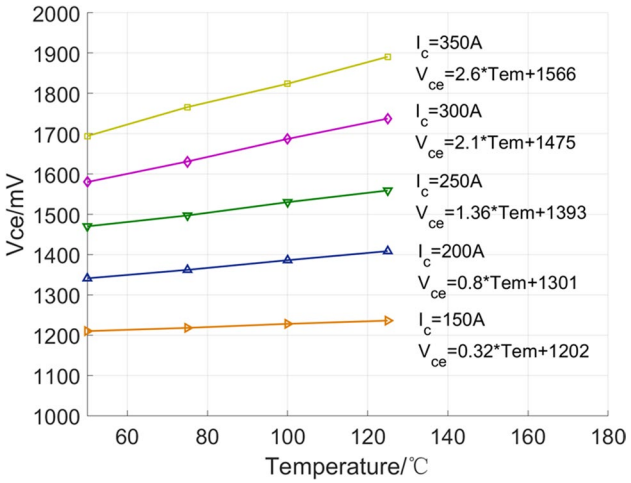

Fig. 20 Calibration results of on-state voltage under a high current density

modulation, the on-state voltage measurement circuit has a fast response speed.

4 Offline verification using V_{ce} under a low current density

Thanks to good linearity and temperature sensitivity, the on-state voltage under a low collector current density $V_{ce(LC)}$ is recommended for an IGBT module thermal impedance test by the Electronic Industries Association (EIA) and Joint Electron Device Engineering Council (JEDEC). To verify the accuracy of the presented method, the junction temperatures monitored by measuring the on-state voltage under a low current density $V_{ce(LC)}$ and a high current density $V_{ce(HC)}$ are compared and analyzed.

4.1 Calibration implementation

Before using a TSEP, it is necessary to make a preliminary calibration to find the relationship between the TSEP and the junction temperature. The on-state voltage under a low current density $V_{ce(LC)}$ is related to the gate voltage, collector current and junction temperature. For a GD400FFT65P3H IGBT module, the $V_{ce(LC)}$ values with different junction temperatures are illustrated as Fig. 18. The gate voltage and injection collector current are 15 V and 145 mA, respectively.

Similarly, the on-state voltage under a high current density $V_{ce(HC)}$ is a function of the gate voltage, collector current and junction temperature. The calibration circuit for $V_{ce(HC)}$ is shown as Fig. 19. To avoid the measurement error caused by the chip self-heating effect, a single pulse generated by a pulse generator based on a Schmitt trigger and a 555 Timer

within 10 μs is used to drive the DUT. The $V_{ce(HC)}$ with different collector currents are shown in Fig. 20. The gate voltage is chosen as 15 V, which is the same as the value used in the $V_{ce(LC)}$ calibration experiment.

4.2 Experimental verification

To verify the measurement accuracy of the presented method, the junction temperature monitoring results using $V_{ce(HC)}$ and $V_{ce(LC)}$ are compared, and the test circuit is illustrated in Fig. 21. First, a constant heating current I_H is applied to the DUT to heat up the device until the thermal steady state is reached. Since the DUT is in contact with the heat sink, the heating time can be selected at around 100 s in most cases.

When the thermal steady state is reached, a 145 mA measurement current I_M is injected into the device while the heating current I_H is cut off. By a comparison of the junction temperature extraction results under high and low collector current densities, the accuracy of the proposed method can be validated. When compared to the heating current, the value of the measurement current is small and the power losses caused by this current can be neglected. The higher the power step between the heating and measurement processes, the higher the signal to noise ratio of the measurement and the more accurately the junction temperature can be monitored.

More importantly, electrical disturbances occur at the moment the heating current is cut off, which renders the signal insignificant for the beginning time. To eliminate the effect caused by electrical disturbances, an offset correction process is required.

For a homogeneous semi-infinite plate, when the heating power density of the material surface is a constant, the temperature rise of the plate is a linear function with the square root of the heating time during the cutting off transient as shown in (9) and (10).

$$\Delta T(t) = \frac{P_H}{A} k_{therm} \sqrt{t} \tag{9}$$

$$k_{therm} = \frac{2}{\sqrt{\pi c \rho \lambda}} \tag{10}$$

where c, ρ and λ are the thermal capacity, density and thermal conductivity of the material, respectively. In addition, k_{therm} is a constant for a certain material. Hence, for a given heating power density, electrical disturbances can be eliminated by reversely extending the temperature rise curve to the cut off moment under the coordinate of the square root time, as depicted in Fig. 22. The on-state voltage under high and low collector currents is measured and the offline junction temperature monitoring results after offset correction are listed in Table 3.

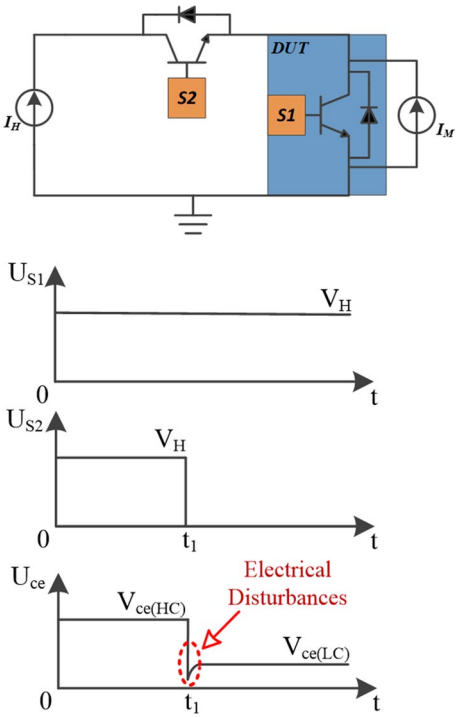

Fig. 21 Verification circuit and control sequence implementation

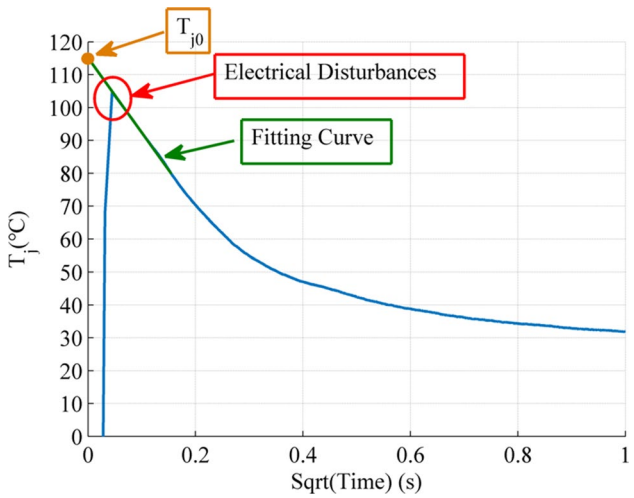

Fig. 22 Offset correction process implementation

Table 3 Experimental Results

Ic /A	$V_{ce(HC)}$ /mV	$T_{j(HC)}$ /°C	$V_{ce(LC)}$ /mV	$T_{j(LC)}$ /°C	Error /%
150	1070	50.56	487	48.45	4.4
200	1351	61.33	457	58.06	5.6
250	1497	73.33	421	68.93	6.4
300	1652	85.35	378	86.30	1.1
350	1833	102.77	334	104.26	1.4

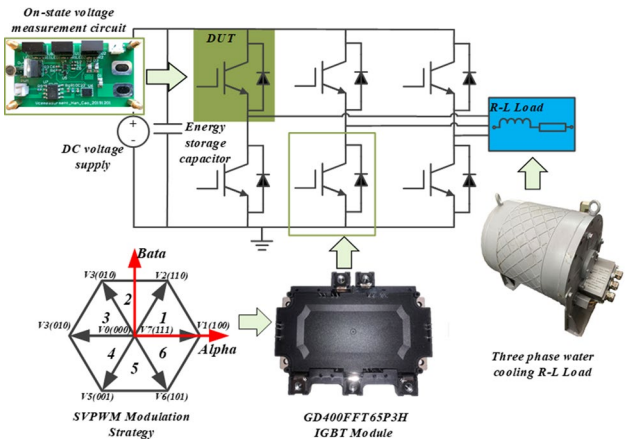

Fig. 23 Circuit schematic for temperature measurements in a three-phase converter

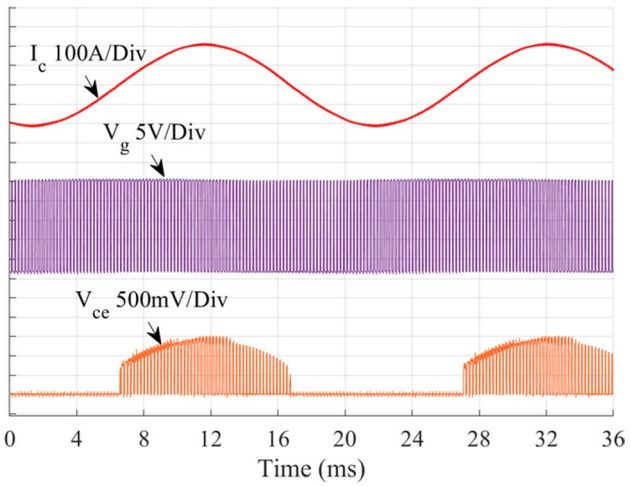

Fig. 24 Waveforms of a three-phase converter with SVPWM modulation

5 Online temperature monitoring during converter operation

In this section, the proposed junction temperature monitoring method is applied to a three-phase voltage source converter. The DUT is chosen as a GD400FFT650P3H IGBT module from Starpower, and it is modulated by the closed-loop space vector pulse width modulation (SVPWM) strategy with a 5 kHz switching frequency. A three-phase water cooling R–L load is used as shown in Fig. 23.

Figure 24 shows experimental waveforms during the junction temperature monitoring circuit operation. The

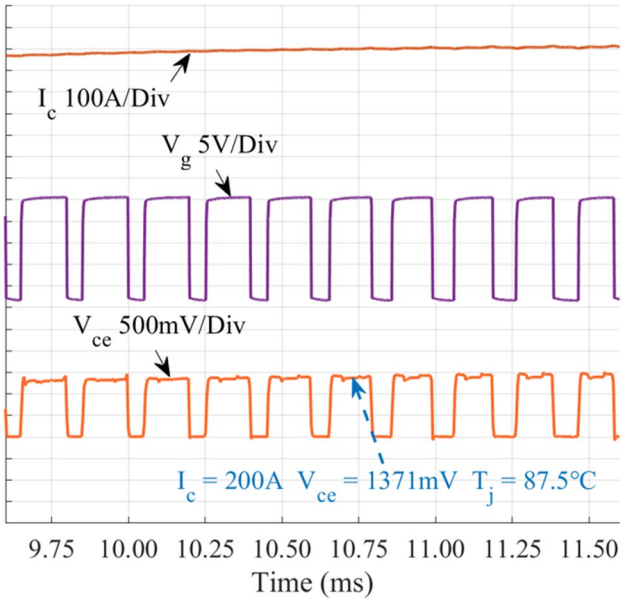

Fig. 25 IGBT junction temperature monitoring results with a 200A collector current

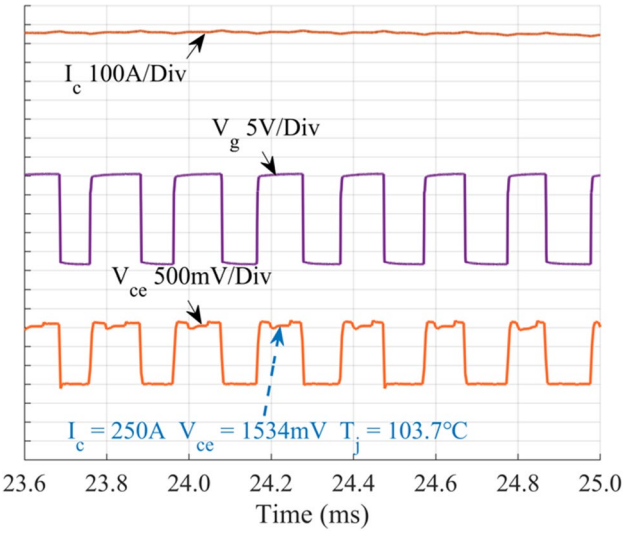

Fig. 26 IGBT junction temperature monitoring results with a 250A collector current

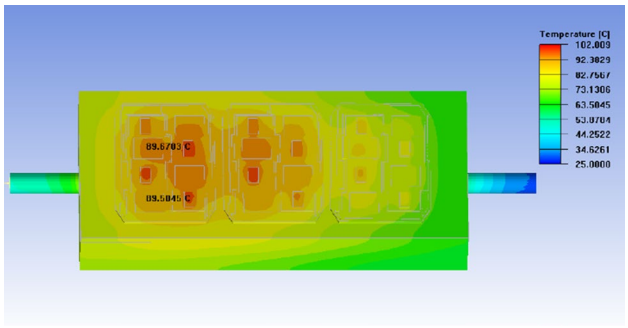

Fig. 27 Junction temperature simulation results with a 200A collector current

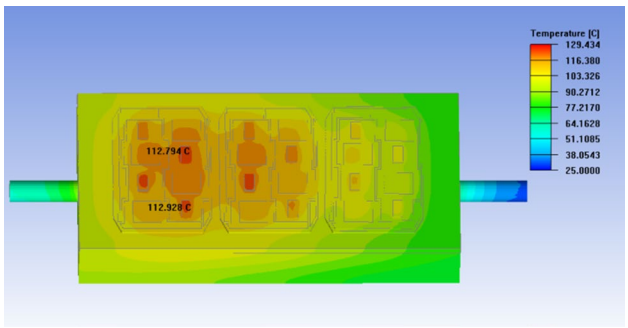

Fig. 28 Junction temperature simulation results with a 250A collector current

voltage measurement circuit obtains the on-state voltage and blocks the DC link voltage. The phase current is measured as the DUT collector current I_c during a transient in which the phase current is positive. When the phase current is negative, the anti-parallel diode of the DUT is conducting and the output of the on-state measurement circuit is 0.

To demonstrate the proposed IGBT junction temperature monitoring method, the on-state voltage is measured under 200A and 250A with a 15.4 V gate voltage. The obtained results are shown in Figs. 25 and 26, respectively.

The high-frequency noises in these waveforms are filtered by a digital filter. Due to the mutual inductances in each of the phases, there exists a tiny voltage overshoot in on-state voltage circuit output during current conversion transients. Hence, the sampling point is set in the middle of two current conversions to avoid measurement errors. The on-state voltage under 200A and 250A with a 15.4 V gate driver voltage indicates junction temperatures of 87.5 ℃ and 103.7 ℃ according to the calibration results.

To verify the junction temperature monitoring results, simulations are implemented in the finite element analysis (FEA) simulation tool. The geometry structure of the proposed IGBT module is created by SolidWorks, and the thermal simulations are generated by ANSYS Icepak. The effective values of the chips heating power dissipations are calculated by the integrating on-state voltage drop and conducting current. For each of the IGBT chips, heating power dissipations under 200A and 250A are 22.22 W and 30.55 W, respectively. Similarly, the dissipations are 19.83 W and 26.66 W for each of the diode chips. The obtained simulation results are illustrated in Figs. 27 and 28. The results under 200A (89.6703 ℃ and 89.5045 ℃) and 250A (112.794 ℃ and 112.928 ℃) agree well with the measurement results, which verifies the effectiveness of the proposed method.

6 Conclusion

This paper proposes an online junction temperature monitoring method based on $V_{ce(HC)}$ measurement for an IGBT power module. By calculating the on-state voltage with different collector current densities, the method is shown to be feasible. To accurately extract on-state voltage during operation, a measurement circuit that combines the advantages of both active MOSFET clamps and diode clamps is designed and tested with an acceptable measurement error and a few microseconds response time. The present method is verified by the JEDEC-51 standard recommended approach and applied to a three-phase voltage source converter controlled by the closed-loop SVPWM modulation strategy. In addition, an Icepak-based thermal simulation is implemented and the obtained results match well with the experimental results. In addition, the IGBT degradation model will be added to the calibration model for more accurate junction temperature measurement in future research.

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Han Cao was born in Hubei, China. He received his B.S. degree in Electrical Engineering from the Harbin Engineering University, Harbin, China, in 2016. He is presently working towards his Ph.D. degree at the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China. His current research interests include power device modeling and high-density converter designs.

Puqi Ning received his Ph.D. degree in Electrical Engineering from the Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, in 2010. He is presently working as a Full Professor at the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China. His current research interests include high-temperature packaging and high-density converter designs.

Xiaoguang Chai was born in Henan, China. He received his B.S. degree in Electrical Engineering from the Harbin Engineering University, Harbin, China, in 2018. He is presently working towards his M.S. degree at the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China. His current research interests include power device modeling and high-density converter designs.

Dan Zheng received her B.S. and M.S. degrees in Electrical Engineering from Beijing Jiaotong University, Beijing, China, in 2005 and 2008, respectively. From 2008 to 2018, she worked for the China Aerospace Science and Industry Corporation (CASIC), Beijing, China. Since 2018, she has been working as a Senior Engineer in the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China. Her current research interests include power electronic converter design.

Yuhui Kang received her B.S. degree in Electrical Engineering and Automation from Shijiazhuang Tiedao University, Hebei, China, in 2015; and her M.S. degree from the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, in 2019. Her current research interests include the packaging technology of power electronic devices.

Xuhui Wen received her B.S., M.S. and Ph.D. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 1984, 1989 and 1993, respectively. She is presently working as a Full Professor at the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China. Her current research interests include high power density electrical drives and generation, especially for electric vehicle applications.