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Coordinated control of series compensation link and bus interface converter in the AC–DC hybrid microgrid

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Abstract

To improve the fault ride-through capability and power quality of a hybrid microgrid (HMG), a series compensation link (SCL) is inserted between an AC–DC HMG and a utility grid, which forms a new HMG topology. Correspondingly, a decoupling coordinated control strategy for the SCL and a bidirectional AC–DC interlinking converter (BIC) is proposed based on a small signal model of the entire system and the principle of voltage regulation. The interferences between the SCL and the BIC due to the coupling of control factors are eliminated by the series and parallel decoupling methods that adopt additional current closed-loop control and output voltage feedforward control, respectively. The proposed HMG topology and strategy can ensure the realization of the predesigned functions of dual converters and avoid frequent switching between the grid-tied mode and the island mode, which improves the fault ride-through capability and power quality. Finally, the effectiveness of the proposed approach is verified by simulations and experiments.

Keywords AC–DC hybrid microgrid · Faulty utility grid · Power quality · Coordinated control · Power converter

1 Introduction

As an effective method to integrate various distributed generations (DGs) and to maximize the use of renewable and alternative energy, research on microgrids has been one of the most popular directions over the past years [1–3]. The AC–DC hybrid microgrid (HMG) combines the comprehensive advantages of AC microgrids and DC microgrids, which is a developmental trend in the microgrid field [4, 5].

In addition to the advantages of the topological structure, many accompanying constraints must be considered, such as the complex power management [6] and highly efficient control strategies of bidirectional AC–DC interlinking converters (BICs) [7], operation mode switching [8], power quality improvement and so on [9, 10]. Furthermore, the operation of an AC–DC HMG requires the coordinated operation of each part, and the BIC plays an important role in the reliability and effectiveness of the system. A variety of studies have been carried out on BIC control strategies. At present, BIC control schemes can be generally classified into three categories. These categories are centralized, decentralized and hierarchical control schemes [11].

For centralized and hierarchical control schemes, the power flow decision of the BIC usually requires the participation of the upper layer energy management system (EMS), and these schemes enable highly efficient power transmission with reduced losses and better performance in terms of frequency and bus voltage regulation [12, 13]. When the centralized-based or hierarchical-based BICs are operating in a faulty utility grid, the upper layer EMS can provide some vital support [14–16]. In [14], a centralized protection strategy has been proposed for microgrids, which can guarantee the reliability of the HMG and protect the devices. A flexible control scheme, which can improve resilience to utility grid perturbations, of the BIC based on large-bandwidth triple-loop organization is presented in [15]. Moreover, a uniform control strategy of the BIC for a hierarchical controlled AC–DC HMG is presented in [16], which is able to ensure smooth operation in the event of faults. Although centralized or hierarchical control schemes have plenty of advantages, many problems are unavoidable. These problems include the increase cost

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and operation complexity caused by adopting the communication infrastructure and a decrease in reliability due to communication failure.

For decentralized control schemes [17–19], the power flow decisions depend on local information of the loads, which can reduce cost, and make the system simpler and more reliable. At present, the decentralized control schemes of BIC are entirely based on the bus voltage regulation principle, the droop principle or a hybrid of these two principles [20]. However, the improvements in BIC control schemes, whether they are improvements in the accuracy of power distribution, power quality or function compounding, are only considered under ideal utility grid conditions in most instances. In [21], an improved droop scheme, which introduces a superimposed frequency in a DC subnet, has been proposed to improve power accuracy and quality. Since decentralized-based BICs get no support from the upper layer infrastructure, the faulty environments of utility grids are not negligible. A control strategy of multi-BICs, which operates in unbalanced utility grids with zero active power oscillation under various power factors, was proposed in [22]. A virtual impedance based on a fault current limiter was presented to improve the reliability and stability of multiple inverter interfaced DGs under an AC microgrid in [23]. A reactive power secondary regulation algorithm based on high bandwidth communication was added to traditional droop control to improve the low-voltage ride-through capability in [24, 25]. However, the addition of a communication link contradicts the original intention of the distributed control scheme. So far, only a few efforts have been made on the operation of a BIC under a faulty utility grid, and existing methods are mostly considered from the perspective of improving BIC control schemes, which cannot completely eliminate negative impacts of utility grid failures or protect related devices.

This paper proposes to insert a series compensation link (SCL) between a conventional AC–DC HMG and a utility grid. Then, it models the system and designs a coordinated control scheme for the SCL and the BIC to achieve reliable, continuous and high-quality operation even under a non-ideal utility grid. Scenarios such as a voltage fault of a utility grid, power fluctuations of AC or DC subnets and harmonic distortion of an AC subnet are considered in the proposed control scheme, which is based on analyzing the mutual influence between the SCL and the BIC for their connection in the AC and DC bus.

This paper is organized as follows. The configuration and modeling of an AC–DC HMG with a SCL are introduced in Sect. 2. The operation modes and the proposed control scheme are presented in Sect. 3. The effectiveness of the proposed approach is verified by simulation and experimental results in Sects. 4 and 5. Some conclusions are given in Sect. 6.

2 Configuration and modeling of an improved hybrid microgrid

2.1 Grid configuration

The topology of the entire power system is shown in Fig. 1. In the dashed box is the improved AC–DC HMG made up of an AC–DC HMG and the newly added SCL. The AC–DC HMG consists of various AC sources, AC loads, DC sources and DC loads, which are connected to their corresponding AC bus or DC bus. The AC and DC buses are connected through a BIC (hereinafter referred to as VSC_M). The newly added SCL consists of a series compensation transformer (SCT) and a corresponding slave voltage source converter (VSC_S). The AC bus of the HMG is tied to a utility grid by the SCT, and the DC side of VSC_S is directly tied to the DC bus.

The overall system of the improved AC–DC HMG has a similar structure to a unified power quality conditioner (UPQC). However, they are fundamentally different. A UPQC is a device to improve the power quality of sensitive loads. The energy that a UPQC relies on to work comes from a utility grid and is temporarily stored in the DC-side energy storage elements. The parallel and series converters of a UPQC serve as a parallel active power filter to compensate harmonic and reactive currents, and a dynamic voltage regulator serves to ensure the reliability of the power supply for sensitive users. However, the proposed HMG with a SCL has a variety of DGs and loads in the AC and DC sides. Thus, the roles of VSC_M and VSC_S are different. VSC_M is used for bidirectionally controlling the power flow, which supports the bus voltage and provides the auxiliary service of power quality control. The SCL needs to realize the dynamic voltage compensation and fault current limitation to ensure the high-quality power supply of the AC subnet and to protect the BIC, loads, sources and devices on the HMG side from voltage fluctuation and flicker.

In addition, the sources of the AC subnet mainly include a miniature turbine (MT), photovoltaics (PV) and wind power generation (WG). The loads of the AC subnet include general loads, sensitive loads and non-linear loads. The sources of the DC subnet contain many new energy power generations and energy storage (ES) devices.
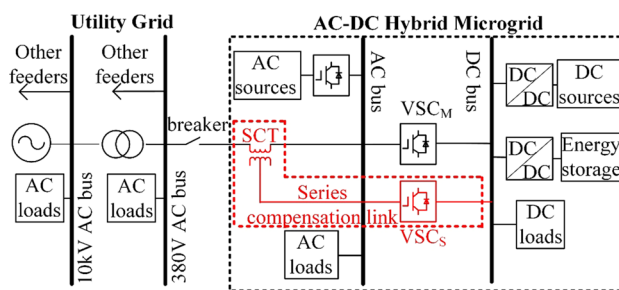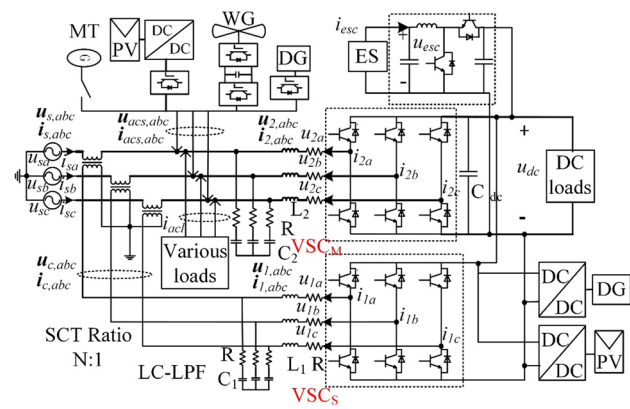

Fig. 1 Topology of the improved AC–DC HMG

Fig. 2 Specific structure of the improved AC–DC HMG

2.2 Modeling of VSC$_S$ and VSC$_M$

Figure 2 shows the specific structure of the improved AC–DC HMG. According to the simplified system circuit, it is easy to obtain the whole model of VSC$_S$ and VSC$_M$ in the *abc*-frame. Then, using the coordinate transformation formula $T_{abc/dq}$, it is possible to convert the model from the *abc*-frame into the *dq*-frame.

$$T_{abc/dq0} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (1)$$

The model of VSC$_S$ in the *dq*-frame is:

$$\begin{cases} L_1 \dfrac{di_{1d}}{dt} = -Ri_{1d} - (u_{sd} - u_{acsd}) \cdot N + \omega L_1 i_{1q} + u_{dc}d_{1d} \\[2mm] L_1 \dfrac{di_{1q}}{dt} = -Ri_{1q} - \left(u_{sq} - u_{acsq}\right) \cdot N - \omega L_1 i_{1d} + u_{dc}d_{1q} \\[2mm] i_{1d} = C_1 \dfrac{d(u_{sd} - u_{acsd}) \cdot N}{dt} + \dfrac{1}{N}i_{sd} - \omega C_1 \left(u_{sq} - u_{acsq}\right) \cdot N \\[2mm] i_{1q} = C_1 \dfrac{d(u_{sd} - u_{acsd}) \cdot N}{dt} + \dfrac{1}{N}i_{sq} + \omega C_1 \left(u_{sd} - u_{acsd}\right) \cdot N \end{cases}, \quad (2)$$

where d_1 is the PWM duty cycle of VSC$_S$.

The model of VSC$_M$ in the *dq*-frame is:

$$\begin{cases} L_2 \dfrac{di_{2d}}{dt} = -Ri_{2d} - u_{acd} - \omega L_2 i_{2q} + u_{dc}d_{2d} \\[2mm] L_2 \dfrac{di_{2q}}{dt} = -Ri_{2q} - u_{acq} + \omega L_2 i_{2d} + u_{dc}d_{2q} \\[2mm] i_{2d} = -i_{sd} - \left(i_{acsd} - i_{acld}\right) + C_2 \dfrac{du_{acd}}{dt} - \omega C_2 \cdot u_{acq} \\[2mm] i_{2q} = -i_{sq} - \left(i_{acsq} - i_{aclq}\right) + C_2 \dfrac{du_{acq}}{dt} + \omega C_2 \cdot u_{acd} \end{cases}, \quad (3)$$

where d_2 is the PWM duty cycle of VSC$_S$.

The model of the DC bus voltage in the *dq*-frame is:

$$C_{dc}\frac{du_{dc}}{dt} = -d_{1d}i_{1d} - d_{1q}i_{1q} - d_{2d}i_{2d} - d_{2q}i_{2q} - \frac{u_{dc}}{R_L} + \frac{u_{sdc} - u_{dc}}{R}, \quad (4)$$

where u_{sdc} and R are the equivalent voltage and internal resistance of the DC sources.

Based on models of VSC$_S$ and VSC$_M$ in the *dq*-frame, the entire small signal linearization model is obtained by the small signal perturbation method, and the entire equivalent circuit diagram is shown in Fig. 3.

3 Coordinated operation of the improved hybrid microgrid

The main objective of this section is to design both the operating mode of the improved AC–DC HMG and the coordinated control strategy of VSC$_S$ and VSC$_M$.

3.1 Operating mode of the improved AC–DC HMG

According to the voltage fault severity of the utility grid, the operation of the improved AC–DC HMG can be divided into three modes as shown in Fig. 4.

1. MODE I:

    In Mode I, VSC$_S$ works in the zero output impedance mode. According to the power balance between the AC subnet and the DC subnet, VSC$_M$ can work in stop mode, rectification mode, inverter mode, support DC bus voltage, and compensate the harmonic and other currents to optimize power quality of the improved AC–DC HMG.
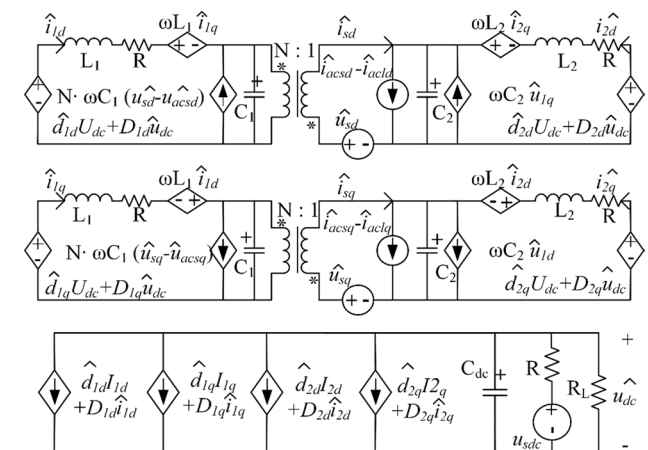
2. MODE II:

Fig. 3 Small signal model of VSC$_S$ and VSC$_M$ in the *dq*-frame
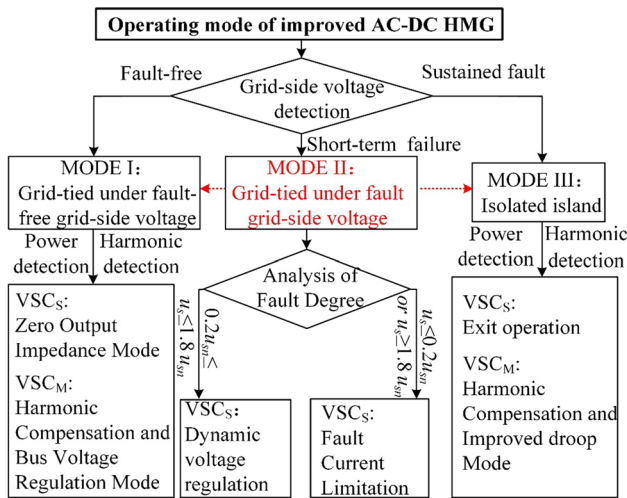
Fig. 4 Operating mode of the improved AC–DC HMG

In Mode II, VSC$_S$ can operate in the dynamic voltage compensation mode or the fault current limitation mode, depending on the voltage fault severity of the utility grid.

When VSC$_S$ operates in the dynamic voltage compensation mode, DGs which adopt the droop control scheme, ES devices and other dispatchable micro-sources should work together to provide the required power for voltage compensation to ensure the reliable and continuous power supply of the AC subnet. After the voltage is compensated by VSC$_S$, VSC$_M$ can run in Mode I.

When VSC$_S$ operates in the fault current limitation mode, the ES runs in the voltage regulation mode, and the MT must be controlled to support the bus voltage of the AC subnet. VSC$_S$ adjusts the output impedance of the SCT to protect the safety of the AC subnet, BICs and loads in the low-voltage feeder side. However, if the grid-side voltage fault is too severe or the fault duration is too long, the capacity of the SCL is insufficient to limit the current. Then, the improved AC–DC HMG switches to Mode III.

3. MODE III:

In Mode III, VSC$_S$ is no longer operating and VSC$_M$ works in the improved droop control mode. Due to the fact that there is no support from the utility grid, the MT starts to provide voltage with the reference amplitude and frequency of the AC subnet. In addition, the ES devices of the DC subnet work in the voltage regulation mode to support the DC bus voltage. PV, WG and other DG sources change from a MPPT or PQ control scheme to the droop control scheme to adapt to operation in the island mode.

3.2 Coordinated control strategy for VSC$_S$ and VSC$_M$

By dividing the operating mode of the improved AC–DC HMG into three parts, the functions of each power converter in this system can be coordinated. The control schemes of VSC$_S$ and VSC$_M$ are described in detail as follows.

The control scheme for VSC$_S$ is shown in Fig. 5.

In Fig. 5, the output impedance of the SCT can be adjusted by controlling VSC$_S$ to meet following requirements: (1) to reach zero output impedance under a normal utility grid; (2) to realize dynamic voltage regulation during a short-term failure; (3) to achieve fault current limitation under a severe sustained failure. It can be seen that the scheme includes fault voltage detection, reference voltage generation, a compensation algorithm and so on.

In the considered scenario, there is an interlinking converter in the improved AC–DC HMG, and it runs in the grid-tied mode. Therefore, the control scheme for VSC$_M$ is based on the bus voltage regulation principle supplemented by harmonic compensation, which can ensure a bidirectional power flow, support DC bus voltage and compensate the harmonic current in the AC subnet, as shown in Fig. 6.

As shown in Fig. 2, VSC$_S$ and VSC$_M$ are coupled by the SCT in the AC bus and connected to the DC bus. It is necessary to consider the coupling between the different outputs of the dual converters, especially when they operate jointly in a faulty utility grid.
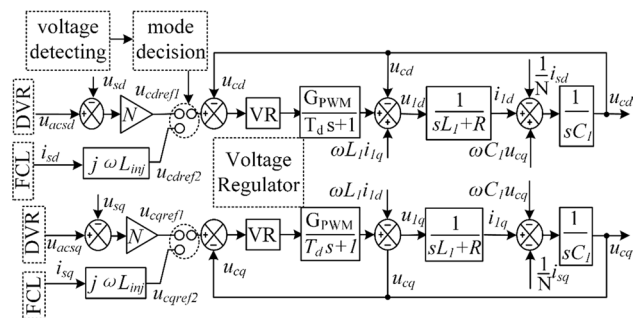

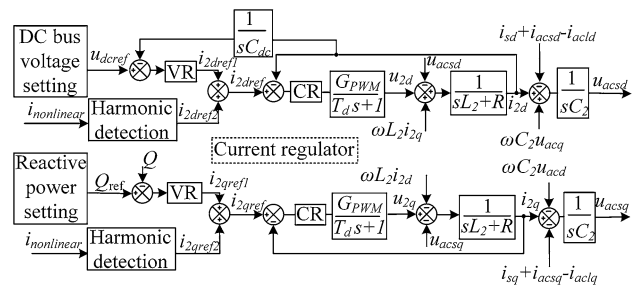**Fig. 5** Control block diagram of VSC$_S$

Fig. 6 Control block diagram of VSC$_M$

To avoid the negative impact of coupling on a system, an improved control scheme should be adopted. Before designing the scheme, the coupling principle based on the small signal model in Fig. 3 and the conventional control scheme of VSC_S and VSC_M should be analyzed.

The implementation process of the previous VSC_S scheme is as follows: (1) adjust u_c to compensate for faulty voltage; (2) modify u_1 according to the updated u_c; (3) modify i_1 according to the updated u_1; (4) the variation of i_1 affects i_s, which further affects i_2 and u_{dc}. Thus, the operation of VSC_M is affected by the operation of VSC_S. Likewise, the implementation of the VSC_M scheme affects the normal operation of VSC_S.

Taking the d-axis as an example, the d-axis control formula of VSC_S is:

$$u_{1d} = G_{VR} \cdot \left(u_{cdref} - u_{cd} \right). \tag{5}$$

In addition, the d-axis control formula of VSC_M is:

$$\begin{cases} i_{2dref} = G_{VR} \cdot \left(u_{dcref} - u_{dc} \right) + i_{2dref2} \\ u_{2d} = G_{CR} \cdot \left(i_{2dref} - i_2 \right) + \omega L_1 i_{1q} - u_{acsd} \end{cases}. \tag{6}$$

According to the above-mentioned coupling principle, additional output current i_1 closed-loop control link is added in the VSC_S control module and a feedforward of the AC bus voltage u_{acs} is added in the VSC_M control module in the proposed scheme to eliminate their interplay. The increased sampling of i_1, which is equivalent to $\frac{1}{N} \cdot i_s$ at the steady state, can also be used in the control scheme of VSC_M to suppresses the DC bus voltage fluctuation caused by intermittent DGs or switching loads. Similarly, the updated d-axis control formula of VSC_S becomes:

$$\begin{cases} i_{1d} = G_{VR} \cdot \left(u_{cdref} - u_{cd} \right) \\ u_{1d} = G_{CR} \cdot \left(i_{1dref} - i_{1d} \right) + \omega L_1 i_{1q} + u_{acsd} \end{cases}. \tag{7}$$

In addition, the d-axis control formula of VSC_M becomes:

$$\begin{cases} i_{2dref} = G_{VR} \cdot \left(u_{dcref} - u_{dc} \right) + i_{2dref2} \\ u_{2d} = G_{CR} \cdot \left(i_{2dref} - i_2 + \frac{1}{N} \cdot i_{1d} \right) + \omega L_1 i_{1q}, \\ \quad - G \cdot u_{acsd} - u_{acsd} \end{cases} \tag{8}$$

where G is the transfer function of i_2 to u_{acs}.

Since the system is in the dq-frame, PI controllers are used for both the voltage regulator (VR) and the current regulator (CR), whose transfer function $G_{PI}(s)$ is:

$$G_{VPI,n}s = k_{VP,n} + \frac{k_{VI,n}}{s}, \tag{9}$$

$$G_{CPI,n}s = k_{CP,n} + \frac{k_{CI,n}}{s}, \tag{10}$$

where $n = 1$, 2 and k_{VP} and k_{CP} affect the stability and response speed of the system, and k_{VI} and k_{CI} are related to the dynamic performance and static errors. The control parameters in this paper are listed in Table 1, and the improved coordinated control scheme of VSC_S and VSC_M is shown in Fig. 7.

4 Simulated verification

To demonstrate the effectiveness of the improved AC–DC HMG topology and the corresponding coordinated control strategy, detailed simulations were implemented in MATLAB/Simulink with the system depicted in Fig. 2. For the convenience of analyzing the coordinated operation of VSC_S and VSC_M without losing generality, PV, WT and other DGs were simplified. In addition, the nonlinear load is a three-phase uncontrolled rectifier with a resistor in the DC side. The system parameters are given in Table 2.

Figures 8 and 9 show the contrastive operation effect of VSC_S and VSC_M in different system modes when using the conventional control strategy and the improved control strategy. The working conditions were designed as follows.

1. Initially, VSC_S and VSC_M begin to run at 0.1 s. During 0.1–0.2 s: the utility grid was ideal, VSC_S operated in the zero output mode, and VSC_M operated in the shutdown mode. The improved AC–DC HMG worked in Mode I.
2. During 0.2–0.6 s: The utility grid dropped to 0.5 pu at 0.2 s, a power fluctuation of the DC subnet occurred at 0.3 s, and the fault of the utility gird was removed at 0.6 s. The system worked in Mode II.
3. During 0.2–0.8 s: the system was restored to the initial operation state.

When comparing Fig. 8 with Fig. 9, it can be observed that when the two converters start working, the compensation performance and the DC bus voltage were degraded in Fig. 8. In addition, the transient process of i_2 lasted for a long

Table 1 Control parameters

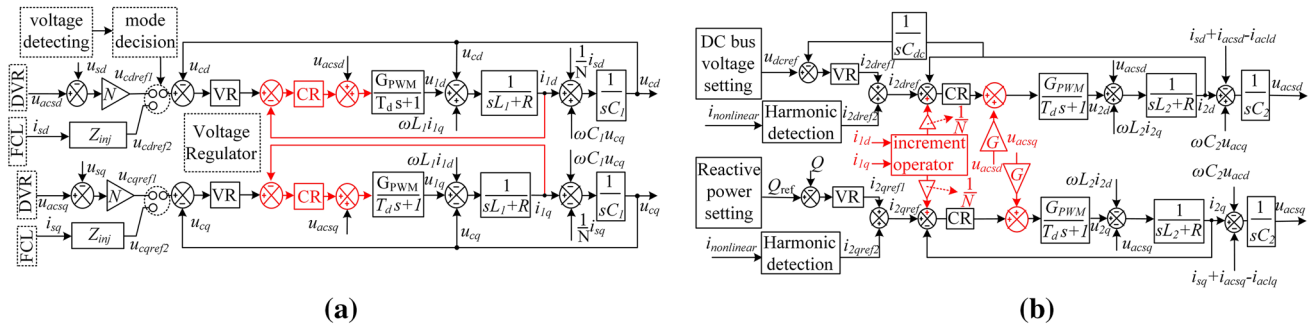| Regulators	Parameters	Simulation	Experiment
VR of VSC_S	k_{VP1}	0.1	0.1
	k_{VI1}	1	0.5
CR of VSC_S	k_{CP1}	0.1	0.5
	k_{CI1}	1	1
VR of VSC_M	k_{VP2}	0.1	0.2
	k_{VI2}	1	0.1
CR of VSC_M	k_{CP2}	0.2	0.05
	k_{CI2}	1	0.1

Fig. 7 Improved control block diagram of the control scheme of: **a** VSC$_S$; **b** VSC$_M$

Table 2 System parameters in the simulation and experiment

	Parameters	Simulation	Experiment
Utility grid	Nominal voltage u_s	220 V/50 Hz	50 V/50 Hz
	Line inductance	0.3 mH	0.3 mH
	Line resistance	0.1 Ω	0.1 Ω
AC–DC HMG	AC-link voltage u_{acs}	220 V/50 Hz	50 V/50 Hz
	DC-link voltage u_{dc}	800 V	200 V
	Rated power of DGs on AC-link	30 kW	2 kW
	Rated power of linear load on AC-link	20 kW	1.5 kW
	Rated power of sensitive load on AC-link	10 kW	0.5 kW
	Rated power of DGs on DC-link	30 kW	1 kW
	Rated power of linear load DC-link	30 kW	1 kW
SCL	Rated voltage of SCT	220 V/50 Hz	220 V/50 Hz
	SCT ratio	1:1	1:1
	LC-LPF of VSC$_S$ L_1	2 mH	2 mH
	LC-LPF of VSC$_S$ C_1	20 μF	20 μF
	VSC$_S$ switch frequency	10 kHz	10 kHz
IC	LC-LPF of VSC$_M$ L_2	6 mH	6 mH
	LC-LPF of VSC$_M$ C_2	20 μF	20 μF
	VSC$_M$ switch frequency	10 kHz	10 kHz
	DC-link capacitor C_{dc}	1000 μF	1000 μF
Rectifier load	DC-side resistor	40 Ω	40 Ω
	AC-side inductor	6 mH	6 mH

time in Fig. 8d. However, the proposed method eliminated the deterioration of the bus voltage and obtained a better dynamic response to the power fluctuation in Fig. 9.

Figure 10 shows the simulated operation effect of VSC$_S$ in the fault current limitation mode. The utility grid sagged to 0 pu in Fig. 10a and swelled to 2.0 pu in Fig. 10d. It can be seen that the large faulty current between the utility grid and the AC subnet had been noticeably restrained, which protects the AC subnet. VSC$_M$, and the low-voltage feeder.

5 Experimental results

To further verify the performance of the improved AC–DC HMG in actual operation, an experimental platform was set up with the system parameters listed in Table 2. In this system, the coordinated control scheme for VSC$_S$ and VSC$_M$ was implemented by dSPACE 1006, the dual converters consisted of Infineon insulated-gate bipolar
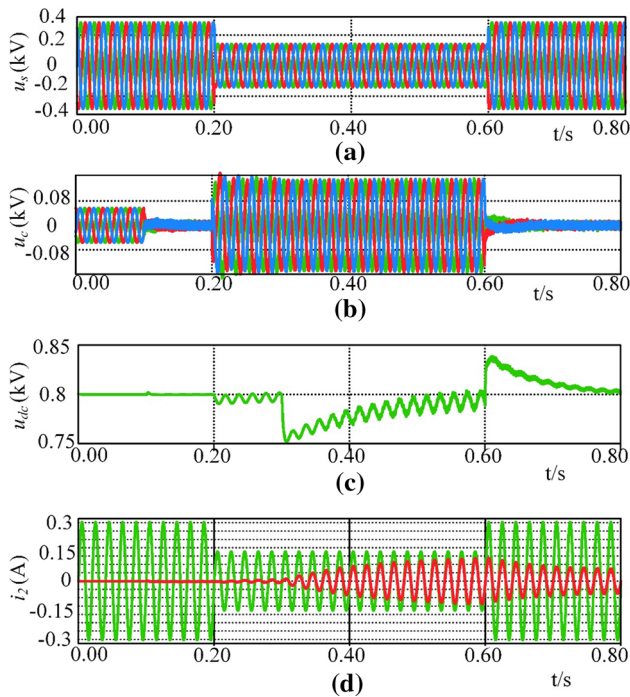
Fig. 8 Simulated operation effects of VSC$_S$ and VSC$_M$ in different system modes under the conventional scheme: **a** utility grid voltage; **b** compensation voltage; **c** DC bus voltage; **d** VSC$_M$ output current (red waveform) of phase-A
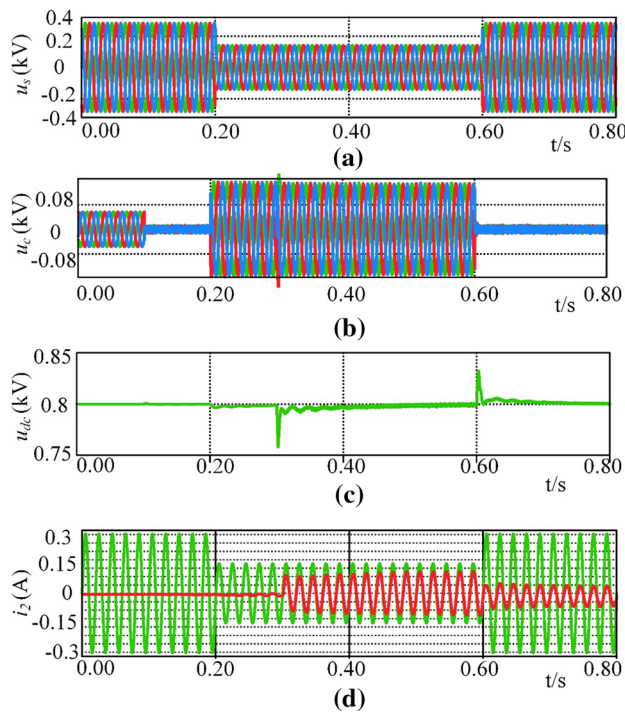

Fig. 9 Simulated operation effects of VSC$_S$ and VSC$_M$ in different system modes under the improved scheme: **a** utility grid voltage; **b** compensation voltage; **c** DC bus voltage; **d** VSC$_M$ output current (red waveform) of phase-A

transistors (IGBTs), which were driven by a Concept 2SC0108T, and the supply voltages were generated by a 12-kVA programmable AC source (chrome 61511) and a 15-kW DC source (chrome 62150H). Photographs of the experimental platform appear in Fig. 11.

In the experiment, the output voltage was 50 V and the short circuit impedance of the SCT and the lines was 0.883 Ω. As a result, the single SCT capacity was designed as 3 kVA to meet the requirements of voltage sag with a certain margin. The capacity of VSC$_S$ was based on the SCT capacity, and the eligible IGBTs and drives were selected as in Table 3. It can be seen from Table 3 that the cost of the SCL is not high, especially considering its benefits for improving the power quality and system reliability along with its ability to avoiding the loss caused by components damage.

5.1 Fault ride-through performance of the improved AC–DC HMG

Figure 12 shows experimental waveforms of the DC bus voltage u_{dc}, utility grid voltage u_s, AC bus voltage u_{acs} and output current i_2 of VSC$_M$, and the compensation voltage u_c of VSC$_S$ from top to bottom. Due to the shortage of an oscilloscope voltage sampling interface, only the phase-A waveforms of all three-phase voltages are given.

In Fig. 12, when the improved AC–DC HMG is operated in Mode I, it can be seen that i_2 has the same phase as u_{acs} and that u_{dc} was stable. This means VSC$_M$ was working in the rectifier state, and the SCT output almost reached 0 by VSC$_S$. When the system operated in Mode II, the utility grid dropped to 0.5 pu at T_1. Then, VSC$_S$ only took one fundamental cycle to compensate the faulty voltage, which ensured the reliable operation of the HMG. Furthermore, even during such a fault, VSC$_M$ was still able to operate normally to ensure the power balance and stability of the DC bus voltage. The utility gird fault was removed at T_4, and the system returned to its initial state. The proposed topology significantly enhances the fault ride-through capability and avoids frequent switching between the grid-tied mode and the island mode.

5.2 Power quality and safety performance of the improved AC–DC HMG

Figure 13 shows experimental waveforms of the DC bus voltage u_{dc}, the utility grid current i_s, the nonlinear load current $i_{Non\ load}$, the VSC$_M$ output current i_2 and the harmonic spectrum of the phase-A utility grid current from top to bottom.

As shown in Fig. 13a, VSC$_M$ operated in the stop state without the harmonic compensation function when a nonlinear load was put into operation. The current of the HMG
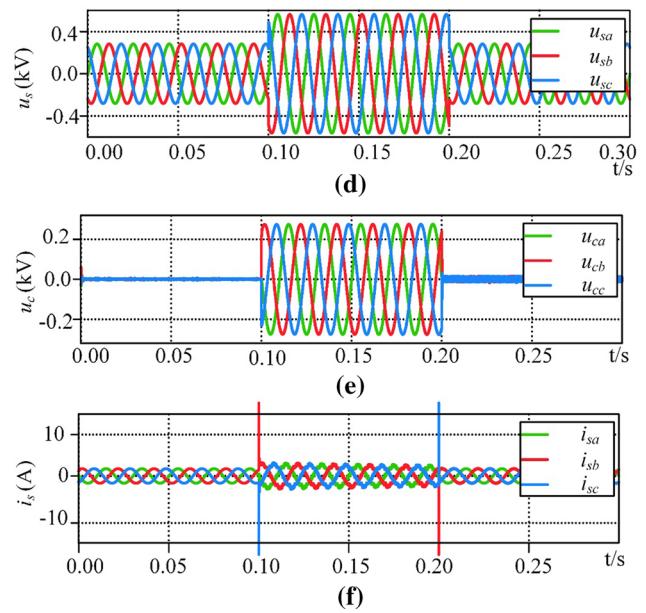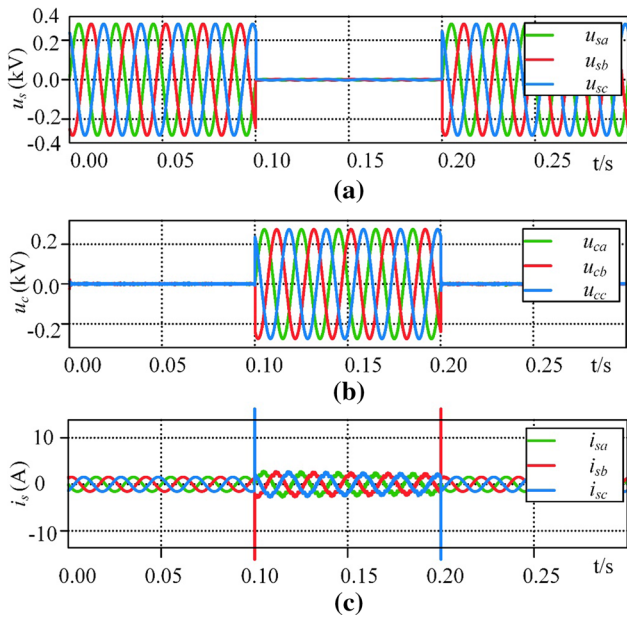
Fig. 10 Simulated operation effect of VSC$_S$ in the fault current limitation mode: **a** utility grid voltage under voltage sag conditions; **b** compensation voltage under voltage sag conditions; **c** utility grid current under voltage sag conditions; **d** utility grid voltage under voltage swell conditions; **e** compensation voltage under voltage swell conditions; **f** utility grid current under voltage swell conditions
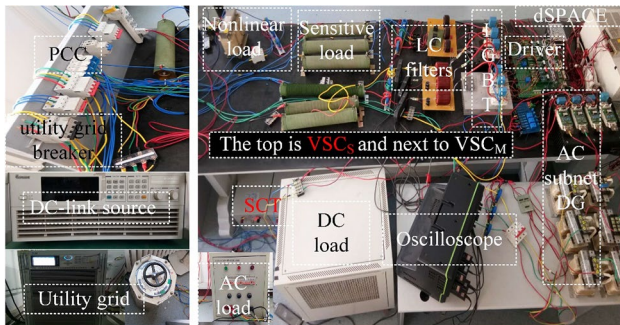

Fig. 11 Experimental platform

Table 3 Expense list of the SCL

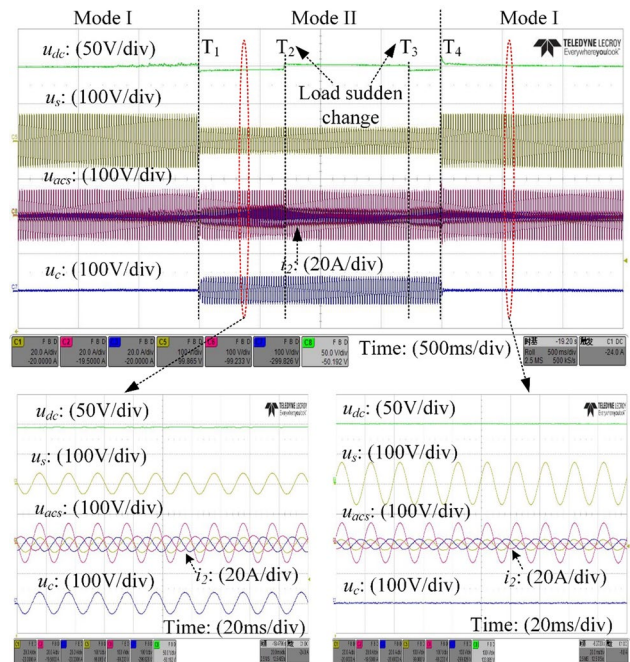| Devices	Model	Unit-price/10^4 yuan	Quantity	Total sum/10^4 yuan
SCT	DG-3kVA	0.15	3	0.45
IGBT	FF150R12RT4	0.012	3	0.036
Drive	2SC0108T	0.01	3	0.03
	2BR0108T	0.01	3	0.03
Total sum				0.546

Fig. 12 Experimental performance of the improved AC–DC HMG when a short-term fault occurs in the utility grid

was distorted and power quality of the system declined. In the case of the proposed scheme, as shown in Fig. 13b, it can be seen that i_s was regulated to be sinusoidal and that the power quality was significantly improved.
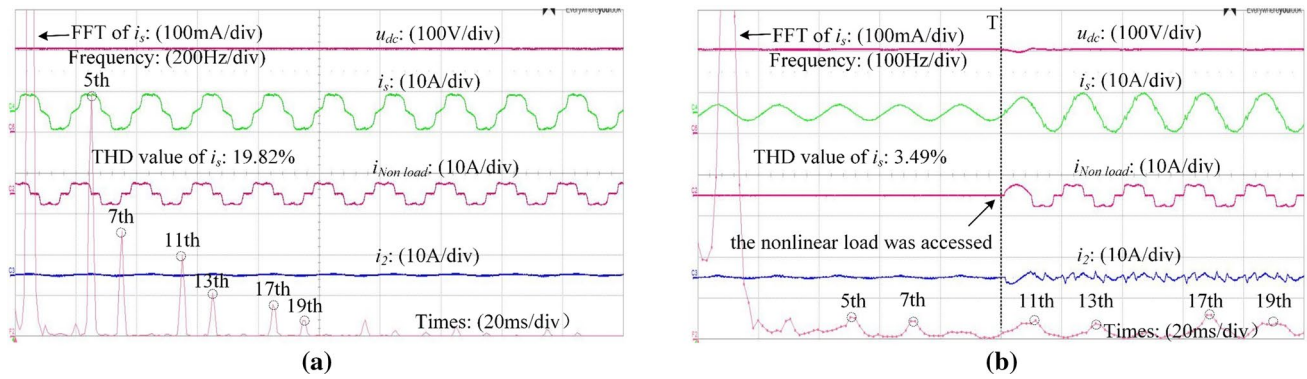
Fig. 13 Experimental performance of the improved AC–DC HMG when a nonlinear load was put into operation: **a** without the harmonic compensation function of VSC$_M$; **b** with the harmonic compensation function of VSC$_M$
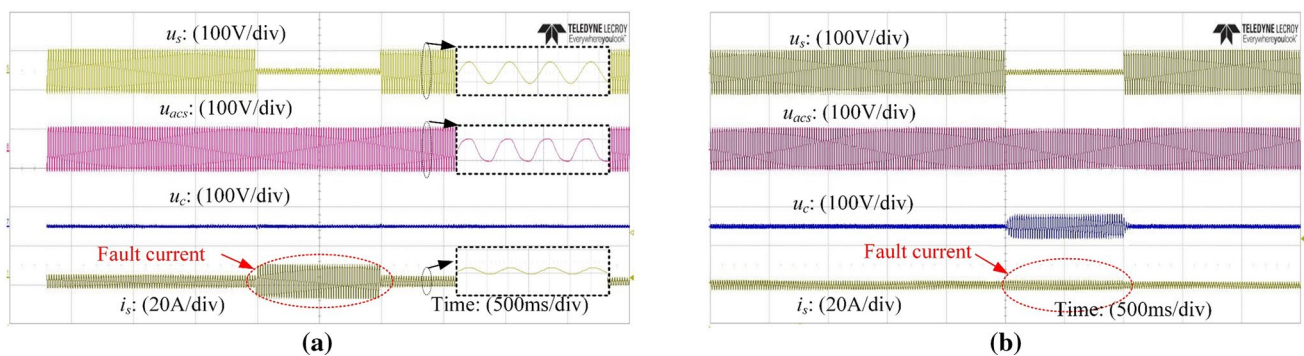

Fig. 14 Experimental performance of the improved AC–DC HMG when a serious fault occurs in the utility grid: **a** without the current limitation of VSC$_S$; **b** with the current limitation of VSC$_S$

Figure 14 shows experimental waveforms of the utility grid voltage u_s, AC bus voltage u_{acs}, VSC$_S$ compensation voltage u_c and utility grid current i_s. When a severe fault occurred in the utility grid, which was dropped to 0 pu, VSC$_S$ operated in the current limitation mode. It can be seen that the fault current had been completely limited in Fig. 14b, which enhanced the safety of this system. In particular, the fault current was not so large by increasing the line impedance, which guaranteed the safety of the experimental process.

The experimental results in Figs. 12, 13 and 14 validate the feasibility and performance of the improved AC–DC HMG.

6 Conclusions

This paper proposes an improved topology of an AC–DC HMG and its corresponding coordinated control strategy. Both of them have been verified by simulation and experimental results. Based on these results, the improved AC–DC HMG has the following advantages.

1. When a minor fault of a utility grid occurs, the voltage sag or swell is within 0.8 pu, and the system operates normally.
2. When a serious fault of a utility grid occurs, the voltage sag or swell is over 0.8 pu, and the SCL ensures the safety of the AC–DC HMG and the low-voltage feeder.
3. VSC$_S$ and VSC$_M$ can coordinate to achieve the optimal power quality of the AC–DC HMG.

In summary, the proposed approach enhances fault ride-through capability, avoids frequent switching between the grid-tied mode and the island mode, and improves the power quality of the AC–DC HMG.

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