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ORIGINAL ARTICLE

Performance study of various discontinuous PWM strategies for multilevel inverters using generalized space vector algorithm

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Abstract
The space vector (SV) pulse-width modulation (PWM) approach is extensively preferred in the control of multilevel inverters (MLI). In this paper, the implementation of various advanced discontinuous pulse-width modulation (ADPWM) strategies using a generalized space vector algorithm is presented. The ADPWM MIN, ADPWM MAX, and ADPWM 0 ~ ADPWM 3, strategies are developed using a combination of advanced switching sequences 1012-2721 and 0121-7212. The output performance in terms of voltage THD, current THD, and reduction of common mode voltage (CMV) of a three-level inverter-fed induction motor for different ADPWM strategies is investigated initially through MATLAB simulation and comparison of the obtained results is presented. It can be observed that the ADPWM 1 strategy with the 0121–7212 switching sequence offered the best performance in terms of the voltage and current THD at the modulation range of 47.5 Hz to 50 Hz. In addition, it is validated experimentally. Experimental work is done on a V/f-controlled three-level inverter-fed induction motor with the help of dSPACE. To validate the study, experimental results of the line voltage, stator current, and CMV waveforms for the ADPWM 1 (optimal performance PWM strategy) are presented in comparison with the 0127 sequence at fundamental frequencies of 49 Hz and 30 Hz.

Keywords MLI · Generalized SVPWM algorithm · Space vector · Multilevel inverters · Bus-clamping · ADPWM

1 Introduction

The SV-based PWM strategies are widely preferred for MLI than carrier comparison, due to advantages of high D.C. bus voltage utilization, improved harmonic spectrum performance, less CMV, and easy of digital implementation [1]. However, the conventional SVPWM produces n^3 switching states and $(n-1)^2$ triangles in each sector for an n level inverter [2–6]. When "n" increase, it impacts the complexity in the SV-based PWM. So far, various advanced SVPWM strategies are proposed by authors in [7–17] with reduced complexity. Further switching sequences were proposed in [18], and using these sequences, various discontinuous SVPWM strategies are presented in [19] to improve the performance of MLIs. The strategies in [7, 8] are developed using the conventional SVPWM. The decomposition-based SVPWM was presented in [9–11]. The offset vector-based approach is presented in [12, 13]. Integer/fractional methods are presented in [14, 15]. The implementation of various advanced discontinuous SVPWM strategies based on a decomposition method for a three-level inverter was presented in [16]. However, the voltage and current THD are both high. The generalized SVPWM with a fixed number of steps for inverters of any level with improved performance was presented in [17] with a conventional sequence 0127. In this article, an extended version of the algorithm in [17] for various ADPWM strategies using various advanced sequences is presented to further improve performance at a higher frequency range of 47.5 Hz to 50 Hz. The performance investigations in terms of voltage THD, current THD, and reduction of the CMV for various ADPWM strategies and CSVPWM are initially carried out through

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MATLAB simulation. A combination of advanced switching sequences 1012, 2721 and 0121, 7212 is used to develop these ADPWM strategies. The strategy and sequence that offered best performance through simulation is validated experimentally on a V/f-controlled three-level inverter-fed induction motor using dSPACE.

Rest of the paper is organized as follows. The procedure to execute various ADPWM strategies is discussed in Sect. "2". A comparison of simulation results is presented in Sect. "3". Experimental results are presented in Sect. "4" and some conclusions are given in Sect. "5".

2 Space vector-based ADPWM strategies

In SV-based ADPWM strategies, the three-level inverter top or bottom two switches of each phase leg are continuously maintained at the on state or off state one after the other two phases. Therefore, the respective phase output terminal is continuously clamped to any one of the input dc bus voltages, and the single-time or double-time switching nature is exhibited in the other two phase legs. The major impact of this in several ADPWM strategies is the clamping of switches to the input dc bus. Based on clamping, the ADPWM strategies are categorized into unipolar and bipolar strategies. In the unipolar strategies, the switches are continuously clamped to either the positive bus or the negative bus within a sampling time interval. There are two unipolar strategies: ADPWM MIN and ADPWM MAX. In case of bipolar strategies, the switches are clamped to the input positive bus and the negative bus within a sampling time interval. Based on the distribution of the clamping period and the place where it occurs, bipolar strategies are classified as ADPWM 0 ~ ADPWM 3. The procedure for the implementation of ADPWM approaches with the 1012-2721 switching sequence is reported in the present research article. Performance with another switching sequence 0121-7212 is also studied. In this article, inverter output terminals of R, Y and B with suffix '+', '−', '0' representing the respective phase of the inverter output terminal are clamped to the 'positive', 'negative', and 'zero' of input dc bus terminals. Similarly, inverter output terminals R, Y, B with suffix '1', '2' representing 'single', 'double' switching, taking place in the respective phase within sampling time interval.

2.1 Continuous SVPWM

The SV plain (SVP) for a three-level inverter is segmented into the sectors S_1–S_6, as shown in Fig. 1a. In CSVPWM, the only conventional sequence 0127 is implemented in all of the sub-triangles of SVP, as illustrated in Fig. 1a. As a result, continuous switching occurred in each phase of the inverter, as shown in Fig. 1b. If the reference vector (V_{ref}) is revolving with a modulation index (M) of 0.866, the gate signals for the inverter related to the top two switches of one phase are generated, as shown in Fig. 1c.

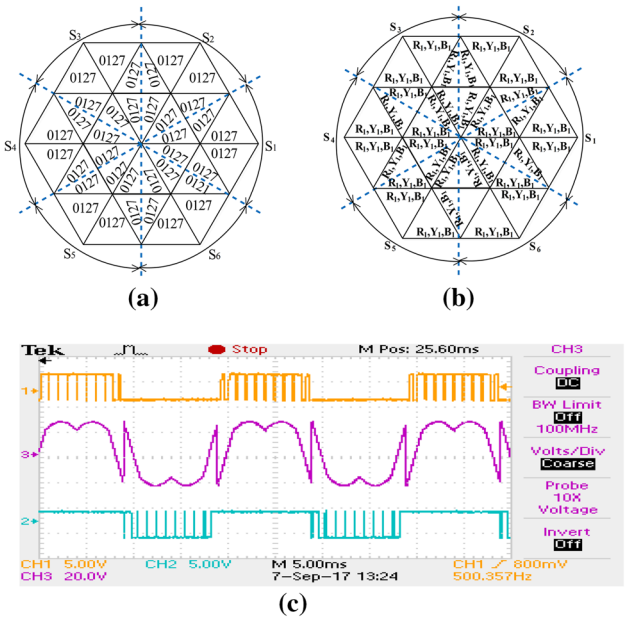

Fig. 1 CSVPWM implementation: **a** sequence applied in each sub-triangle; **b** number of switching's in each phase; and **c** gate signals of the inverter for top two switches of one phase

2.2 ADPWM MIN

In the ADPWM MIN strategy, the sequence of 1012 is implemented in all of the sub-triangles of the SVP, as shown in Fig. 2a. As a result, for the duration of 120^0, the inverter output terminal of each phase is continuously clamped to the negative potential of the input dc bus when M is 0.8666 and the zero potential of the input dc bus for less than 0.4333, as shown in Fig. 2b. In the remaining phases, either single or double switching is taking place irrespective of M. For an M of 0.866, the gate signals generated for the inverter related to the top two switches of one phase are shown in Fig. 2c along with a modulating wave. From Fig. 2c, it is observed that at the same time instant, two switches are continuously engaged in the off state for the duration of 120^0. Therefore, by implementation of this strategy with M of 0.866, each phase of the induction motor stator terminal is continuously clamped for duration of 120^0 to the input dc bus negative voltage.

2.3 ADPWM MAX

In the ADPWM MAX strategy, the sequence of 2721 is implemented in all of the sub-triangles of the SVP, as

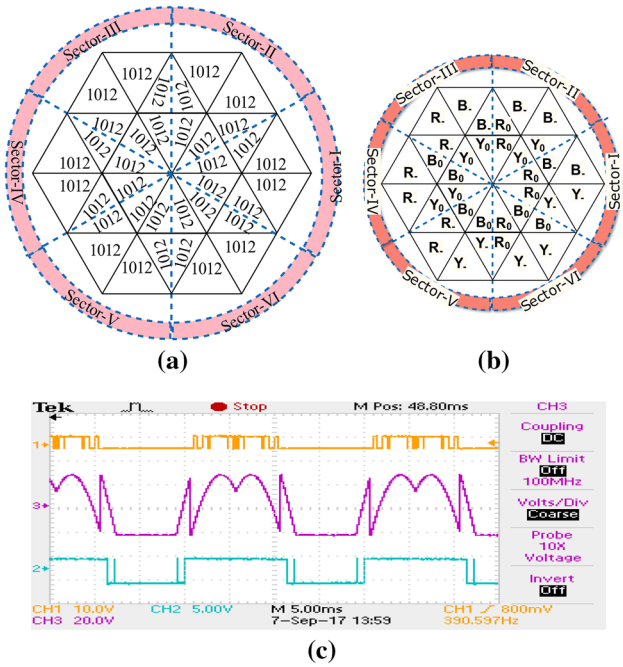

Fig. 2 ADPWM MIN implementation: **a** sequence applied in each sub-triangle; **b** clamping and number of switching's in each phase; and **c** gate signals of the inverter for top two switches of one phase

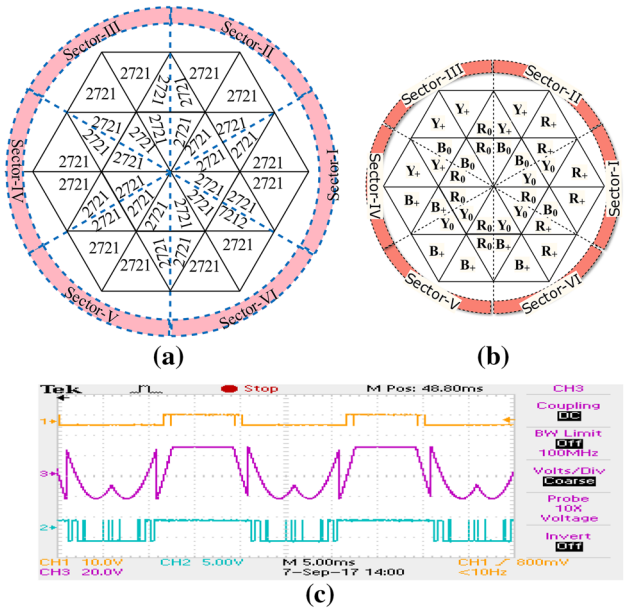

Fig. 3 ADPWM MAX implementation: **a** sequence implemented in each sub-triangle; **b** clamping and number of switching's in each phase; and **c** gate signals of the inverter for top two switches of one phase

shown in Fig. 3a. As a result, for the duration of 120^0, the inverter output terminal of each phase is continuously clamped to the positive potential of the input dc bus when M is 0.8666 and zero potential of the input dc bus for M less than 0.4333, as shown in Fig. 3b. In the remaining phases, either single or double switching occurs irrespective of M. For an M of 0.866, the clamping in the generated gate signals of the inverter related to the top two switches of one phase are shown in Fig. 3c along with a modulating wave. From Fig. 3c, it is observed that two switches are simultaneously engaged in the on state for the duration of 120^0. Therefore, by the implementation of this strategy with an M of 0.866, each phase of the induction motor stator terminal is continuously clamped for the duration of 120^0 to the input dc bus positive voltage. In the ADPWM MIN and the ADPWM MAX approaches, clamping occurs to either the positive or negative bus. As a result, they are called unipolar ADPWM strategies.

2.4 ADPWM 0

From the ADPWM 0 strategy onwards, the combination of the 1012 and 2721 switching sequences are implemented. For this, each sector of the SVP is divided into two zones of Z_1 and Z_2. The sequences 1012 and 2721 are implemented in their respective zones, as shown in Fig. 4a. As a result, for an M of 0.866, each phase of the inverter output terminals is clamped to the input negative terminal for the duration of 60^0 at the end part of the first half cycle, and to the positive terminal for the duration of 60^0 at the end part of the next half cycle, as shown in Fig. 4b. The clamping in the generated gate signals of the inverter related to the top two switches of one phase is shown in Fig. 4c along with a

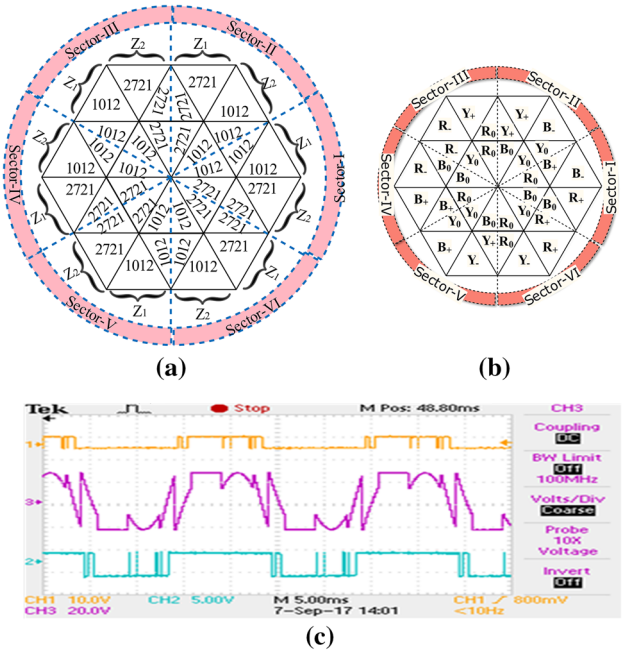

Fig. 4 ADPWM 0 implementation: **a** sequence implemented in each sub-triangle; **b** clamping and number of switching's in each phase; and **c** gate signals of the inverter for top two switches of one phase

modulating wave. From Fig. 4c, it is observed that, by implementation of this strategy, each terminal of the induction motor is clamped to the input negative terminal and positive terminal during the one cycle, each for duration of 60^0.

2.5 ADPWM 2

In the ADPWM 2 strategy, the sequences 1012 and 2721 are implemented, as shown in Fig. 5a. This is a reverse process of ADPWM 0. Through this for an M of 0.866, each terminal of the inverter output is continuously clamped to the input dc bus for the duration of 60^0 in each half cycle, as shown in Fig. 5b. This is similar to that of ADPWM 0. The clamping in the generated gate signals of the inverter related to the top two switches of one phase is shown in Fig. 5c along with a modulating wave. From Fig. 5c, it is observed that the location of the clamping accrued with the ADPWM 2 strategy is different when compared with that of ADPWM 0.

2.6 ADPWM 1

In the ADPWM 1 strategy, the sequences 2721 and 1012 are implemented in odd numbered and even numbered sectors, respectively, as shown in Fig. 6a. Like ADPWM 0 and ADPWM 2, in this strategy, each terminal of the inverter output is clamped to the input dc bus for the duration of 60^0 in each half cycle, as shown in Fig. 6b. The clamping in the generated gate signals of the inverter related to the top

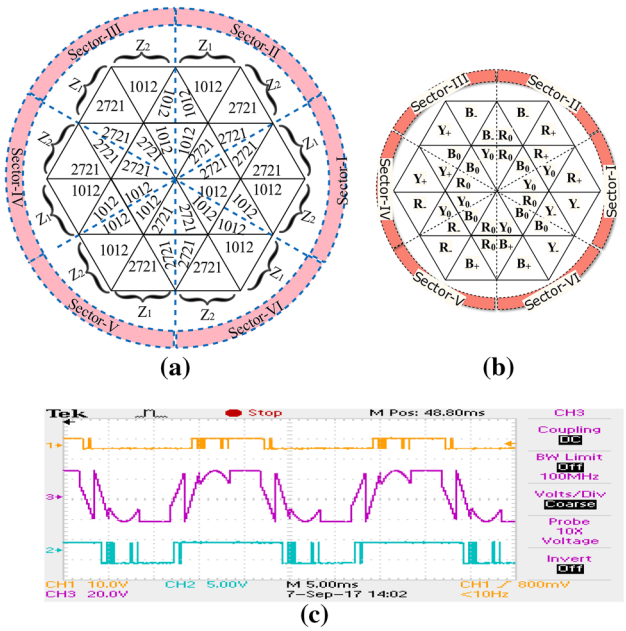

Fig. 5 ADPWM 2 implementation: **a** sequence implemented in each sub-triangle; **b** clamping and number of switching's in each phase; and **c** gate signals of the inverter for top two switches of one phase

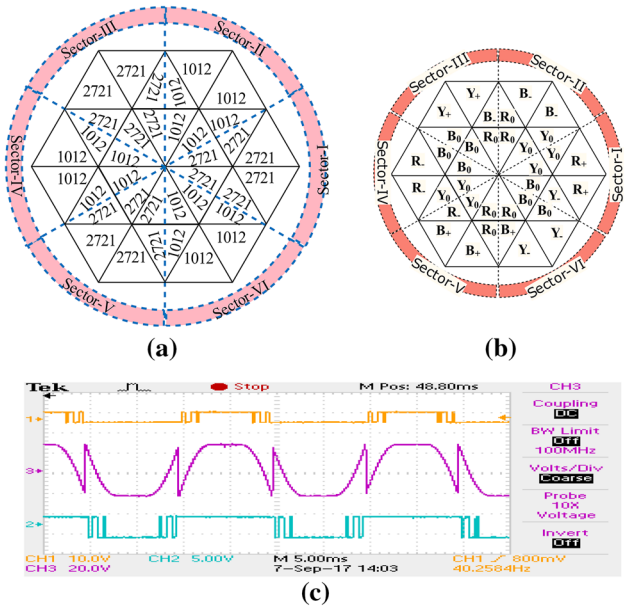

Fig. 6 ADPWM 1 implementation: **a** sequence implemented in each sub-triangle; **b** clamping and number of switching's in each phase; and **c** gate signals of the inverter for top two switches of one phase

two switches of one phase is shown in Fig. 6c along with a modulating wave. From Fig. 6c, it is observed that the location of the clamping accrued with this strategy is in the middle of each half cycle. This is different than the cases of ADPWM 0 and ADPWM 2.

2.7 ADPWM 3

In the ADPWM 3 strategy, the sequences 1012 and 2721 are implemented in the odd number and even number sectors, respectively, as shown in Fig. 7a. In the ADPWM 0, ADPWM 1, and ADPWM 2 strategies, the inverter output is continuously clamped to the input dc bus for the duration 60^0 in each half cycle. In this strategy, split clamping with 30^0 occurs twice in each half cycle, as shown in Fig. 7b. The clamping in the generated gate signals of the inverter related to the top two switches of one phase of the inverter is shown in Fig. 7c. From this, it is observed that the two switches are engaged in the on state for the duration of 30^0 twice in each half cycle.

3 Simulation results

The THD in the line current, voltage, and CMV of a three-level inverter-fed induction motor without filters has been studied through MATLAB simulations. To control the MLI, various unipolar and bipolar DPWM signals have been generated, using a generalized SVM algorithm. Current and voltage THD simulations results obtained for various ADPWM strategies with a combination of the switching

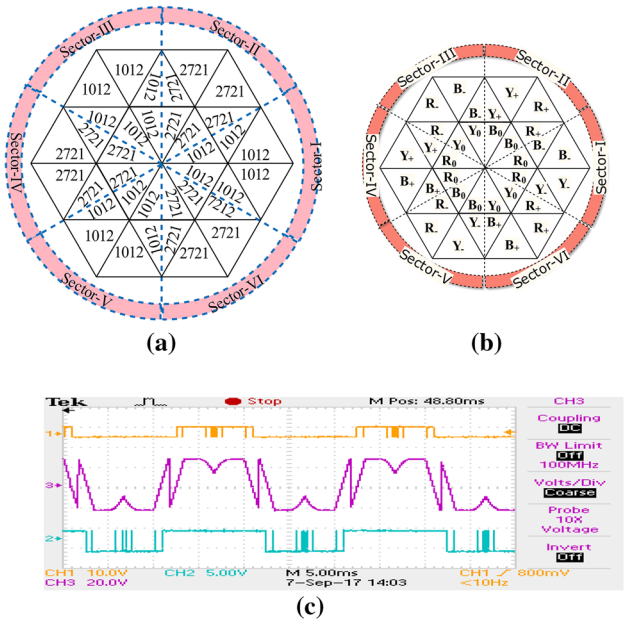

Fig. 7 ADPWM 3 implementation: **a** sequence implemented in each sub-triangle; **b** clamping and number of switching's in each phase; and **c** gate signals of the inverter for top two switches of one phase

sequences 0121-7212 and 1012-2721 are compared with CSVPWM, and presented in Figs. 8 and 9. From these results, it is observed that at a modulation greater than 47.5 Hz, all the ADPWM strategies, at modulation less than 47.5 Hz, and the CSVPWM offered the best performance in terms of current and voltage THD. Among them, the ADPWM-1 strategy gave the best performance. The results obtained with the ADPWM-1 strategy with switching sequences of 0121-7212 and 1012-2721 are compared with those of the CSVPWM. The results are presented in Fig. 10 for a comparison over a frequency range of 15–49.95 Hz. Figure 10a and b compare the motor current and voltage THD at no-load for the conventional sequence 0127 and for the two ADPWM-1 approaches that use a combination of advanced switching sequences. From simulation results, it is observed that the ADPWM-1 approach offers the lowest THD at a higher modulation of 47.5–49.95 Hz through the switching sequence of 0121–7212. Additionally, the magnitude of the CMV produced for a given DC input voltage is studied for various ADPWM strategies. It is observed that the reduction of the CMV is identical to the switching sequences of 0121–7212 and 1012–2721 at a modulation frequency of 49.94 Hz. A comparison of the results from the ADPWM and CSVPWM strategies is presented in Fig. 11.

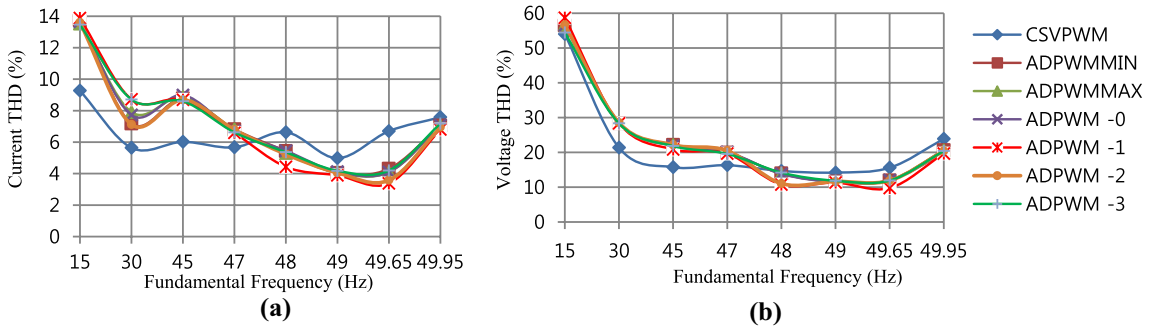

Fig. 8 THD of various ADPWM strategies with a switching sequence of 0121–7212: **a** motor line current; **b** motor line voltage

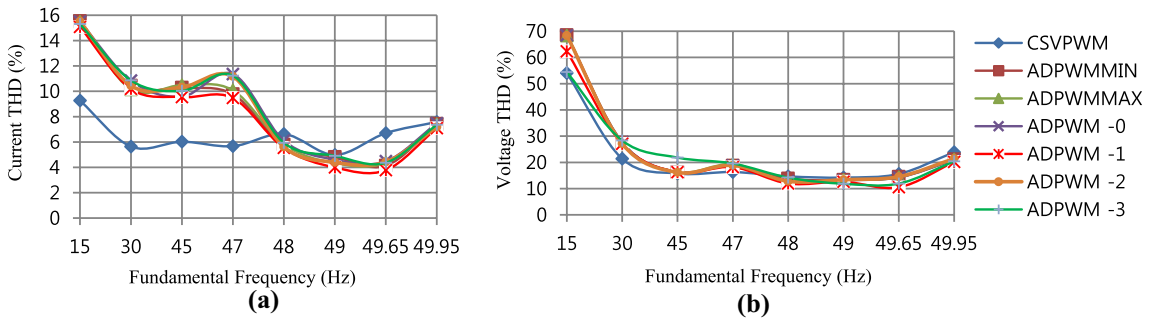

Fig. 9 THD of various ADPWM strategies with a switching sequence of 1012–2721: **a** motor line current; **b** motor line voltage

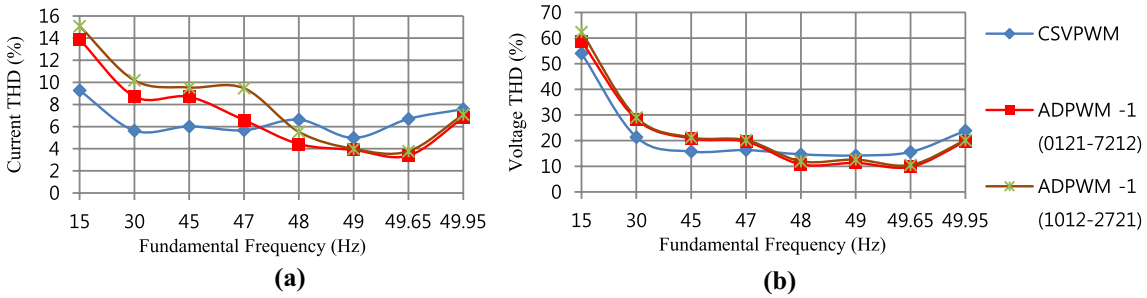

Fig. 10 THD comparison of ADPWM-1 using switching sequences of 1012–2721 and 0121–7212 with a sequence 0127: **a** line current; **b** line voltage

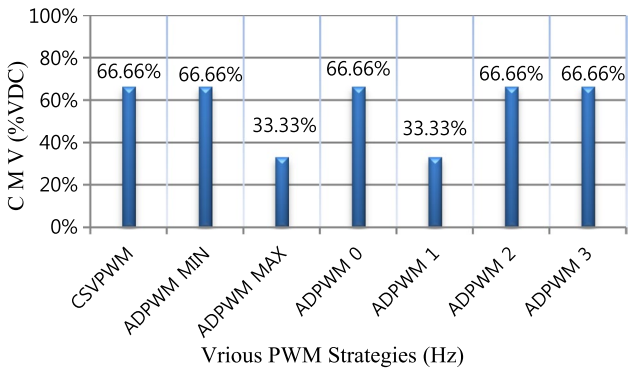

Fig. 11 CMV comparison between various ADPWM and CSVPWM strategies

Table 1 Dominate harmonic order for ADPWM strategies with a switching sequence of 0121–7212

PWM Strategy	Voltage		Current	
	H order	%Mag.	H order	%Mag.
ADPWM MIN	H-37	7.94	H-13	3.57
ADPWM MAX	H-37	7.76	H-13	3.52
ADPWM 0	H-41	10.15	H-13	3.42
ADPWM 1	H-45	9.02	H-13	3.36
ADPWM 2	H-39	9.65	H-13	3.71
ADPWM 3	H-33	9.21	H-13	3.74

Table 2 Dominate harmonic order for ADPWM strategies with a switching sequence of 1012–2721

PWM Strategy	Voltage		Current	
	H order	%Mag.	H order	%Mag.
ADPWM MIN	H-23	7.95	H-15	4.26
ADPWM MAX	H-23	8.62	H-15	4.69
ADPWM 0	H-25	10.60	H-15	5.18
ADPWM 1	H-31	10.41	H-19	3.66
ADPWM 2	H-27	10.21	H-15	4.93
ADPWM 3	H-29	10.62	H-19	6.34

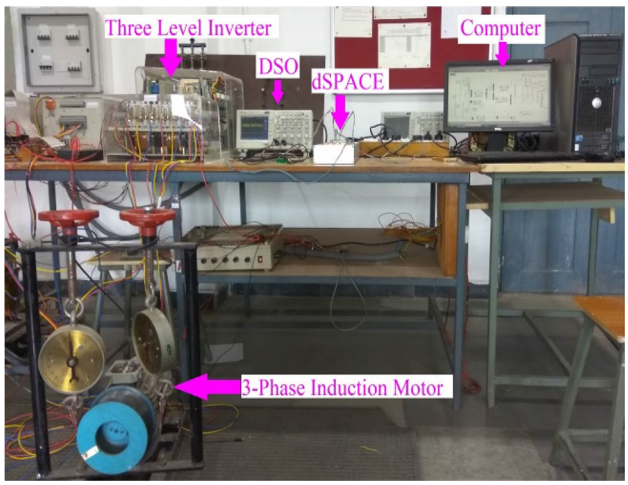

Fig. 12 Experimental setup

From Fig. 11, it is observed that the ADPWM-1 and ADPWM MAX strategies experience a 50% in the CMV when compared to the other strategies, including the CSVPWM. Finally, the dominate harmonic order in the output line voltage and current for various ADPWM strategies with the switching sequences 0121–7212 and 1012–2721 is presented in Tables 1 and 2 at a modulation frequency of 49.95 Hz. The dominate harmonics (H) order in the case of the CSVPWM strategy is 18. It is observed from these results that the ADPWM 1 strategy with switching sequences of 0121-7212 and 1012-2721 produces dominate harmonics at the highest order when compared to other strategies.

4 Experimental results

The performance of a three-level inverter-fed induction motor using a combination of the switching sequences 0121–7212 and 1012-2721 is investigated using dSPACE control desk 1104. The experimental setup is shown in Fig. 12. The results obtained through experiments are captured using a Textronix TDS 2014 C digital storage oscilloscope. The motor current and voltage waveforms at modulation frequencies of 49 Hz and 30 Hz are presented in Figs. 13 and 14, respectively. The reduction of the CMV with the ADPWM 1 strategy when compared with the CSVPWM strategy is presented in Fig. 15.

It is observed that with the ADPWM 1 strategy, there is a 50% reduction in the CMV when compared with the CSVPWM strategy. Comparative experimental results of the line current and line voltage THD at different frequencies are presented in Fig. 16 for the CSVPWM and ADPWM 1 approaches with the sequence 0121-7212. From Fig. 16, it is observed that the ADPWM-1 strategy produces the minimum no-load current ripple at a higher modulation frequency range, 45–49.94 Hz, when compared with the conventional sequence of 0127. The

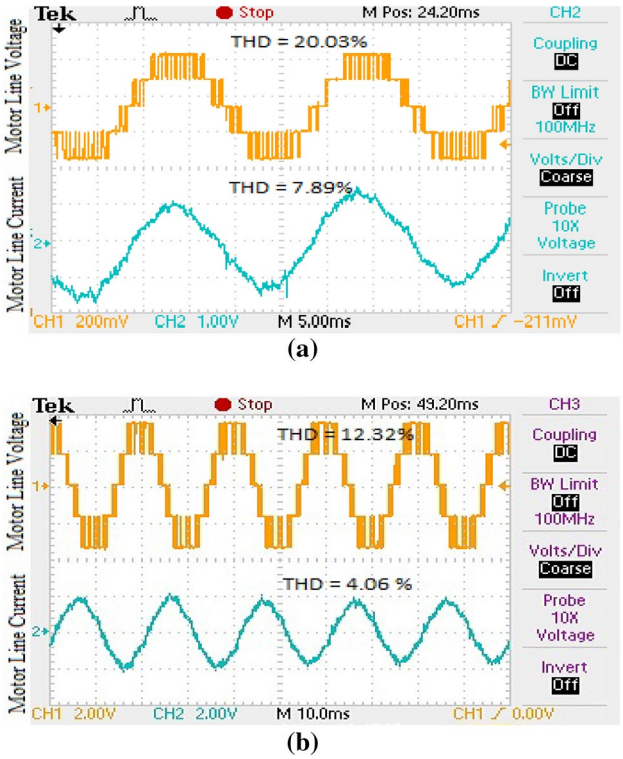

Fig. 13 Line voltage and current performance of a motor at no load for a modulation frequency of 49 Hz: **a** using a switching sequence of 0127; **b** using the ADPWM-1 approach with a switching sequence of 0121-7212

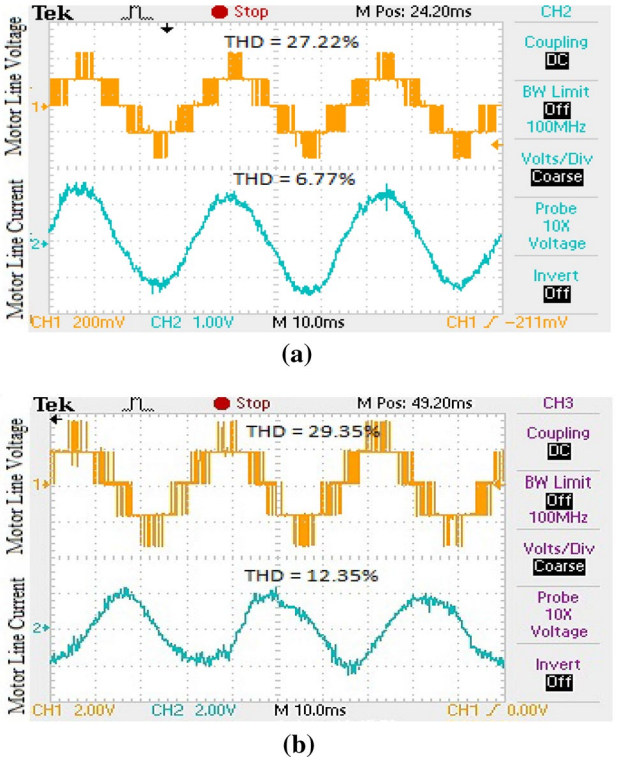

Fig. 14 Line voltage and current performance of a motor at no load for a modulation frequency of 30 Hz: **a** using a switching sequence of 0127; **b** using the ADPWM-1 approach with a switching sequence of 0121–7212

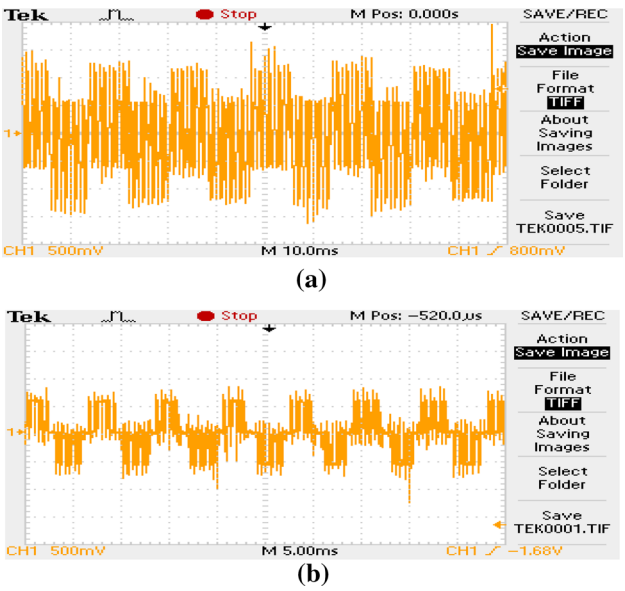

Fig. 15 CMV at a modulation frequency of 49.94 Hz: **a** CSVPWM; **b** ADPWM -1

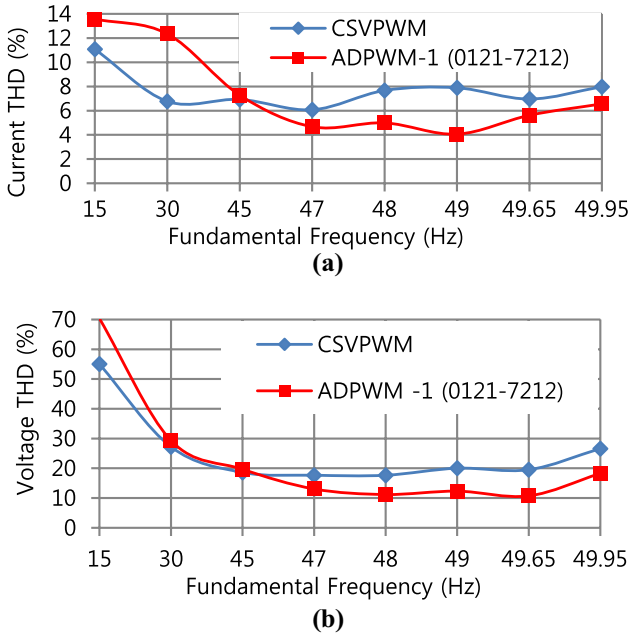

Fig. 16 THD of various ADPWM strategies with a switching sequence of 0121–7212: **a** line current; **b** line voltage

sequence of 0127 gives a better performance at a modulation frequency less than 45 Hz. The experimental results validate the results obtained through simulations.

5 Conclusion

In this paper, the implementation of ADPWM strategies, such as ADPWM MIN, ADPWM MAX, and ADPWM 0 ~ ADPWM 3, using a generalized SVPWM for an MLI is presented. The performance of a three-level inverter-fed induction motor applying ADPWM strategies with two combinational switching sequences of 0121–7212 and 1012–2721 is studied through simulation. The strategy that offered best performance in terms of current and voltage THD through simulation is experimentally confirmed using dSPACE tool. Experimental results of ADPWM-1 strategy based on switching sequence of 0121–7212 are presented and compared with CSVPWM up to the rated frequency range. Based on the simulation and experimental results, we finally concluded that at a higher frequency range of 47.5 Hz to 50 Hz, the ADPWM strategies with a 0121–7212 switching sequence offer a better performance than CSVPWM. In addition, the ADPWM-1 strategy offers the best performance in terms of voltage and current THD when compared with the others, including the conventional strategy. Therefore, fewer filtering components are required.

Appendix

Simulation and experimental parameters.

Parameter	Value
IGBT-based three-level inverter	
Input DC voltage	510 V
Switching frequency	2000 Hz
Filters	No filters
Three-phase induction motor	
Rotor type	Squirrel Cage
Rated power, frequency	1.491 kW, 50 Hz
Speed	1500 RPM
Number of poles	4
Stator resistance and rotor resistance	7.83 Ω, and 7.55 Ω
Stator and rotor leakage reactance	0.4751 H
Magnetizing reactance	0.4535 H
Moment of inertia of the rotor	0.006 kg m^2

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