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ORIGINAL ARTICLE

High Efficiency and Low Complexity Dual-Reference Voltage-Based Pulse Width Modulation for Three-Phase Five-Level HANPC Inverters

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Abstract

This study proposes a low complex and high efficient dual-reference voltage-based pulse width modulation (DRV-PWM) scheme for three-phase five-level hybrid active neutral-point-clamped (HANPC) inverters. Although phase-shifted carrier PWM (PSC-PWM) is capable of naturally balancing dc-link and flying capacitors voltages, such a process requires a tedious and sophisticated adjustment of the phase-shift between the PWM signals, particularly in a digital signal processor (DSP). As a result, a phase-delay eventually occurs, which leads to unevenly distributed thermal losses among the three phases of the five-level HANPC inverter. Therefore, this study introduces an alternative switching scheme that has the same merits as the conventional PSC-PWM in naturally balancing the voltages without requiring voltage sensors. It also balances the thermal losses across the three phases, which enhances the reliability and efficiency of the switching devices. The proposed DRV-PWM is experimentally evaluated in comparison to conventional PSC-PWM on a TMS320F28377S DSP. The experimental results reveal that the proposed DRV-PWM effectively synchronizes the execution of the three-phase pole voltages while also keeping the thermal losses evenly distributed among the three phases.

Keywords Digital signal processor (DSP) · Dual-reference voltage · Five-level hybrid active neutral-point-clamped (HANPC) inverters · Phase shifted carrier pulse width modulation (PSC-PWM) · Thermal losses balancing · Time-delay

1 Introduction

Multilevel converters are widely used in a variety of industrial applications, including those related to renewable energy, motor drives, and power transmission [1–3]. These converters are preferred due to their high power density, good power quality, low *dv*/*dt*, and the low voltage stress they exert on the switching devices [4]. The neutral-point clamped (NPC) inverter is one type of multilevel converter. In contrast to other types of multilevel inverters, such as the flying capacitor and cascaded H-bridge, the NPC inverter does not require flying capacitors or isolated dc-link sources [2]. However, as the number of levels in the output voltage increases, the number of diodes required also increases, which leads to uneven distribution of switching losses and a reduction in the overall efficiency of the inverter.

To address these issues with the NPC inverter, some hybrid variations of the NPC inverter have been proposed and implemented in industries. One such variation is the five-level active NPC (ANPC) inverter, which was first introduced in 2005 [5], then commercialized by ABB in 2010 in their 800 kW 6 kV transformer-less ACS 2000 drive [6]. This type of inverter is popular due to the fact that it requires fewer active switching devices and capacitors. It is an extension of the three-level hybrid ANPC (HANPC) inverter [7–10] and incorporates an additional two active switches and one flying capacitor per phase (C_{fx}).

As shown in Fig. 1, this design utilizes three different cells: *Cell-I*, *Cell-II*, and *Cell-III*. Si IGBT switching devices are employed in *Cell-I* whereas SiC MOSFET switching devices are used in *Cell-II* and *Cell-III*; this is intended to achieve better performance in the high

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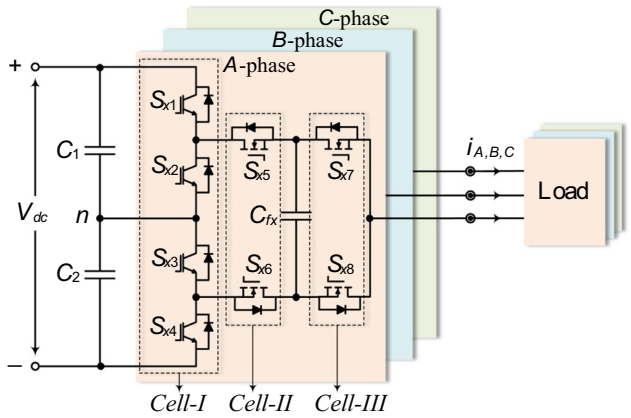

Fig. 1 Circuit topology of a three-phase five-level HANPC inverter feeding a three-phase load

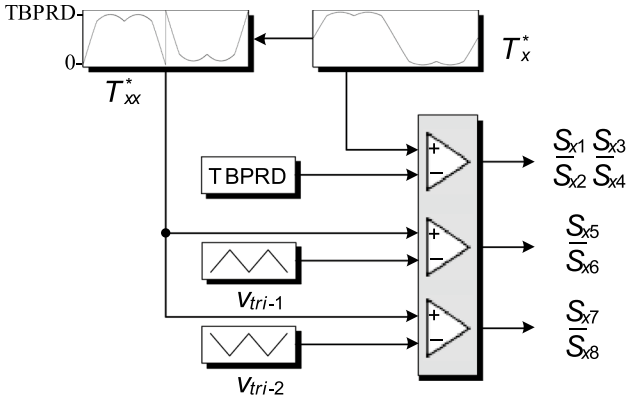

Fig. 2 Block diagram of conventional PSC-PWM for five-level HANPC inverter

switching frequency (f_{sw}) range. Using all SiC MOSFETs in the five-level inverter design would significantly increase the cost while only slightly improving system performance. On the other hand, if all Si IGBTs were to be used, then the cost would decrease but the performance would deteriorate at high f_{sw} range. Therefore, the criteria for this arrangement are a balance between effective performance, reliability, and cost [11].

Prior studies have presented several modulation techniques that can be used to control the five-level HANPC inverter, including selective harmonics elimination pulse width modulation (SHE-PWM) [12], phase disposition carrier PWM (PDC-PWM) [13], and phase shifted carrier PWM (PSC-PWM) [14]. While the SHE-PWM technique is capable of balancing the voltage across the C_{fx}, it is complex and requires a predefined lookup table to store as many voltage control angels as possible to reduce output voltages and currents total harmonic distortion (THD) [15]. This process could result in a slow response control of the inverter and increase its complexity. On the other hand, although PDC-PWM offers fast response control with low computational requirements compared to SHE-PWM, it leads to a more distorted output voltage due to non-uniformly distributed switching and conducting losses [16].

The PSC-PWM modulation technique is effective in balancing the flying capacitor voltages in comparison to the PDC-PWM technique, but it requires two inverted PWM carriers, $v_{tri\text{-}1}$ and $v_{tri\text{-}2}$, to create the five-level output pole voltage v_{xn}, as shown in Figs. 2 and 3. Table 1 presents the eight possible voltage states of the five-level HANPC inverter, which can be controlled by the switching mechanism of the PSC-PWM modulation technique. As a result, natural voltage balancing is achieved in dc-link capacitors C_1 and C_2 at $V_{dc}/2$, and C_{fx} at $V_{dc}/4$, where x represents A-, B-, or C-phase. Nevertheless, implementing PSC-PWM modulation technique on a digital signal processor (DSP) is a challenging task due to the need to compensate for the time-delay ($T_{d,PWM}$) caused by the PWM modulator [17].

Recently, a few studies have addressed the issue mentioned above regarding $T_{d,PWM}$ [18–27]. For example, in [20], the authors proposed a synchronized PSC-PWM for a cascaded H-bridge multilevel inverter. Although this approach results in reduced f_{sw} and switching losses, it suffers from undesirable uncontrolled and noneliminated harmonics. Another approach involves using compensatory techniques such as lead-lag compensators and predictive control [17, 26, 27]. However, these methods are limited in their ability to effectively compensate for computation delay. For example, the lead-lag compensator has been found to only achieve limited compensation effects, and to amplify high-frequency noise. Meanwhile, predictive control relies on past information and the plant model to estimate future information, and it is therefore susceptible to model errors caused by changes in circuit parameters, which can lead to prediction bias and negatively impact control performance and system stability.

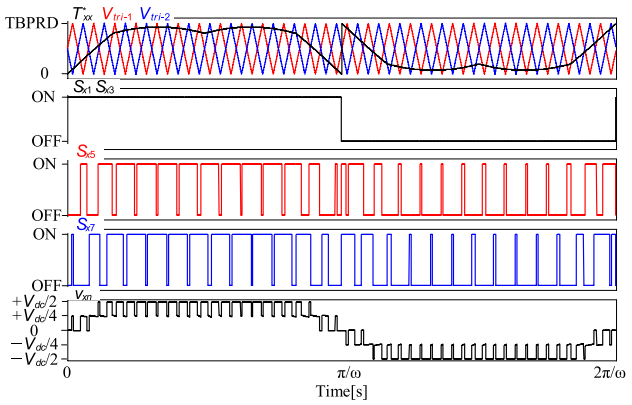

Fig. 3 Demonstration of conventional PSC-PWM for generating a five-level v_{xn}

Table 1 Eight switching states of five-level HANPC inverter using PSC-PWM switching scheme

Voltage state	S_{x1} S_{x3}	S_{x2} S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	v_{xn}
v_1	ON	OFF	ON	OFF	ON	OFF	$V_{dc}/2$
v_2	ON	OFF	ON	OFF	OFF	ON	$V_{dc}/4$
v_3	ON	OFF	OFF	ON	ON	OFF	$V_{dc}/4$
v_4	ON	OFF	OFF	ON	OFF	ON	0
v_5	OFF	ON	ON	OFF	ON	OFF	0
v_6	OFF	ON	ON	OFF	OFF	ON	$-V_{dc}/4$
v_7	OFF	ON	OFF	ON	ON	OFF	$-V_{dc}/4$
v_8	OFF	ON	OFF	ON	OFF	ON	$-V_{dc}/2$

Moreover, PWM methods have gained attention as a mean of compensating for computation delay [20, 23, 24]. By moving the sampling instant closer to the PWM loading instant, the computation delay can be reduced substantially. Nevertheless, this approach can still introduce aliasing and switching noise problems. Asymmetric PWM is another method that has been shown to effectively compensate for computation delay, but it may limit the variable range of duty ratios and introduce extra harmonics. Moreover, real-time compensation with dual sampling mode and real-time loading has been proposed as a means of completely eliminating computation delay [18, 22]; however, this method is currently only applicable to single-phase converters due to its reliance on unipolar and frequency-doubling modulation.

Multisampling PWM techniques have been used in recent years to address computation delay in various applications [19]. However, despite their popularity in DSP platforms, multisampling technology has several key issues, such as switching noise, nonlinearities, and vertical crossing DSPs, which may affect the overall performance of the system. In addition, methods such as digital-filter-based delay compensation, including high-pass filter, Smith predictor, and linear predictor, have been proposed, but the compensation effect is limited in the high-frequency range, and high-frequency noise may even be amplified [21].

Therefore, the present paper proposes a low complexity and high efficiency dual-reference voltage-based pulse width modulation (DRV-PWM) scheme as an alternative control scheme for three-phase five-level HANPC inverters. The DRV-PWM does not require sophisticated phase adjustments to achieve a desirable control of this topology without $T_{d,PWM}$. Instead, it simplifies the control structure without requiring two PWM carriers. Hence, its implementation on a DSP is less complex, and it does not require the PWM phase tuning between *Cell-II* and *Cell-III*. As a result, it is achievable to have balanced losses distributions among the three phases of the five-level HANPC inverter due to the elimination of $T_{d,PWM}$. Further, switching devices could have higher reliability, and overall efficiency would increase. This is demonstrated by sets of experimental trials comparing the operation of the inverter under the conventional PSC-PWM and proposed DRV-PWM.

The rest of this paper is organized as follows. Section II presents the switching scheme and the limitations of the conventional PSC-PWM technique. Section III introduces the proposed DRV-PWM method. Section IV provides information on the intensive experimental verifications that were conducted. Finally, Section V presents the conclusions of this study.

2 Conventional PSC-PWM and its Limitations

2.1 Switching Scheme

Unlike other modulation schemes that are used to control the five-level HANPC inverter, the PSC-PWM can be considered one of the best candidates due to its robust and natural ability to balance the voltage across C_1 and C_2 at $V_{dc}/2$ and C_{fx} at $V_{dc}/4$. The switching losses are also evenly distributed among the switching devices. Figure 3 shows a demonstration diagram of the conventional PSC-PWM. For clarity of the switching mechanism of the conventional PSC-PWM, f_{sw} has been set at 1.3 kHz. As can be seen from Fig. 2, the process of generating the switching states for the Si-IGBT S_{x1}–S_{x4} and SiC-MOSFET S_{x5}–S_{x8} are processed according to the fundamental frequency or line frequency (f_o) of 50 Hz for each phase.

To begin, the three phases' reference voltages v^*_{xs} can be expressed as shown in (1),

$$\begin{cases} v^*_{As} = v_m \cdot \sin\left(2\pi f_o t\right), \\ v^*_{Bs} = v_m \cdot \sin\left(2\pi f_o t - \dfrac{2\pi}{3}\right), \\ v^*_{Cs} = v_m \cdot \sin\left(2\pi f_o t + \dfrac{2\pi}{3}\right), \end{cases} \tag{1}$$

where v_m represents the voltage magnitude, which corresponds to *MI*.

Secondly, the pole voltage (v^*_{xn}) needs to be generated by injecting a zero-sequence signal (v^*_{sn}) to extend the *MI* to ($2/\sqrt{3} \approx 1.15$), which improves the THD characteristics of the load current and reduces the switching losses [28]. v^*_{sn} can be calculated by considering the absolute values of the maximum and minimum reference voltages v^*_A, v^*_B, and v^*_C, respectively, as in (2),

$$v^*_{sn} = -\left(\frac{\max\left\{v^*_{As}, v^*_{Bs}, v^*_{Cs}\right\} + \min\left\{v^*_{As}, v^*_{Bs}, v^*_{Cs}\right\}}{2}\right). \quad (2)$$

Due to the nature of the three-phase system, v^*_{sn} is switching f_o three times. Therefore, v^*_{xn} can be expressed as in (3),

$$v^*_{Xn} = v^*_{Xs} + v^*_{sn} \quad (3)$$

To effectively simplify the algorithm of conventional PSC-PWM, v^*_{xn} needs to be normalized while considering V_{dc} as expressed in (4),

$$T^*_x = \left[1 + \left(\frac{2 \times v^*_{xn}}{V_{dc}}\right)\right] \times \text{TBPRD}, \quad (4)$$

where TBPRD is the time-based period peak value of PWM counter in the DSP. The next step is to convert T^*_x into T^*_{xx} as depicted in the block diagram in Fig. 2. This process could reduce the number of the required PWM carriers to half of the original number. T^*_{xx} can be calculated as shown in (5),

$$T^*_{xx} = \begin{cases} T^*_x - \text{TBPRD}, & T^*_x \geq \text{TBPRD}, \\ T^*_x, & T^*_x < \text{TBPRD}, \end{cases} \quad (5)$$

To satisfy the requirements for generating five-level output v_{xn}, two PWM triangular carriers, $v_{tri\text{-}1}$ and $v_{tri\text{-}2}$, need to be included in the structure of the switching scheme with a 180° phase-shift, as shown in Fig. 3. The switching principle for S_{x1}–S_{x4} in *Cell-I* depends on T^*_x. This means they are switching at f_o. Hence, the switching rules are given by (6),

$$S_{x1}, S_{x3}, \overline{S}_{x2}, \text{ and } \overline{S}_{x4} = \begin{cases} \text{ON}, & T^*_x \geq \text{TBPRD}, \\ \text{OFF}, & T^*_x < \text{TBPRD}. \end{cases} \quad (6)$$

By contrast, *Cell-II* and *Cell-III* turn ON and OFF in a complementary manner, when comparing T^*_{xx} with $v_{tri\text{-}1}$ and $v_{tri\text{-}2}$, respectively, as expressed in (7),

$$\begin{aligned} S_{x5} \text{ and } \overline{S}_{x6} &= \begin{cases} \text{ON}, & T^*_{xx} \geq V_{tri-1}, \\ \text{OFF}, & T^*_{xx} < V_{tri-1}, \end{cases} \\ S_{x7} \text{ and } \overline{S}_{x8} &= \begin{cases} \text{ON}, & T^*_{xx} \geq V_{tri-2}, \\ \text{OFF}, & T^*_{xx} < V_{tri-2}. \end{cases} \end{aligned} \quad (7)$$

However, this scheme results in a generation of v_{xn} with balanced voltage across C_{fx} as well as C_1 and C_2, and the implementation process for a three-phase five-level HANPC inverter is going to be complicated due to the need to generate the switching signals from a single DSP without $T_{d,PWM}$.

2.2 Limitations of Implementing PSC-PWM on DSPs

It should be noted that the three-phase five-level HANPC inverter requires twenty-four switching signals. Therefore, it is excessively complicated to generate those switching signals from a single DSP due to the limitation of PWM channels and/or other factors such as synchronization process. As a result, a twenty-four PWM-channel single DSP TMS320F28377S from Texas Instruments [29] is selected to perform the execution of the control algorithm. Although this DSP provides switching for all switching devices of the three-phase five-level HANPC inverter, the synchronization process between *Cell-II* and *Cell-III* is complex, as shown in Fig. 4. There is also a delay due to the implementation process, as shown in Fig. 5.

To implement the synchronization process to maintain the same switching principle of generating interleaved PWM carriers, as shown in Fig. 5, there is a need to eliminate the $T_{d,PWM}$, which is a challenging task. It is necessary to have interrupt signals for $v_{tri\text{-}1}$ and $v_{tri\text{-}2}$ to ensure the same switching scheme as the conventional PSC-PWM

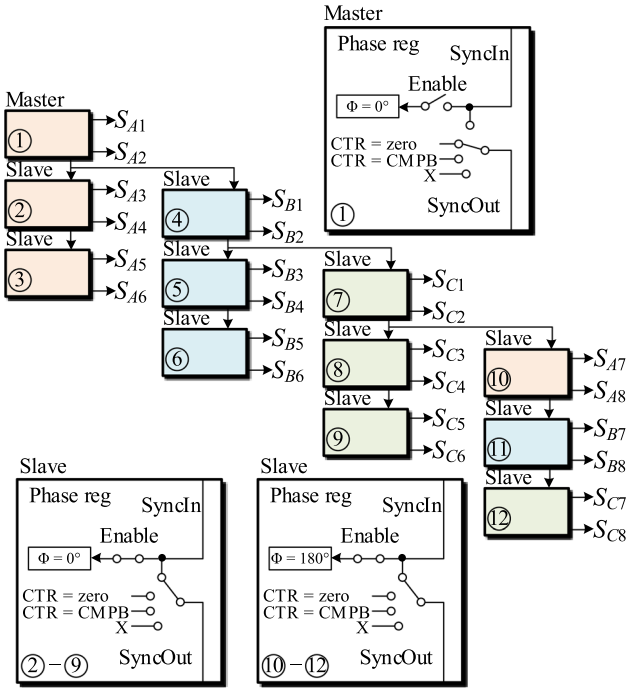

Fig. 4 Structural scheme of conventional PSC-PWM based on time-base counter synchronization for three-phase five-level HANPC inverter

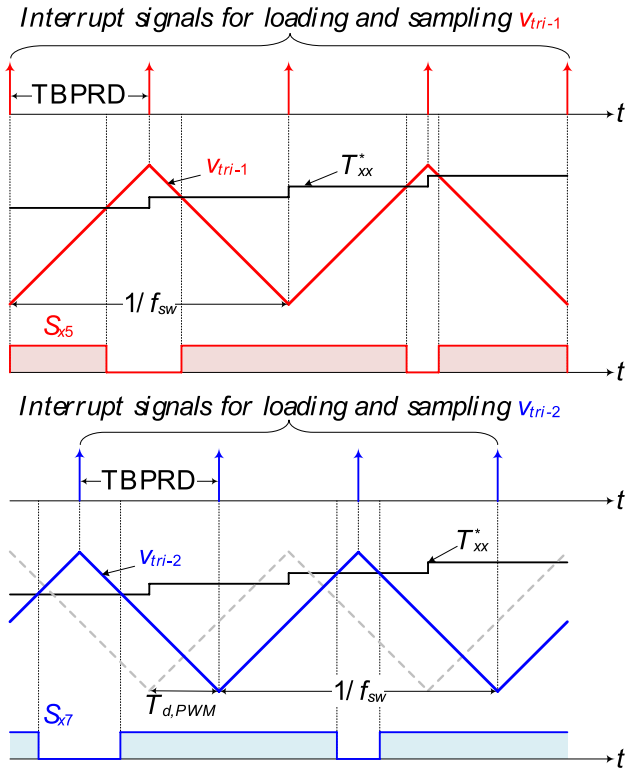

Fig. 5 Implementation scheme of conventional PSC-PWM based on time-base counter synchronization for *Cell-II* and *Cell-III* of five-level HANPC inverter. A half-dash-gray carrier, which is 180° phase shifted with respect to $v_{tri\text{-}1}$, highlights how $T_{d,PWM}$ affects the switching scheme

method. To satisfy this condition, dual-synchronization is implemented as shown in Fig. 4. The first synchronization is related to $v_{tri\text{-}1}$, while the second one is for $v_{tri\text{-}2}$. Updating those interrupt signals twice at the same time creates a time delay, which results in undesirable switching that does not satisfy the control of the five-level HANPC inverter.

3 Proposed DRV-PWM

3.1 Proposed Switching Scheme

Due to the limitations of the conventional PSC-PWM presented in the previous section, there is a need for an effective yet less complex alternative control algorithm for the five-level HANPC inverter. The proposed switching scheme is based on generating dual-reference voltage signals $T^*_{xx\text{-}1}$ and $T^*_{xx\text{-}2}$ to avoid the complexity involved in implementing the conventional PSC-PWM in a single DSP. $T^*_{xx\text{-}1}$ and $T^*_{xx\text{-}2}$ are both extracted simultaneously from (5), as shown in Fig. 6, and expressed mathematically as shown in (8),

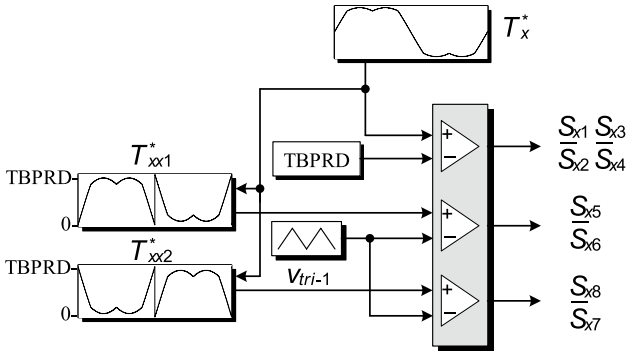

Fig. 6 Block diagram of proposed DRV-PWM for five-level HANPC inverter

$$T^*_{xx-1} = \begin{cases} T^*_x - \text{TBPRD}, & T^*_x \geq \text{TBPRD}, \\ T^*_x, & T^*_x < \text{TBPRD}, \end{cases}$$
$$T^*_{xx-2} = \begin{cases} \text{TBPRD} - T^*_{xx-1}, & T^*_x \geq \text{TBPRD}, \\ \text{TBPRD} - T^*_x, & T^*_x < \text{TBPRD}. \end{cases} \quad (8)$$

The proposed DRV-PWM approach maintains a similar switching principle achieved by (6) for *Cell-I* due to switching at f_o. However, *Cell-II* and *Cell-III* are turning ON and OFF at f_{sw} in a complementary manner by comparing $T^*_{xx\text{-}1}$ and $T^*_{xx\text{-}2}$ with only one triangular carrier, $v_{tri\text{-}1}$, as expressed in (9),

$$S_{x5} \text{ and } \overline{S}_{x6} = \begin{cases} \text{ON}, & T^*_{xx-1} \geq V_{tri-1}, \\ \text{OFF}, & T^*_{xx-1} < V_{tri-1}, \end{cases}$$
$$S_{x5} \text{ and } \overline{S}_{x6} = \begin{cases} \text{ON}, & T^*_{xx-2} \geq V_{tri-1}, \\ \text{OFF}, & T^*_{xx-2} < V_{tri-1}. \end{cases} \quad (9)$$

This process satisfies the requirements for operating the five-level HANPC inverter without the need for two PWM carriers or complex phase shift tuning inside the DSP. The new switching states generated by the proposed DRV-PWM are tabulated in Table 2.

3.2 Implementation on DSPs

Regardless of the advancements that have been achieved in DSPs used to controlling the three-phase five-level hybrid active NPC inverter, it is necessary to support twenty-four PWM channels. The proposed DRV-PWM does not require any phase-shift tuning between *Cell-II* and *Cell-III* of this topology, as shown in Fig. 7. Moreover, the reference voltages are designed alternatively to achieve the desired five-level v_{xn} without any abnormal distortion among the three phases. It is worth noting that the switching signals sent to *Cell-III* do not require any phase-shifting or time-based synchronization;

Table 2 Eight switching states of five-level HANPC inverter using proposed DRV-PWM switching scheme

Voltage state	S_{x1} S_{x3}	S_{x2} S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	v_{xn}
v_2	ON	OFF	ON	OFF	OFF	ON	$V_{dc}/2$
v_1	ON	OFF	ON	OFF	ON	OFF	$V_{dc}/4$
v_4	ON	OFF	OFF	ON	OFF	ON	$V_{dc}/4$
v_3	ON	OFF	OFF	ON	ON	OFF	0
v_6	OFF	ON	ON	OFF	OFF	ON	0
v_5	OFF	ON	ON	OFF	ON	OFF	$-V_{dc}/4$
v_8	OFF	ON	OFF	ON	OFF	ON	$-V_{dc}/4$
v_7	OFF	ON	OFF	ON	ON	OFF	$-V_{dc}/2$

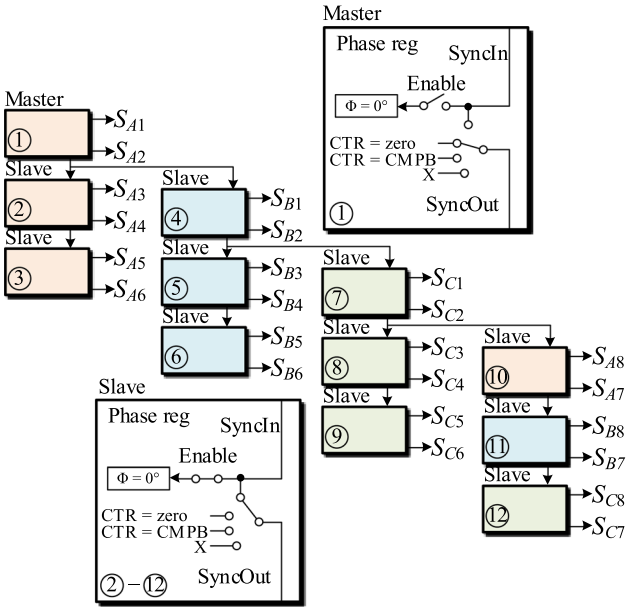

Fig. 7 Structural scheme of proposed DRV-PWM based on time-base counter synchronization for three-phase five-level HANPC inverter. There is no need to include phase-shift algorithm or sophisticated phase tuning

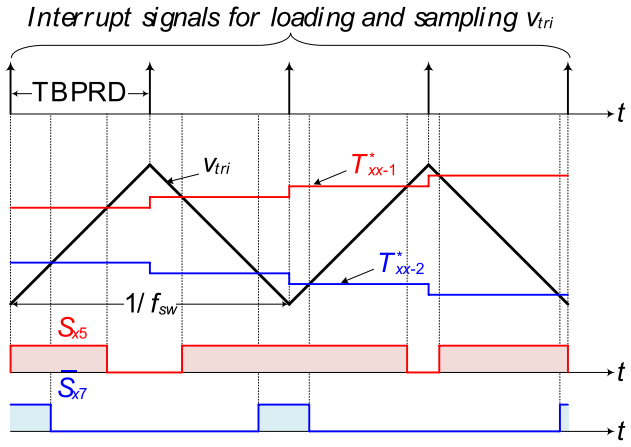

Fig. 8 Implementation scheme of proposed DRV-PWM based on time-base counter synchronization for *Cell-II* and *Cell-III* of five-level HANPC inverter with elimination of $T_{d,PWM}$

instead, $T^*_{xx\text{-}2}$ is compared with $v_{tri\text{-}1}$ as indicated in (9) and shown in Fig. 8, so a simple hardware implementation is achieved.

Further, Fig. 8 shows a time-based implementation of the proposed DRV-PWM. Unlike the conventional PSC-PWM, the interrupt signals for loading and sampling the switching signals for *Cell-II* and *Cell-III* required to implement the proposed DRV-PWM are less complex. This process simplifies the whole system and eliminates the $T_{d,PWM}$ that might appear during the generation of S_{x5}–S_{x8}.

4 Experimental Results and Discussion

4.1 Experimental Hardware Setup

To verify the effectiveness of the proposed DRV-PWM for a three-phase five-level hybrid active NPC inverter, the experimental hardware setup shown in Fig. 9 is used. It consists of a combination of three cells, control, and power parts. *Cell-I* consists of six Si IGBT module (SK75GB-BB066T), developed by SEMIKRON, where each module consists of four Si IGBT devices and their gate drives. The other two cells (i.e., *Cell-II* and *Cell-III*) contain the SiC MOSFET (C2M0040120D) developed by CREE. It is worth noting that there is one C_{fx} per phase, which is connected in parallel between *Cell-II* and *Cell-III*. The type of C_{fx} is selected to be a film capacitor type to handle high f_{sw} with lower capacitance ratings than electrolytic capacitors [11].

In the control part, a single TMS320F28377S DSP board is used as a control board, which is supplied by a 5 V DC power supply. There are also two boards connected

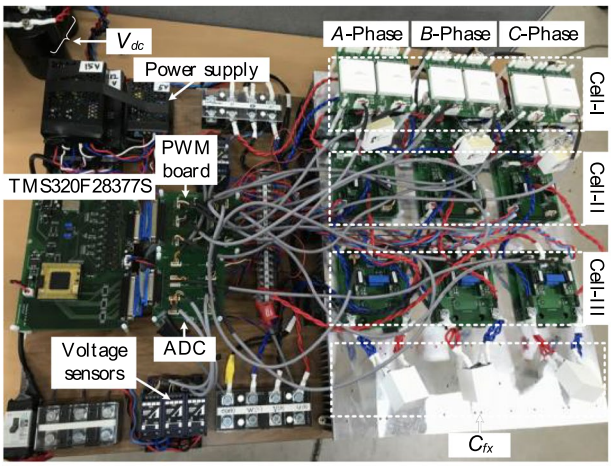

Fig. 9 Experimental setup of hardware

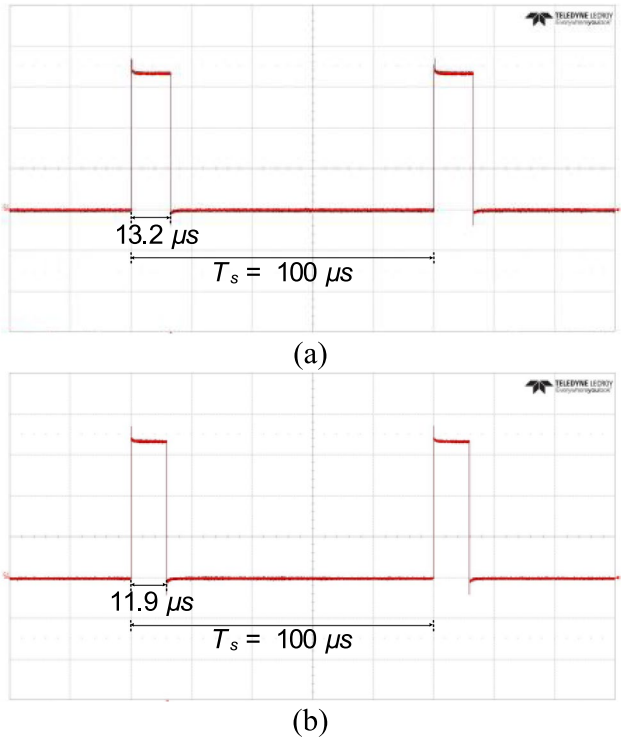

Fig. 10 Hardware execution time of PWM control method: **a** Conventional PSC-PWM; **b** Proposed DRV-PWM

to the DSP board and used for the PWM signals and the analogue-to-digital converter (ADC). In the power part, C_1 and C_2 are used to smooth the DC power supplied to the inverter and connected to two voltage sensors that send their signals to the ADC and then on to the DSP control board. The complete list of experimental specifications is presented in Table 3. To achieve high f_{sw} at 30 kHz, TBPRD is denoted as expressed in (10),

$$\text{TBPRD} = \frac{EPWMCLK \times T_{PWM}}{2} = \frac{100\ \text{MHZ}}{2 \times 30\ \text{kHz}} = 1667. \tag{10}$$

where *EPWMCLK* is the maximum clock used for EPWM in the TMS320F28377S DSP [29].

4.2 Hardware Execution Time of Conventional and Proposed Methods

The experimental results of hardware execution time for the conventional PSC-PWM and proposed DRV-PWM techniques are shown in Fig. 10. It can be seen from the figure that the proposed DRV-PWM requires less computational time than the conventional PSC-PWM. This difference is not substantial, because the TMS320F28377S DSP is an advanced microcontroller, which includes some predefined functions such as *TBPHS* for setting the phase-shift. However, there is still a $T_{d,PWM}$ because of the sophisticated tuning of the phase-shift between the three-phases, particularly in *Cell-II* and *Cell-III*, as illustrated in the aforementioned section.

The proposed DRV-PWM has the merits of maintaining the simplicity of the hardware coding for generating the switching signals. As explained in the previous section, the proposed method does not require any complex phase-shift tuning between *Cell-II* and *Cell-III* to achieve the desired output signals to construct v_{xn}. Conversely, the conventional technique requires an additional coding to create a phase-shift between the switching signals sent to *Cell-II* and *Cell-III*. This increases the system complexity and restricts its flexibility from executing other functions properly. Undesirable switching signals are also present in the output waveforms.

Table 3 Experimental specifications

Parameter	Value	Unit
V_{dc}	300	V
$C1 = C2$	4700	μF
C_{fx}	30	μF
R	10	Ω
L	2	mH
f_o	50	Hz
T_s	100	μs
TBPRD	1667	–
f_{sw}	30	kHz

4.3 Comparative Experimental Results of Conventional PSC-PWM and Proposed DRV-PWM

Figure 11 shows the experimental validation of the conventional and proposed switching techniques when *MI* is 1.15.

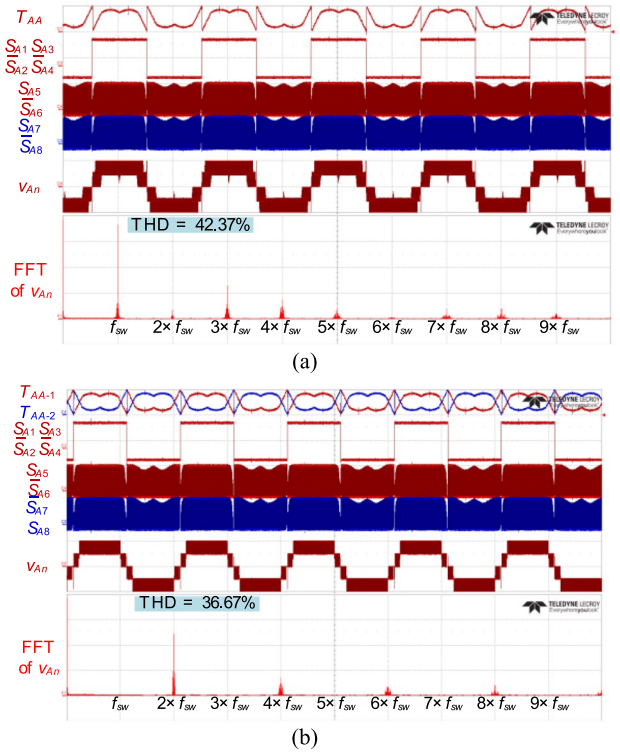

Fig. 11 Experimental results of generating v_{An}: **a** Conventional PSC-PWM; **b** Proposed DRV-PWM

In Fig. 11a, it can be seen that the conventional PSC-PWM can be implemented with sophisticated tuning of phase-shift among switching signals to achieve a similar form of v_{xn} with undesirable switching that leads to high distortion in v_{xn}. Nevertheless, the proposed DRV-PWM solves the issue of $T_{d,PWM}$ as shown in Fig. 11b. This results in less distorted v_{xn} with a 5.7% improvement in the THD, as can be clearly seen from the fast Fourier transform (FFT) analysis of v_{xn} in Fig. 11a and b for the conventional and proposed switching methods, respectively.

Other sets of experimental results are given in Figs. 12 and 13 for the conventional and proposed techniques, respectively. These results show the three-phase output voltage and current waveforms. It can be seen from these figures that the conventional PSC-PWM suffers from $T_{d,PWM}$ issue, which results in asynchronous switching. This leads to higher voltage stress on some switching devices, which in turn degrades system reliability. Meanwhile, the proposed DRV-PWM generates a synchronous output voltage and current waveforms as desired. Moreover, the results shown in Fig. 14a highlight the effects of $T_{d,PWM}$ in disturbing the switching signals in the difference phases, where it can be seen that the A phase has clearer effects as the peaks of the $v_{tri\text{-}1}$ and $v_{tri\text{-}2}$ and other PWM signals are generated with respect to it, as shown in Fig. 4. The black-line triangular in this figure is magnified in Fig. 15a. In addition, the area near zero crossing (i.e., circle black-line area) also showed the disturbance on the switching signals and output v_{xn}. The proposed method effectively eliminates the effects of the uneven losses distribution and

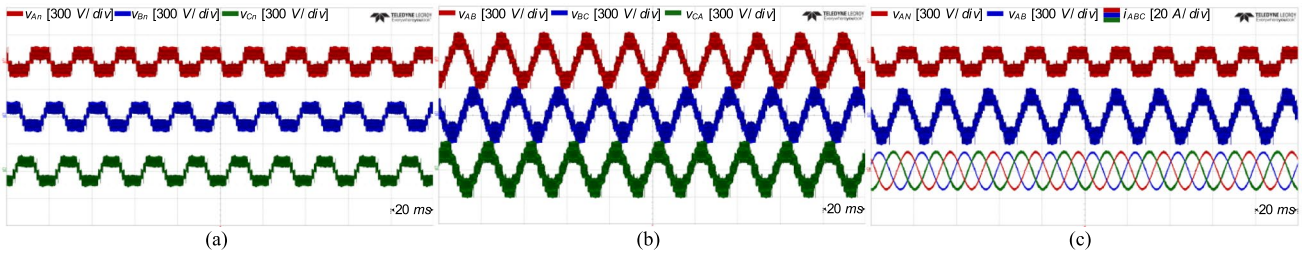

Fig. 12 Experimental results of conventional PSC-PWM: **a** Three-phase pole voltages; **b** Three-phase line-to-line voltages; **c** Output voltages and three-phase currents

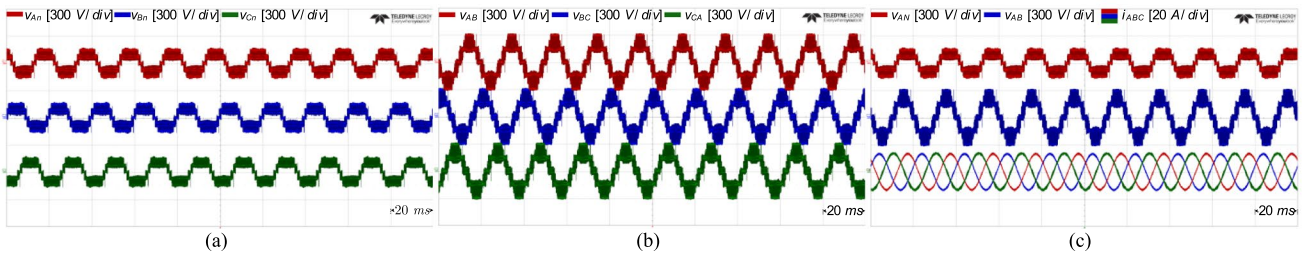

Fig. 13 Experimental results of proposed DRV-PWM: **a** Three-phase pole voltages; **b** Three-phase line-to-line voltages; **c** Output voltages and three-phase currents

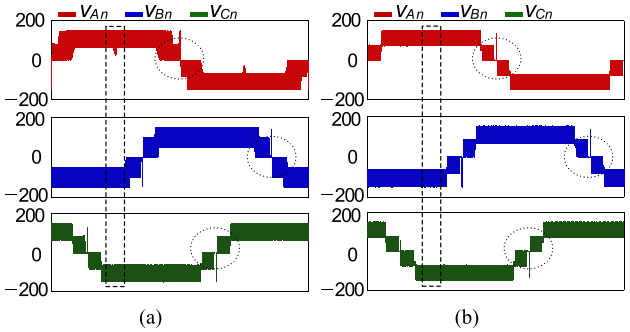

Fig. 15 Experimental magnified results of $T_{d,PWM}$ effects on v_{xn}: **a** Conventional PSC-PWM; **b** Proposed DRV-PWM

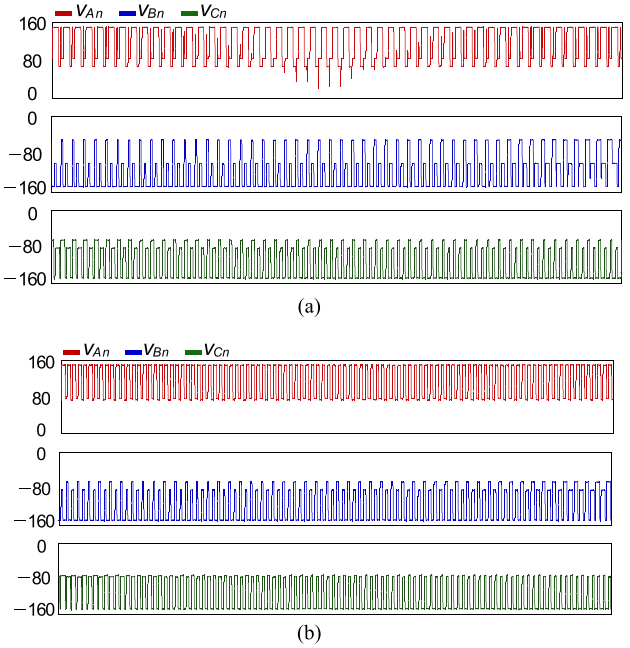

Fig. 14 Experimental results of $T_{d,PWM}$ effects on v_{xn}: **a** Conventional PSC-PWM; **b** Proposed DRV-PWM

PWM switching signals as shown in Figs. 14b and 15b, respectively. Thus, voltage stress and losses can be evenly distributed among three-phase switching devices.

4.4 Numerical Comparative Analysis of Thermal Losses for Conventional PSC-PWM and Proposed DRV-PWM

To verify the capability of the proposed DRV-PWM technique to balance the thermal losses among the among three-phase switching devices, the system was operated at full *MI* for an hour using the conventional PSC-PWM. This procedure was repeated for the proposed PSC-PWM after allowing the system to completely cool down. The results were

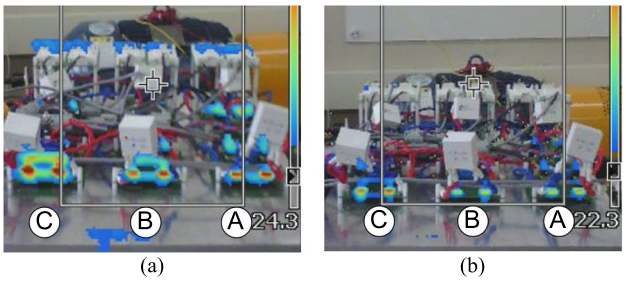

Fig. 16 Investigation of thermal behavior of the three phases of five-level HANPC inverter: **a** Conventional PSC-PWM; **b** Proposed DRV-PWM

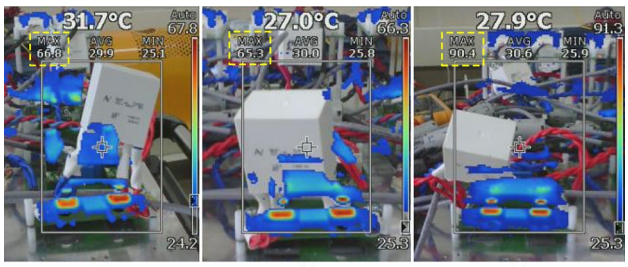

Fig. 17 Detailed investigation of *Cell-III* thermal behavior during the utilization of conventional PSC-PWM: **a** S_{A7} and S_{A8}; **b** S_{B7} and S_{B8}; **c** S_{C7} and S_{C8}

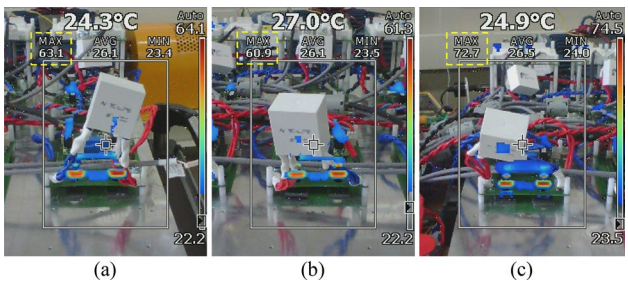

Fig. 18 Detailed investigation of *Cell-III* thermal behavior during the utilization of proposed DRV-PWM: **a** S_{A7} and S_{A8}; **b** S_{B7} and S_{B8}; **c** S_{C7} and S_{C8}

taken using a thermal camera, and are shown in Figs. 16, 17, and 18.

Figure 16 depicts the effectiveness of the proposed DRV-PWM in reducing and balancing the thermal losses of S_{x7} and S_{x8} among the three phases of the five-level HANPC inverter. To obtain a detailed thermal measure of S_{x7} and S_{x8} in each phase, close-up measurements were taken as shown in Figs. 17 and 18 for the conventional and proposed techniques, respectively. It can be seen in Fig. 17 that the conventional PSC-PWM results in unevenly distributed thermal losses among three phases.

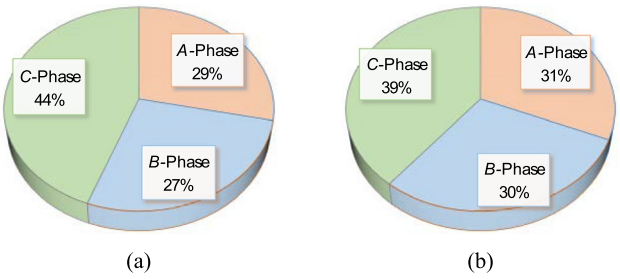

Fig. 19 Investigation of thermal losses distribution for the three phases of five-level HANPC inverter: **a** Conventional PSC-PWM; **b** Proposed DRV-PWM

For example, S_{C7} and S_{C8} have the highest thermal losses, where the junction temperature T_J reaches a maximum value of 90.4 °C, and where the maximum temperature obtained in other two phases are at ≈ 66 °C. On the other hand, the proposed DRV-PWM maintains the maximum T_J at 72.7 °C for S_{C7} and S_{C8}, whereas *A*-phase and *B*-phase achieve relatively lower temperatures of 63.1 °C and 60.9 °C, respectively. This is due to the total control time-delay of whole system. A summary of the thermal losses comparison between the conventional and proposed switching schemes is presented in Fig. 19. It can be seen that the proposed DRV-PWM technique manages to balance the thermal losses among the switching devices of the three-phase five-level HANPC inverter. Conversely, the conventional PSC-PWM method results in more stress on the *C*-phase. Therefore, the reliability and efficiency of system is enhanced by implementing the proposed DRV-PWM.

5 Conclusion

This study presents a less complex but still effective and efficient DRV-PWM scheme for three-phase five-level HANPC inverters that can be used as an alternative to the conventional phase shifted PSC-PWM method. The proposed DRV-PWM simplifies the control structure by eliminating the need for complex phase adjustments and additional PWM carriers; therefore, it is recommended for various microcontrollers. The proposed switching scheme also results in a balanced distribution of thermal losses among the three phases, along with improved reliability and efficiency of the switching devices. The implementation process of the proposed DRV-PWM was explained and experimentally validated using a TMS320F28377S DSP. The results showed that the execution of the three-phase pole voltages was effectively synchronized, and that a balanced distribution of thermal losses was maintained. Further, the proposed DRV-PWM simplifies the hardware coding for generating the switching signals and improves the THD by 5.7%. Overall, the proposed DRV-PWM can be effectively implemented in three-phase five-level HANPC inverters to balance the switching losses and achieve optimal control of this topology.

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