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ORIGINAL ARTICLE

A Novel Quadruple-Boost Nine-Level Switched-Capacitor Inverter

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Abstract
A novel single-phase nine-level switched-capacitor inverter (9LSCI) with quadruple-boost ability and reducing the component counts is proposed. Only one DC source, nine switches, two diodes and two switched capacitors (SCs) are employed in the basic unit of the proposed topology to realize nine-level output. Due to the passive voltage balancing of each capacitor maintains a constant voltage without additional control. A simple logic-gate-based pulse width-modulation scheme is developed for gating switches of the proposed topology. The working principle of the basic unit topology, the voltage/current stress on the switch, the determination of the capacitance and the simulation and the experiment at 400 W output power are introduced in this paper. In addition, an extended form of the basic unit is provided. A detailed analysis of the proposed topology has been carried out to show the superiority of the proposed converter with respect to the other existing MLI topologies. Various simulations are carried out in Matlab/Simulink R2021b and the feasibility is verified in experiments.

Keywords Nine-level inverter · Switched capacitor · Quadruple boost · Passive voltage balancing

1 Introduction

With the depletion of fossil energy and the aggravation of environmental pollution, fossil fuel power generation is gradually replaced by renewable energy, such as photovoltaic and wind energy. In renewable energy systems, power electronic circuits play an important role to supply power stably and efficiently.

Multilevel inverter (MLI) has attracted much attention due to its low total harmonic distortion (THD), low switching voltage stress, low switching loss and small output filter. The classical MLI topology includes cascaded H-bridge (CHB) multilevel inverter, neutral point clamped (NPC) multilevel inverter and flying capacitor (FC) multilevel inverter. However, when the number of operation voltage levels exceeds three, some problems such as voltage imbalance and using many components will be caused. Therefore, MLI with fewer components is studied. However, the applicability of such circuits is highly constrained because most of them are buck type. In general, the renewable sources (such as PV) are available in the form of low-voltage supplies, which needs to be boosted to supply power to the load. First scheme is to connect several PV modules in series to form a high voltage input, which has encountered many mismatch problems. Another traditional solution is to add a DC-DC boost converter to the front stage of the traditional MLI. But the complexity is increased, and efficiency is reduced.

The integrated boost technology based on switching capacitor has been widely studied as a new method to solve the above problems [1]. In [2–7], voltage balance of capacitor can be achieved without auxiliary method by using SC. But boost capacities of them are poor. Recently, this problem has been solved in [8–12], which provide four times the output voltage gain. In [8, 9], 12 power switches are required, which increases the volume of the inverter and reduces the efficiency. The topology in [10, 11] can achieve the nine-level output by 8 power switches. However, more capacitors and diodes are needed in [10, 11] and the inverter topology in [10] has no scalability.

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The scalability is an important performance of MLI. Especially in high-power applications, the switching frequency of inverter is limited due to the limitation of material and technology level of power electronic devices, which leads to the decline of output power quality. There are two solutions in MLI.

The first solution is to increase the switching frequency by reducing the maximum voltage stress on both ends of each switching device in MLI, to achieve high power quality output. However, this method has a high requirement for MLI topology, which requires that the maximum voltage stress at both ends of all high frequency switching devices should not exceed the rated value of safe operation. Moreover, this scheme increases the switching frequency, which increases the switching loss.

Another effective solution is to increase the number of output levels. This scheme has been applied in [13]. Through the nearest level control methods, the output bus voltage presents a step wave, and the number of step waves is determined by the number of levels. The THD of output voltage can be calculated according to the equation provided in [14].

$$\mathrm{THD}, \% = \frac{42}{(h-1)\mathrm{M}}, \% \tag{1}$$

where h is the count of non-negative level and M is the modulation index. It can be concluded from Eq. (1) that when the number of step waves of the output bus voltage is enough, the THD of the output voltage can be reduced to the required value. The outstanding feature of this method is that it does not need to switch the two levels at high frequency due to the output step wave, and the switching frequency is only a few hundred hertz.

Some limitations also exist in the second solution. The increase of output level will inevitably increase the number of components, which will increase the volume of inverter and reduce the efficiency. In [15–18], the number of output bus voltage levels is increased, and the number of components required is reduced by adding DC sources. However, their applications are limited due to the increasing number of DC power supplies. In [19–21], the number of output bus level is increased by using SC in single DC power supply. Unfortunately, a lot of switches, SC and other components are required.

The aim of this article is to cover this specific research gap by introducing a novel 9LSCI inverter and its extended topology suitable for PV power generation that requires boost capability, etc. applications. The base unit inverter that makes up the proposed topology uses fewer components, and it can provide quadruple the output voltage boost function. In addition, the basic cell topology has good scalability, the higher number of output levels can be expanded by adding only a small number of components. The rest of this article is organized as follows. In the second part, the extended topology of 9LSCI basic cell topology, working principle, PD modulation strategy based on logic and the calculation of two switched capacitor parameters are discussed. In the third part, the loss is analyzed. The fourth part gives the comparison between the proposed topology and other topology. The results and analysis are given in the fifth part. Experiments are carried out on the experimental platform based on STM32H750VBT6 to verify its performance. Finally, the conclusion is given in the sixth part.

2 Proposed Circuit

2.1 Circuit Description

The Basic unit of the proposed topology is demonstrated in Fig. 1. In ideal circumstance, the proposed inverter has nine output voltage levels: $\pm 4V_{in}, \pm 3V_{in}, \pm 2V_{in}, \pm V_{in}$ and 0, and to achieve this goal, only one dc voltage source, two capacitors, two diodes, and nine power switches are needed. To realize nine-level output and four times boost of basic cell topology, the capacitor C_1 and C_2 are expected to be charged on V_{in}, $3V_{in}$ and $2V_{in}$, respectively. Among the nine switches in the basic unit topology, the switch S_i has complementary operation with $\overline{S}_i (i = 1, 2, 3, 4)$, which simplifies the switch control. Switch S_1 and $\overline{S}_1$ work in low frequency mode, which further reduces the switching loss.

Further, the number of voltage levels can be increased by cascading multiple such units. The expansion circuit of the basic unit is shown in Fig. 2. The expressions of the number of switches (N_{sw}), capacitors ($N_{C)}$, diodes (N_d) and level (N) are given.

$$\left.\begin{aligned} N_{sw} &= \tfrac{N+9}{2} \\ N_C = N_d &= \tfrac{N-1}{4} \end{aligned}\right\} \tag{2}$$

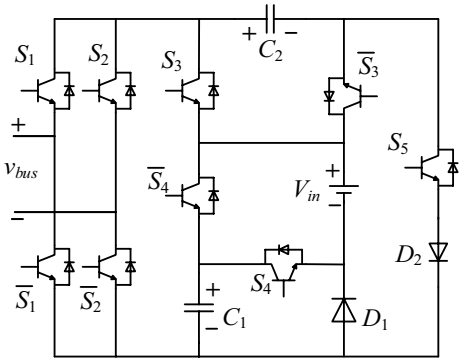

Fig. 1 Basic unit of proposed nine-level inverter

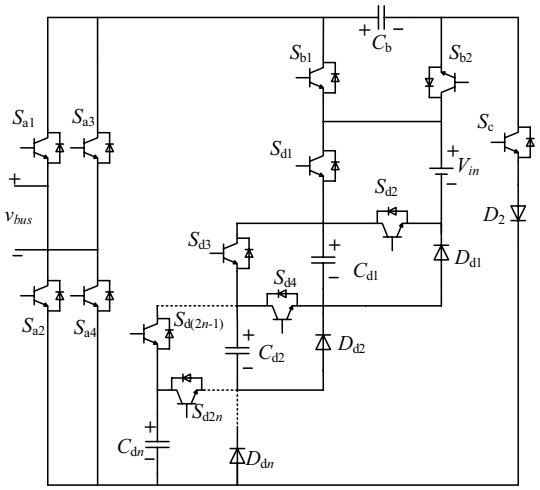

Fig. 2 Extension of the basic unit

The relationship between the number of switches, capacitors, diodes and the number of levels in the extended circuit can be obtained from Eq. (2). According to their relationship, the number of output voltage (v_{bus}) levels increases by 4 with the addition of two switches, a capacitor and a power diode. Its expanded performance is excellent.

The switching states of the proposed topology and the corresponding current paths for each of the output voltage levels are shown in Table 1 and Fig. 3, respectively. The entry "1 =" indicates that a particular switch is ON and "0" indicates the OFF condition.

2.2 Description of Each Voltage Level

For the proposed nine-level inverter, switching patterns are listed in Table 1, including the states of the capacitors, and to have a quick and better understanding, current paths in the positive half cycle are demonstrated in Fig. 3a–e for each case, respectively. Assumptions have been given: all the power devices are ideal, the on-state resistances and forward voltage drops of power devices are considered as zero, the capacitance of the two capacitors is large enough, and the proposed inverter has already entered steady states. To make the concept more accessible, the capacitor voltages are assumed to be constant at $V_{C1}=V_{in}$ and $V_{C2}=2V_{in}$.

State A: it can be seen from Table 1 and Fig. 3a that in state A, capacitors C_1 and C_2 discharge in series with power supply V_{in}, and they share the same discharge current. At this point, the bus voltage (v_{bus}) is

$$V_{bus} = V_{C1} + V_{in} + V_{C2} = 4V_{in} \tag{3}$$

State B: in state B shown in Fig. 3b, capacitor C_1 is charged in parallel with power supply V_{in}, so capacitor C_1 is equal to power supply V_{in}. Capacitor C_2 is discharged in series with power supply V_{in}. At this point, the bus voltage v_{bus} is

$$V_{C1} = V_{in} \tag{4}$$

$$v_{bus} = V_{in} + V_{C2} = 3V_{in} \tag{5}$$

State C: in State C shown in Fig. 3c, capacitor C_1 is connected in series with power supply V_{in} to supply power to load and capacitor C_2. At this point, the bus voltage v_{bus} is

$$V_{C2} = V_{C1}+V_{in}= 2V_{in} \tag{6}$$

$$v_{bus} = V_{C1}+V_{in}= 2V_{in} \tag{7}$$

State D: in state D shown in Fig. 3d, capacitor C_1 is charged in parallel with power supply V_{in}, which satisfies formula (5). Capacitor C_2 does not participate in the charging and discharging process, and it maintains the voltage state at the previous moment. At this point, the bus voltage v_{bus} is

$$v_{bus} = V_{in} \tag{8}$$

State E: in state E shown in Fig. 3e, capacitor C_2 is charged by capacitor C_1 and power supply V_{in}, which satisfies formula (7). At this point, the bus voltage v_{bus} is

Table 1 Switching patterns and state of the capacitors at each voltage level

State	Voltage levels (v_{bus})	S_1	S_2	S_3	S_4	S_5	C_1	C_2
A	$+4V_{in}$	1	0	0	1	0	Discharge	Discharge
B	$+3V_{in}$	1	0	0	0	0	Charge	Discharge
C	$+2V_{in}$	1	0	1	1	1	Discharge	Charge
D	$+V_{in}$	1	0	1	0	0	Charge	None
E	+0	1	1	1	1	1	Discharge	Charge
–	−0	0	0	1	1	1	Discharge	Charge
–	$-V_{in}$	0	1	1	0	0	Charge	None
–	$-2V_{in}$	0	1	1	1	1	Discharge	Charge
–	$-3V_{in}$	0	1	0	0	0	Charge	Discharge
–	$-4V_{in}$	0	1	0	1	0	Discharge	Discharge

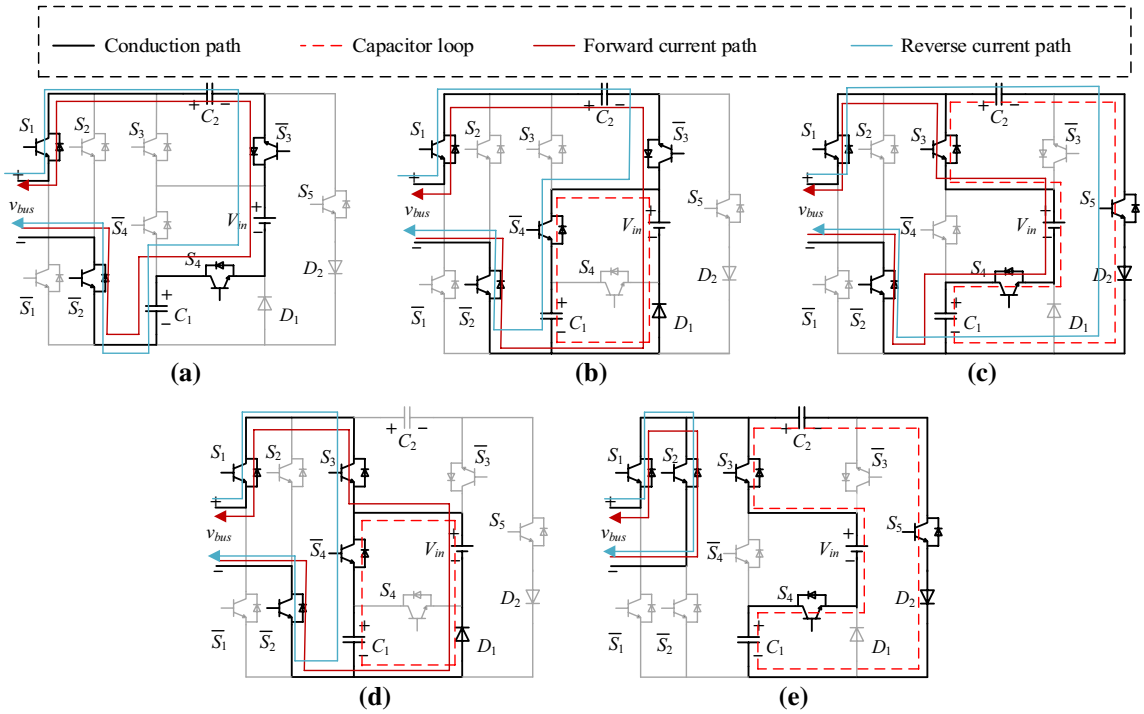

Fig. 3 Current flows in the proposed inverter. **a** State A. **b** State B. **c** State C. **d** State D. **e** State E

$$v_{bus} = 0 \tag{9}$$

Actually, the capacitor C_1 is directly charged in parallel by the input DC source V_{in}, and the capacitor C_2 is charged in parallel by the capacitor C_1 inputting the DC source V_{in} in series and then in parallel. The charging or discharging states of capacitors C_1 and C_2 in each level state are shown in Table 1. After each capacitor is charged, it is equivalent to an independent DC source, and the voltage drop across the capacitor due to discharge is a slow process with small voltage fluctuations. Therefore, it is assumed that $V_{C1} = V_{in}$ and $V_{C2} = 2V_{in}$ are constant.

Overall, the proposed nine-level inverter is equipped with the self-voltage balancing ability, thus simplifying the driving circuits and modulation algorithms. When the load is inductive, the current will flow in the opposite direction, and Fig. 3a–e show the reverse current paths for each voltage level in the positive half cycle. It can be found that the output voltage levels remain the same regardless of the directions of the load current. Since the proposed inverter has a symmetric operation, it can be considered for the other four states in negative half cycle as well.

2.3 Control Strategy

Multi-Carrier PWM has many modulation methods, such as level-shift pulse width modulation (LS-PWM) [22, 23] and phase-shift pulse width modulation (PS-PWM) [24]. However, for MLI with N levels, both LS-PWM and PS-PWM need (N − 1) carriers, and more complex logic control strategies are required.

An optimized multicarrier phase disposition (PD) pulse width modulation (PWM) method is proposed in [25] to simplify the modulation strategy, and it is adopted for the proposed topology. As shown in Fig. 4a, the carrier voltage levels of e_1, e_2, e_3 and e_4 have the same phase and amplitude, but the horizontal displacement difference between adjacent levels is A_C. Sinusoidal modulated signal waveforms $e_s = A_{ref}\sin 2\pi f_{ref} t$ share the same time axis with these carriers. A_{ref} is the amplitude of the sine wave $|A_{ref}| < 4A_c$, f_{ref} is the frequency of the sine wave.

The amplitude of the output voltage waveform V_o is determined by the ratio of the amplitude of the reference sinusoidal signal waveform e_s to the amplitude of the carrier. Therefore, the modulation index m is defined as:

$$M = \frac{A_{ref}}{4A_c} \tag{10}$$

According to Table 1, the simple logic circuits or a lookup table method of the controller can be used for the PWM signals of the switches.

As shown in Fig. 4b, according to the relationship between e_s and e_k (k = 1,2,3,4), four positive level states and one fundamental level can be obtained, and then each switch can be controlled by simple logic control.

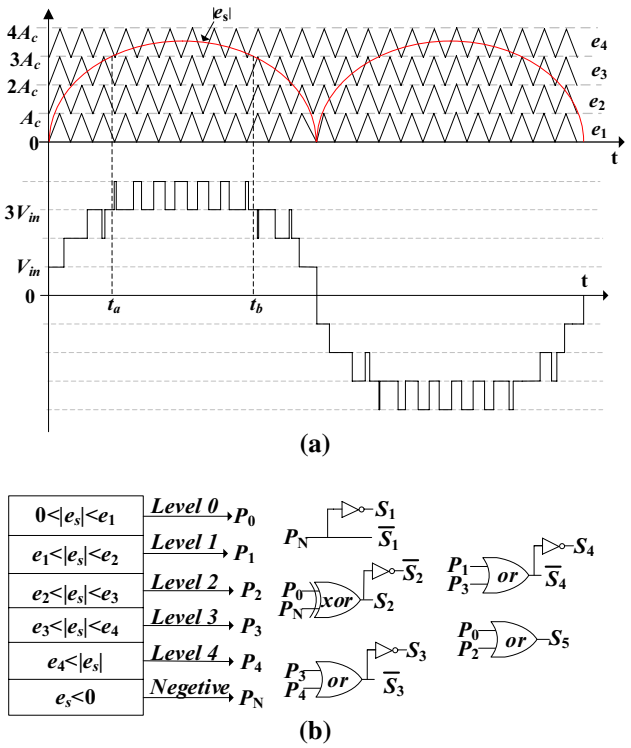

Fig. 4 PD PWM modulation strategy and logic for the proposed topology. **a** Modulation waveform. **b** Modulation logic

2.4 Determination of Capacitances

The peak charging and discharging currents of SC are depended on the voltage ripple at both ends of the capacitor. The high voltage ripple of SC will lead to the decrease of power conversion efficiency. Therefore, through the proper design of the capacitor, the voltage ripple of the floating capacitor can be kept low, and the two peak currents can be reduced to an acceptable value, the efficiency can also be improved. According [26], each capacitance is calculated from their voltage ripple.

For capacitor C_1, voltage ripple can be maintained at a small value by a small capacitance. Because capacitor C_1 does not discharge in two continuous states, energy can be supplemented in each switching cycle.

It is known from [9] that when the capacitor voltage V_{C2} is less than $V_{in}+V_{C1}$, the voltage ripple of capacitor C_1 occurs, and the inverter is in the state of Fig. 3c. Capacitor C_1 discharges and capacitor C_2 is charged. In this state, the current flowing through capacitor C_1 is equal to the output current plus the current of capacitor C_2 charging circuit, which is expressed as

$$i_{C1d}(\mathrm{t}) = i_{C2c}(\mathrm{t}) + i_o(\mathrm{t}) \tag{11}$$

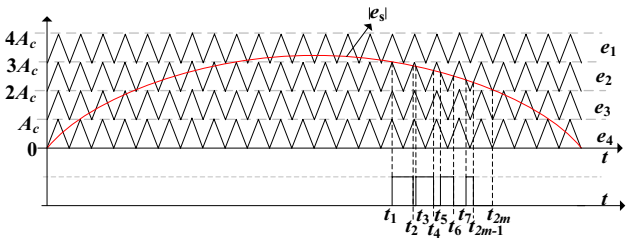

Fig. 5 Discharge period of capacitor C_1 using PD-PWM

i_{C2c} is the charging current of capacitor C_2, which can be expressed as

$$i_{C2c}(\mathrm{t}) = \frac{V_{in} + V_{C1}(\mathrm{t}) - V_{C2}(\mathrm{t})}{r_{in} + r_{C1} + r_{C2} + 3r_{DS} + r_{DD}} \tag{12}$$

where r_{C1} and r_{C2} are the equivalent series resistance (ESR) of the capacitors C_1 and C_2. r_{DS} is ON resistance of the switch. r_{DD} is ON resistance of the diode. $i_o(t)$ is the output current, which can be expressed as

$$i_o(t) = I_{bus} \sin\left(2\pi f_{\mathrm{ref}} \mathrm{t} - \varphi\right) \tag{13}$$

Among them, I_{bus} represents the peak value of the output sinusoidal current; φ represents the phase difference between the output voltage and the output current. When the capacitor C_1 is in the period from $t_{2\mathrm{m}-1}$ to $t_{2\mathrm{m}}$ as shown in Fig. 5, the discharge current flowing through the capacitor C_1 is shown in Eq. (11), and the discharge amount of the capacitor C_1 at this time is expressed as

$$\Delta Q_{1d} = \int_{t_{2m-1}}^{t_{2m}} i_{C1d}(\mathrm{t})dt \tag{14}$$

Therefore, the total discharge of capacitor C_1 during the period t_1 to $t_{2\mathrm{m}}$ is expressed as

$$Q_{1d} = \sum_{m=1}^{n} \Delta Q_{1d} \tag{15}$$

When capacitor C_1 is directly connected in parallel with the power supply, the inverter is in the state of Fig. 3b or Fig. 3d. In the state, the current flowing through capacitor C_1 is

$$i_{C1c}(\mathrm{t}) = \frac{V_{in} - V_{C1}(\mathrm{t})}{r_{in} + r_{C1} + r_{DS} + r_{DD}} - i_o(\mathrm{t}) \tag{16}$$

According to Eq. (16), in the time period of t_{2m-1} and t_{2m-2}, C_1 is charged, which is expressed as

$$\Delta Q_{1c} = \int_{t_{2m-2}}^{t_{2m-1}} i_{C1c}(\mathrm{t})dt \tag{17}$$

The total charging amount Q_{1c} is given as

$$Q_{1c} = \sum_{m=1}^{n} \Delta Q_{1c} \tag{18}$$

Therefore, through Eqs. (15) and (18), the difference between the discharge amount and the charge amount of capacitor C_1 from t_1 to t_{2m} is

$$\Delta Q_1 = Q_{1d} - Q_{1c} \tag{19}$$

Finally, taking the allowable voltage ripple ΔV_{C1} into consideration, the minimum capacitance should meet the following formula

$$C_{1\,\min} = \frac{\Delta Q_1}{\Delta V_{C1}} \tag{20}$$

The same does not apply to C_2, which continuously discharges to the output over the time span (t_a–t_b), as shown in Fig. 4a. In this state, the current flowing through the capacitor C_2 is consistent with the output current. Therefore, the discharge amount of capacitor C_2 in this period is

$$Q_2 = \int_{t_a}^{t_b} i_o(\mathrm{t})dt \tag{21}$$

Considering the voltage ripple ΔV_{C2} of capacitor C_2, the minimum value of capacitor C_2 should be

$$C_{2\,\min} = \frac{\Delta Q_2}{\Delta V_{C2}} \tag{22}$$

2.5 Voltage/Current Stresses on Switches

From the five states in Fig. 3, voltage stresses (V_{si}, $i = 1$–5) of the nine switches are found as

$$V_{S4} = \frac{1}{2}V_{S3} = \frac{1}{2}V_{S5} = \frac{1}{4}V_{S1} = \frac{1}{4}V_{S2} = V_{in} \tag{23}$$

It should be noted that the voltage stresses of S_i and $\overline{S}_i (i = 1, 2, 3, 4)$ are the same, but the current stresses flowing through them are different.

It can be seen from Fig. 3 that the maximum current stress of switches S_1, S_2 and $\overline{S}_i (i = 1, 2, 3)$ is the output current I_{bus}. The maximum current flowing through the switch S_3 occurs in the State C shown in Fig. 3, which is consistent with the discharge current flowing through the capacitor C_1 as $i_{c1d}(t)$. In state A and State C, the current flowing through switch S_4 is $i_o(t)$ and $i_{c1d}(t)$, respectively. Therefore, the maximum current stress of switch S_4 is I_{bus} or $i_{C1d,max}$. Where $i_{C1d,max}$ is the maximum discharge current of capacitor C_1 in state C. The difference is that the switch $\overline{S}_4$ is only turned on when the capacitor C_1 is charged, and it is directly connected in series with C_1.

Therefore, the current stress is $i_{C1c}(t)$ according to Eq. (16). Similarly, the switch S_5 is only turned on when the capacitor C_2 is charged, and it is directly connected in series with C_2. The current stress $i_{C2c}(t)$ is obtained from Eq. (12).

3 Loss Analysis

Three types of losses are considered for the switched capacitors converters, which include capacitors conduction losses (P_C), switching losses (P_S), and capacitors charging losses (P_{Rip}).

3.1 Calculation of Conduction Losses

Conduction losses for the power switch and power diode is obtained from the following equations [27]:

$$P_{C,sw}(t) = V_{on,sw} i_{sw,avg} + r_{on,sw} i_{sw,rms}^2 \tag{24}$$

$$P_{C,D}(t) = V_{on,D} i_{D,avg} + r_{on,D} i_{D,rms}^2 \tag{25}$$

where $P_{C,sw}(t)$ and $P_{C,D}(t)$ indicates the conduction loss of the switch tube and diode respectively. V_{on} and r_{on} is the voltage drop and the on resistance of the device in the on state. i_{avg} and i_{rms} represents the RSM current and average current flowing through the switch tube and diode respectively.

Each level state shown in Fig. 3 corresponds to a discharge path, so there is a corresponding conduction loss on the on path. By calculating the conduction loss of the level in each state, the total conduction loss can be obtained in a whole period. The conduction loss can be obtained by the following formula:

$$P_{C,(State,A)} = 4V_{on,sw} i_{bus,avg} + 4r_{on,sw} i_{bus,rms}^2 \tag{26}$$

$$\begin{aligned} P_{C,(State,B)} = {} & V_{on,sw}(3i_{bus,avg} + i_{C1c,avg}) + r_{on,sw}(3i_{bus,rms}^2 \\ & + i_{C1c,rms}^2) + V_{on,D} i_{in,avg} + r_{on,D} i_{in,rms}^2 \end{aligned} \tag{27}$$

$$\begin{aligned} P_{C,(State,C)} = {} & V_{on,sw}(2i_{bus,avg} + 2i_{C1d,avg} + i_{C1c,avg}) \\ & + r_{on,sw}(2i_{bus,rms}^2 + 2i_{C1d,rms}^2 + i_{C1c,rms}^2) \\ & + V_{on,D} i_{C2c,avg} + r_{on,D} i_{C2c,rms}^2 \end{aligned} \tag{28}$$

$$\begin{aligned} P_{C,(State,D)} = {} & V_{on,sw}(3i_{bus,avg} + i_{C1c,avg}) + r_{on,sw}(3i_{bus,rms}^2 \\ & + i_{C1c,rms}^2) + V_{on,D} i_{in,avg} + r_{on,D} i_{in,rms}^2 \end{aligned} \tag{29}$$

In the state E shown in Fig. 3, the currents of load circuit switch and charging circuit of capacitor C_2 are small, so the conduction loss in this state is ignored. It is worth noting that the conduction loss in the four states of negative half period is symmetrical with that of positive half period, so the total conduction loss can be calculated as:

$$P_C = 2(P_{C,(State,A)} + P_{C,(State,B)} + P_{C,(State,C)} + P_{C,(State,D)}) \tag{30}$$

3.2 Calculation of Switching Losses

One of the most important sources of the power loss is switching losses (P_S) which are generated due to switching delays that are intrinsic to the semiconductor devices. Because of the different delay time of switching on and off, the loss of each switch can be divided into on loss ($P_{sw,i(on)}$) and off loss ($P_{sw,i(off)}$) in one basic frequency period. The losses of the active switches during the turning ON and OFF are obtained as following equations [3]:

$$\begin{aligned} P_{sw,i(on)} &= f_{ref} \cdot N_{sw,i(on)} \left[\int_0^{t_{on}} v_{S,i}(t) i_{S,i}(t) dt \right] \\ &= \frac{f_{ref} \cdot N_{sw,i(on)} \cdot V_{S,i} \cdot I_{S,i} \cdot t_{on}}{6} \end{aligned} \tag{31}$$

$$\begin{aligned} P_{sw,i(off)} &= f_{ref} \cdot N_{sw,i(off)} \left[\int_0^{t_{off}} v_{S,i}(t) i_{S,i}(t) dt \right] \\ &= \frac{f_{ref} \cdot N_{sw,i(off)} \cdot V_{S,i} \cdot I_{S,i} \cdot t_{off}}{6} \end{aligned} \tag{32}$$

where, $N_{sw,i(on)}$ and $N_{sw,i(off)}$ are the number of times that the switch i is turned on and off in the fundamental frequency period. t_{on} and toff are the delay time for the switch to turn on and turn off completely. $V_{S,i}$ and $I_{S,i}$ can be approximately considered as the voltage stress and current stress before the switch is turned on and off respectively. The on loss ($\overline{P}_{sw,i(on)}$) of switch $\overline{S}_i (i = 1, 2, 3, 4)$ and off loss ($\overline{P}_{sw,i(off)}$) is similar to the above formula.

Further, $N_{sw,i(on)}$ and $N_{sw,i(off)}$ are equal in one fundamental frequency period and expressed as $N_{sw,i}$. Since the operation of switch S_i and switch $\overline{S}_i (i = 1, 2, 3, 4)$ are complementary, the number of times they on and off is considered equal. The switching losses of S_1 and $\overline{S}_1$ operating at fundamental frequency are neglected. $N_{sw,i(on)}$ and $N_{sw,i(off)}$ for switches of each module is calculated as following equations:

$$N_{sw,i} = \begin{cases} \frac{\sin^{-1}\left(\frac{A_c}{A_{ref}}\right)}{\pi} \cdot \frac{f_s}{f_{ref}}, i = 2 \\ \frac{\sin^{-1}\left(\frac{3A_c}{A_{ref}}\right) - \sin^{-1}\left(\frac{2A_c}{A_{ref}}\right)}{\pi} \cdot \frac{f_s}{f_{ref}}, i = 3 \\ \frac{f_s}{f_{ref}}, i = 4 \\ \frac{\sin^{-1}\left(\frac{3A_c}{A_{ref}}\right)}{\pi} \cdot \frac{f_s}{f_{ref}}, i = 5 \end{cases} \tag{33}$$

Therefore, the total switching loss is

$$P_S = \sum_{i=2}^{5} \left(P_{sw,i(on)} + P_{sw,i(off)} \right) + \sum_{i=2}^{4} \left(P_{\overline{sw},i(on)} + P_{\overline{sw},i(off)} \right) \tag{34}$$

3.3 Calculation of Ripple Losses of Capacitors

The ripple losses are caused by the parallel connection of capacitors with input DC sources for charging the capacitors. The voltage ripple of capacitor is calculated by (20) and (22). Therefore, capacitors ripple losses are obtained from the following equation [28]:

$$P_{Rip} = \frac{f_{ref}}{2} \sum_{k=1}^{2} \left(C_k \Delta V_{Ck}^2 \right) \tag{35}$$

where C_k and ΔV_{Ck} represent the capacity and voltage ripple of capacitor $k(k = 1,2)$ respectively.

Then, using (30), (34), and (35), the total losses of proposed topology (P_{tot}) will be

$$P_{tot} = P_C + P_S + P_{Rip} \tag{36}$$

Finally, the efficiency can be achieved as

$$\eta = \frac{P_{out}}{P_{tot} + P_{out}} \times 100\% \tag{37}$$

4 Comparative Study

In order to evaluate the advantages and disadvantages, the comparisons between the proposed topology and other nine-level inverters reported recently are given. Table 2 shows the comparison of the key characteristics between the nine-level inverter introduced in this paper and the nine-level inverter recently reported. According to the number of power switches (N_{SW}), the number of input DC sources (N_{DC}), the number of independent diodes (N_d), the number of capacitors (N_{cap}), the output voltage gain and the scalability of the topology are compared.

The three traditional types of nine-level inverters have good scalability, and with the increase of the number of

Table 2 Comparison of proposed nine-level inverter with conventional and other recent SCMLI topologies

References	Power electronic components					
	Nsw	Ndc	Nd	Ncap	Gain	Expandability
[2]	19	1	3	3	4	Yes
[3]	12	2	2	2	2	Yes
[4]	11	1	0	2	2	Yes
[5]	9	1	2	2	2	No
[6]	9	1	1	4	2	No
[7]	8	1	1	2	2	No
[8]	12	1	0	2	4	Yes
[9]	12	1	0	3	4	Yes
[10]	8	1	3	3	4	No
[11]	8	1	4	4	4	Yes
[12]	9	1	1	2	4	No
Proposed	9	1	2	2	4	Yes

levels, the output power quality also increases. Unfortunately, a large number of components are required and they do not have boost capability.

Compared with the nine-level topology reported in [2–9], the basic unit of the proposed topology has more advantages in the number of components or output performance. For example, the basic unit of the proposed topology in this paper has the same number of components as the topology reported in [5, 6]. However, the proposed topology has more advantages in terms of output voltage gain and scalability.

The nine-level topologies reported in [10, 11] have good output voltage gain, and the number of switches is less than the proposed topology. However, the proposed topology has obvious advantages in terms of the number of independent diodes and capacitors. Compared with the nine-level topology reported in [12], the proposed topology has one more diode, but the topology reported in [12] has no scalability.

The single source extension of the proposed topology has been compared with several single source extension circuits introduced in other literatures. As shown in Fig. 6, the curves of the number of switches, driving circuits and capacitors with the increase of the level are shown respectively. Figure 6a shows the curve of the number of switches varies with the number of levels. When the number of levels exceeds five, the proposed topology needs fewer switches and has obvious advantages. Figure 6b shows the relationship between the required gate drive and the number of levels. It is worth noting that, except for the inconsistency of the number of driving circuits and switches in the topology introduced in [4], the number of driving circuits in other expansion circuits compared is consistent with their respective number of switches. Figure 6c shows the curve of the number of capacitors varies with the number of levels. The proposed topology also has advantages.

5 Results and Analysis

5.1 Simulation Results

Simulink simulations are carried out to verify the performance of the proposed nine-level inverter. The simulation model is shown in Fig. 7, and the simulation parameters are shown in Table 3. DC input is 50 V, which leads to 50 V and 100 V at C_1 and C_2 of SC capacitor. The peak value of nine-level output voltage is 200 V. According to the data sheet of IXFH80N65X2, the conduction resistance and drain-source capacitance of MOSFET are determined. According to the data sheet of DSEI60, the conduction resistance r_{D1}-r_{D2} and the forward conduction voltage drop of independent diodes $D_1 - D_2$ are determined.

Figure 8a and b show the simulation waveforms of bus voltage, output voltage and output current under pure resistive load Z_1 and inductive load Z_2 respectively. The DC voltages at both ends of switching capacitor voltage C_1 and C_2 under inductive load Z_2 are shown in Fig. 8c. The simulation waveform is consistent with the analysis. The FFT analysis of bus voltage v_{bus} under load Z_2 is shown in Fig. 8d. Compared with the fundamental frequency component, the odd order harmonics are greatly attenuated, and the frequency of the fundamental frequency component is the same as the output voltage. That is to say, the low THD is achieved by the proposed nine-level inverter with fewer components. On the other hand, the THD of bus voltage v_{bus} shown in Fig. 8d is 16.89%, which satisfies another THD calculation expression described in [11].

$$\mathrm{THD},\% = \frac{57.7}{(h-1)M},\% \tag{38}$$

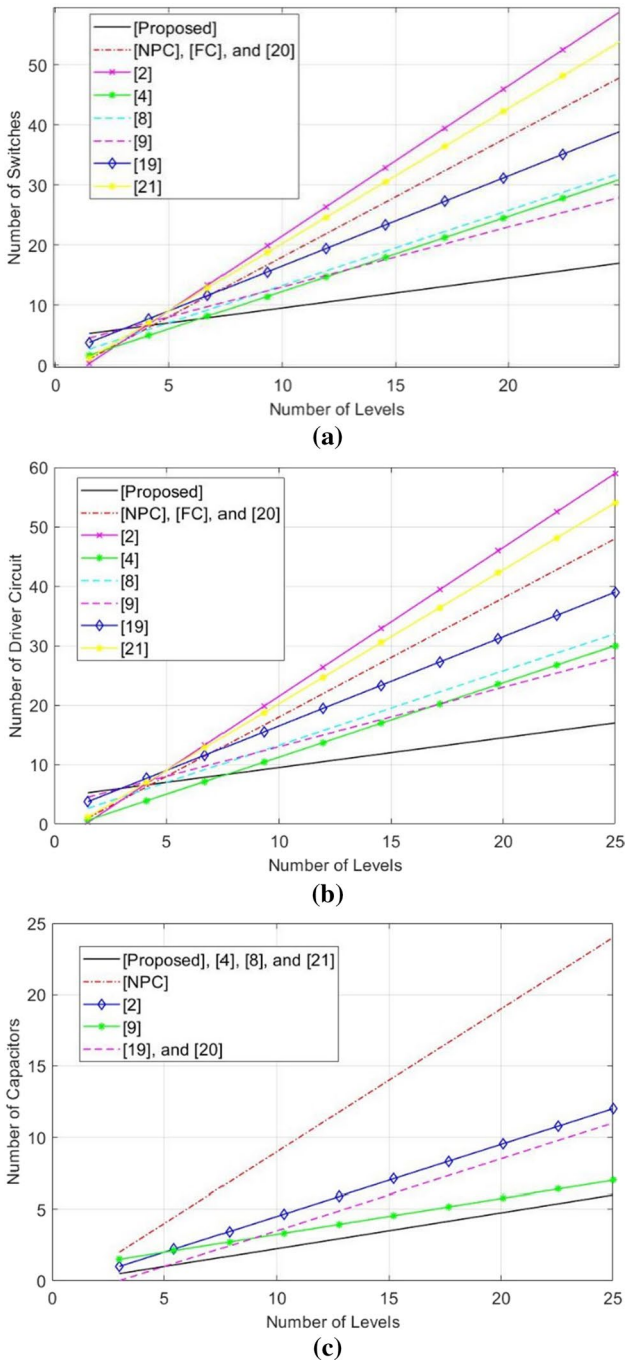

Fig. 6 Extension Variation of **a** number of switches **b** number of gate driver circuit and **c** number of capacitances

When the modulation index M is 0.9, the voltage THD is estimated to be 16.03%, which is in good agreement with the simulation results. In fact, formula (1) and formula (38) are not contradictory, because they serve different objects. Equation (1) is for the case that the output of bus voltage v_{bus} is a step wave, while Eq. (38) is for the case that bus voltage v_{bus} switches quickly under two levels.

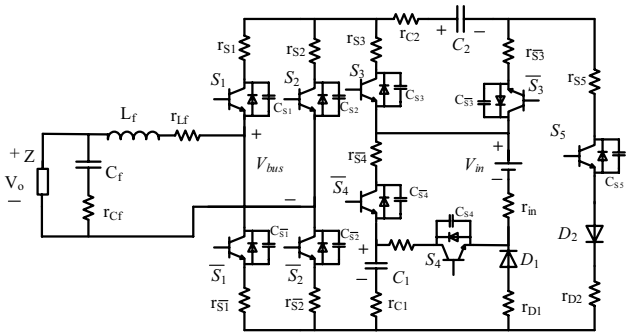

Fig. 7 Simulation model of the proposed inverter

Table 3 Simulation parameters of the proposed inverter

Parameters	Value
Input voltage V_{in}	50 V(r_{in}:50 mΩ)
Modulation index M	0.9
Output load Z	Z_1:50 Ω
	Z_2:50 Ω + 100 mH
MOSFETs	r_{DS}:38 mΩ C_{DS}:5000 pF
Independent diode	V_F:1.13 V $r_{D1} - r_{D2}$:4.7 mΩ
Capacitor C_1	2 mF(r_1: 20 mΩ)
Capacitor C_2	4 mF(r_1: 10 mΩ)
Filter capacitor C_f	8 μF(r_f: 25 mΩ)
Filter inductor L_f	0.4 mH(r_{Lf}: 35 mΩ)
Switching frequency f_s	10 kHz
Frequency of the sinusoidal signal waveform f_{ref}	50 Hz

The dynamic waveform of modulation index M of the proposed basic cell topology under inductive load Z_2 is given in Fig. 9a. 0.2, 0.4, 0.6–1, the corresponding THD of the output voltage is 5.29%, 2.76%, 1.68%, and 1.24%, respectively, and the power quality of output voltage and current waveform will be improved. Moreover, when the modulation index M changes dynamically, its dynamic performance does not decrease.

The key waveforms of the proposed basic cell topology when load is suddenly added are shown in Fig. 9b. Figure 9b is the waveform of bus voltage v_{bus}, output voltage v_{out} and output current i_{out} from no-load sudden change to inductive load Z_2. The output voltage is stable, and the output current can be smoothly transited under sudden load addition.

The curve of output efficiency changing with power is shown in Fig. 10 when the output load is reduced from 320 to 40 Ω. When the output power $P_o = 115$ W, the maximum power conversion efficiency is 97.2%.

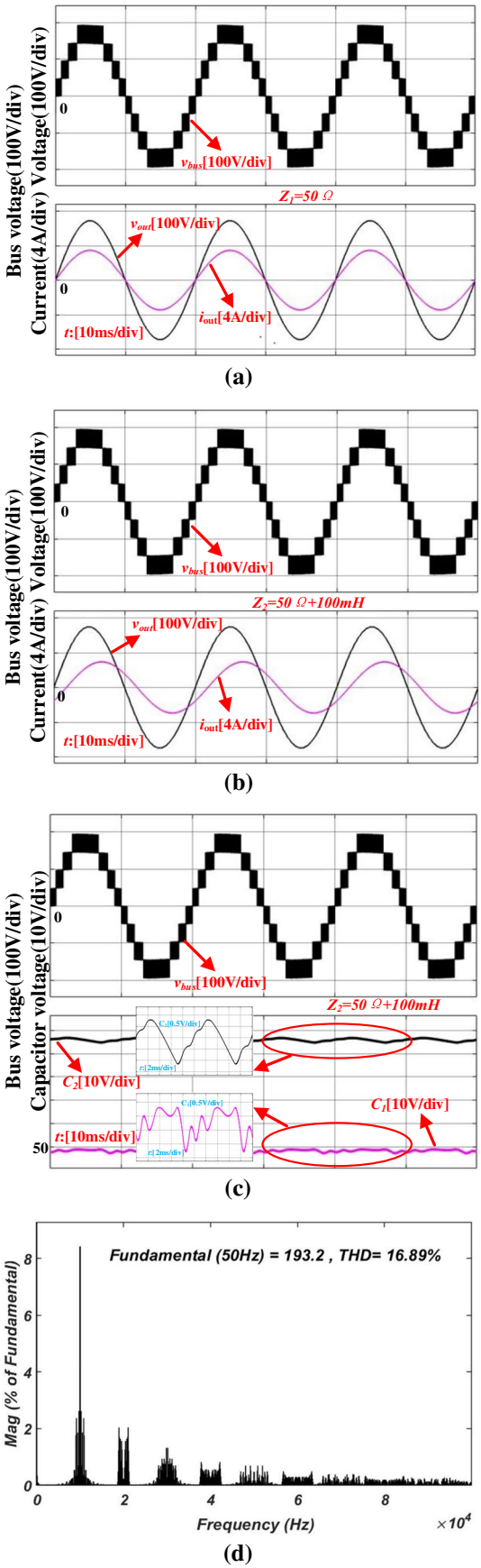

Fig. 8 Simulation results with **a** $Z_1 = 50\ \Omega$. **b** $Z_2 = 50\ \Omega + 100$ mH. **c** ▶ SC voltages with Z_2. **d** FFT of bus voltage v_{bus} with Z_2

5.2 Experiment Analysis

In order to further verify the feasibility of the proposed basic unit nine-level SC inverter, the experimental prototype shown in Fig. 11 is realized. The experimental circuit parameters and equipment specifications are shown in Table 4. The system is controlled by STM32H750VBt6 single chip microcomputer. The DC voltage of the system is 50 V and the modulation index is 0.9. The load is 45 Ω. The filter inductor is self-winding, the inductance is 1.1mH, and the filter capacitor is 8 μF. The switching frequency is 10 kHz and the frequency of output fundamental is 50 Hz.

The experimental results of the proposed basic cell nine-level SC topology are shown in Fig. 2. Under pure resistive load, the phase of output voltage and current are the same, as shown in Fig. 12a. Figure 12b shows the DC voltage waveforms at both end of two SC in the main circuit. The experimental results are consistent with the simulation, and the fluctuation of voltage is small.

The experimental results when the modulation index changes dynamically are shown in Fig. 13. In Fig. 13a, when the modulation index increases from 0.2 to 0.6, the output bus voltage is transited from 3-level output to 7-level output, and the dynamic performance of the transition is good. Figure 13b shows the dynamic change of modulation index from 0.9 to 0.4. At this time, the corresponding level of output bus voltage is transited from 9-level output to 5-level output. When the output level is decreased, the output waveform is still stable. Figure 14 shows the experimental results of the proposed basic cell nine-level SC inverter under sudden load change. When the load is suddenly added, the experimental waveform is consistent with the simulation. It should be pointed out that the parameters of the simulation model are assumed to be known. For the black-box inverter system in practical applications, that is, when the parameters of the components in the inverter are unknown, these unknown parameters are expected to be estimated and determined by some identification algorithms [29–34] to make them to be white-box, such as the least squares algorithm [35–40] and the gradient algorithm [41–48], etc. The combination of recognition algorithm and power electronics has broad application prospects.

6 Conclusions

In this paper, a novel switched capacitor nine-level inverter with four times boost capability is proposed. The proposed topology is highly scalable, which can increase the output voltage by four levels and four times the output voltage gain

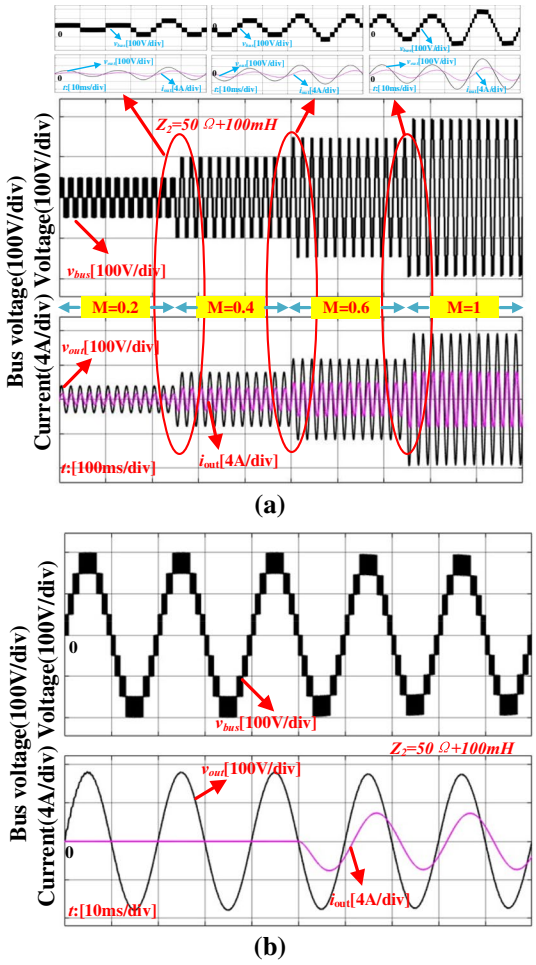

Fig. 9 Simulation results with **a** dynamic change of modulation index **b** output voltage and current waveforms with change of load from no-load to Z_2

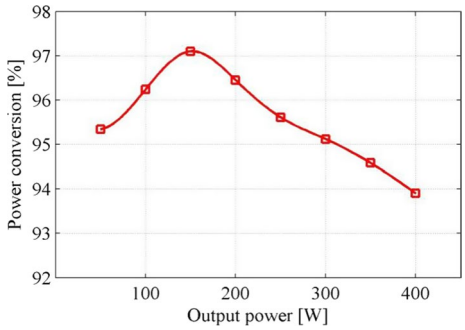

Fig. 10 Efficiency of the proposed topology

when every two switches and a small number of auxiliary passive components are added to the base unit of the proposed topology. However, an H-bridge is required in the proposed topology, which increases the output voltage stress. The high scalability of the proposed topology can reduce

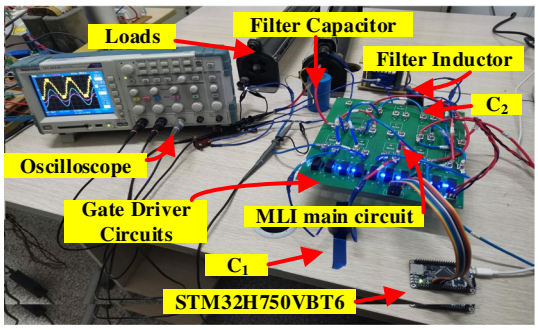

Fig. 11 Hardware setup of the proposed inverter

Table 4 components of the experimental prototype

Devices	Modes
Switches	IXFH80N65X2
Capacitors C_1	2000 µF/250 V
Capacitors C_2	4000 µF/250 V
Diodes D_1 and D_2	MUR3060P
Filter Capacitor C_f	8 µF
Filter Inductor L_f	1.1 mH

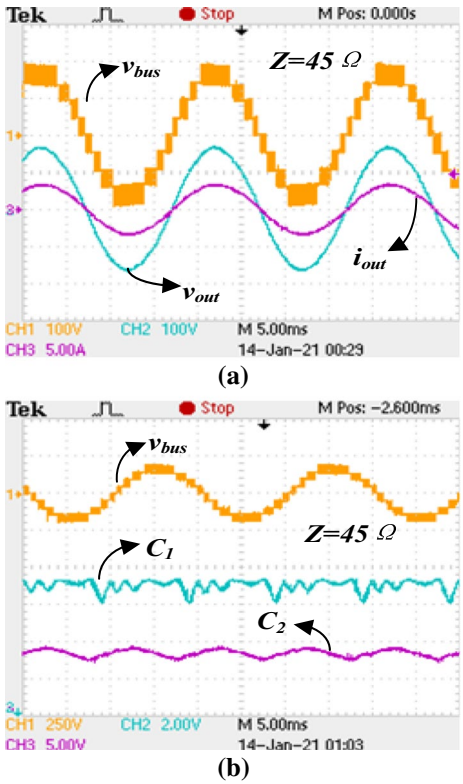

Fig. 12 Experimental results with **a** bus voltage v_{bus}, output voltage v_{out} and output current i_{out}. **b** SC voltages

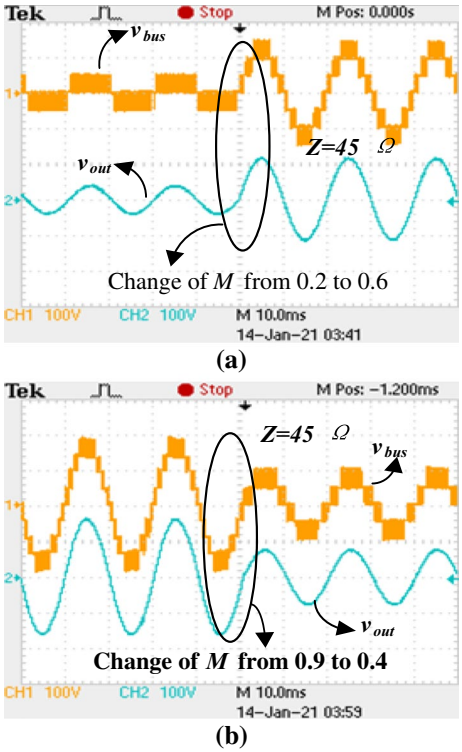

Fig. 13 Experimental results of propose topology after changing M values from. **a** 0.2–0.6 **b** 0.9–0.4

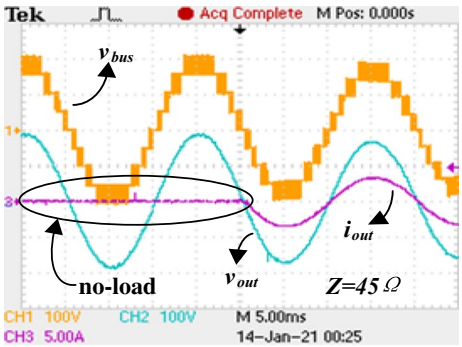

Fig. 14 Experimental waveform of sudden load change

the influence of this disadvantage. When the number of the output level of the expansion circuit is enough, the switching frequency can be effectively reduced by using the output step wave. This paper presents extended form of the basic unit, and introduces the working principle, modulation method, switched capacitor parameter calculation, loss analysis, comparison, simulation and experimental results of the basic unit as a conventional nine level inverter. The capacitor in the proposed topology has the capacity of capacitor voltage self-balancing, and the PD modulation algorithm based on logic is used to simplify the complexity of the modulation circuit. Compared with the existing topology, the superiority of the proposed inverter is proved. All the advantages and feasibility of the proposed topology are evaluated through the simulation model. An experimental prototype with rated power of 400 W is built, and the experimental dynamic waveforms under different conditions are described. The results show that the proposed inverter has good dynamic performance as a switching power supply. It is worth noting that the topology proposed in this paper still needs to be improved. For example, the mathematical model study of the proposed topology has not been given. Some advanced modeling methods for linear [49–55] and nonlinear [56–60] systems are helpful for the establishment of a more accurate mathematical model of the proposed structure, which in turn can be applied to other fields.

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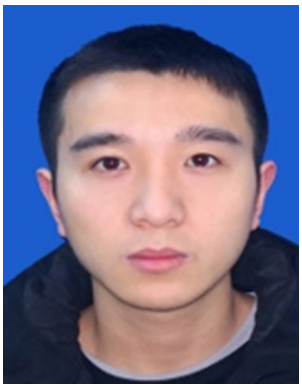

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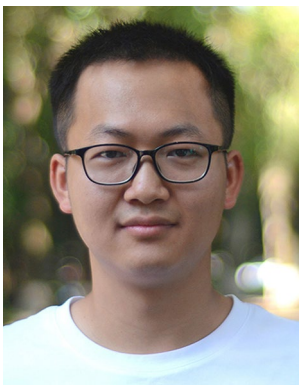

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