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ORIGINAL ARTICLE

Design and Realization of Ultra Gain Boost Seven Level Inverter for Solar PV System

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Abstract
A new triple gain boost seven-level inverter is proposed for solar photo voltaic (PV) system suitable for standalone and grid-connected operations. The system is developed with a boost cascaded two-stage configuration. The principal stage comprises of a high gain DC–DC converter to boost and normalise the input DC voltage with a single switch high gain converter (SSHGC), and the subsequent stage comprises of new multilevel inverter (MLI) topology with triple voltage gain to produce seven level AC. Proposed SSHGC is suitable for a wide conversion range. The switched capacitor techniques were employed to gain the voltage in MLI. The maximum voltage gain of the DC–DC converter is twelve and the voltage gain of the MLI is three, the resultant voltage DC–DC–AC is achieved up to 36. Modified Perturb and Observe (P&O) based maximum power point tracking (MPPT) algorithm is applied in SSHGC to achieve maximum power utilisation in PV module and sinusoidal pulse width modulation (SPWM) is realistic in MLI control. A prototype model of 200 Watts is developed to analyze the proposed system. The overall converter system efficiency reaches up to 92% with a total harmonics distortion (THD) of 0.18%.

Keywords Single switch high gain converter · Boost multilevel inverter · Solar PV system

1 Introduction

The widespread of industrialisation and population increases caused to increase the energy consumption. The use of conventional energy sources increased carbon dioxide emission by simulating global warming and caused to creates unfavorable issues. Researchers are continuously struggling to develop alternate energy sources to replace conventional energy sources. Nonconventional energy sources are a good substitute for conventional energy sources. Unlikely, Nonconventional energy sources lead to high initial cost and low efficiency. Solar photovoltaic (PV) modules, small wind turbines (WT), fuel cells, etc., are widely used to harvest electrical power from non-conventional sources. However, most of the nonconventional energy systems produced unregulated low DC Voltages (12 V–48 V) and it is supposed to step up to regulated higher DC voltage levels to feed cascaded connected voltage source inverter (VSI). The converters used in the systems need some unique characteristics, such as low cost, small size, wide conversion voltage range, and Great efficiency. The DC–DC power converter can be categorised into non-isolated, partially isolated, and isolated [1].

If a wide conversion range and galvanic isolation are necessary, isolated converters (IC)is the obvious choice. A wide conversion range is achieved not only in the duty cycle, but it can also achieve between the high-frequency transformer (HFT) winding ratio. Isolated converters are faced with massive leakage inductance problems. High switching frequency has reduced the size of the HFT. However, it creates high voltage stress across switches. Isolated converters with HFT are perceived as high volume and weight, high cost, and low efficiency [2, 3].VariousPartially isolated converters (PIC) structure has been proposed [4, 5]. Partially isolated converters are preferred substantial of isolated bidirectional half and full-bridge PWM Converters. PIC is consequential of isolated bidirectional half and full-bridge PWM Converters and its area viable choice for extent input, and output ports, The prominent feature of partially isolated converters are low components count leads to avoid complex circuit.

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Conversely, partially isolated converters had constricted voltage regulation, making high voltage stress consequences restricted to low power application. Moreover, the failure of a single element creates enormous issues.

Non-isolated converters (NIC) are used in a wide conversion range and where galvanic isolation is not necessary. The reactive components and semiconductors have dispersed the load. A wide conversion range is attained with a high duty cycle that produces high current and voltage stress, consequently reducing dynamic response. Non isolated converters are produced high current ripples in the series inductor. Undesirably its create reverse recovery issues that lead to conduction loss and poor efficiency [4, 5]. The converters are referred to in [6] is proposed a converter with a coupled inductor for high voltage conversion. Coupled inductors are made with a ferrite core with a 1:1 transformation radio. Coupled inductor-based converters are produced high EMI issues and it's are not suitable for high-frequency operation. Voltage doubler circuits [7] are used for a high conversion ratio, Two are more reactive components are used. Voltage doubler circuits are suitable for high-frequency operation. Interleaved converters [8, 9] are preferred for high power applications, more number of inductors, switches, coupled inductors, and Transformers are involved. Switches are operated in a different period leads to difficult control and reduced static gain. Cascaded boost converters are referred to in [10–12], two simple boost converters are connected in cascade for a wide conversion range. Superior voltage gain achieved. Conversely, more components and more stages influenced noises to create poor efficiency. Snubbed circuits and complex control schemes are indispensable to remove noises and increase the efficiency of the cascaded converter. The single-ended primary-inductor converter (SEPIC) [13–15], Cuk converter [16, 17], and interleaved flyback converter [18, 19] are choices for a wide conversion range. Aforesaid topologies, necessary to operate low or high-duty radio, lead to high cost and complex driver circuits. Wide range conversion influenced high voltage stress and filter inductor parasitic resistances create significant losses instigated to performance degrade and poor efficiency.

Commercial PV systems need DC–AC conversion to operate AC Loads. Multilevel inverters are an obvious choice for smooth operation [20–23]. MLI is considered to meet fixed AC output voltage and frequency, Low THD, Restricted voltage fluctuation. Conventionally, many topologies are emerged to achieve multilevel outputs. It prerequisites multiple sources to generate multilevel outputs. The maximum output voltage of a conventional multilevel inverter is a sum of input DC source voltages. Split capacitors and T-type multilevel inverter [24–26] are used laterally to increase the level of output from a single DC source. However, the maximum output voltage of the T-type multilevel inverter is equal to the input DC source voltage. Switched capacitors multilevel inverters [27–30] are better for a renewable energy system due to their robustness. Switched capacitors MLI multilevel output is generated from a single DC source and creditable voltage gain.

In view of the extensive analysis, indispensable to develop a converter with a good voltage conversion, less voltage stress across switches. Incorporation of voltage multiplier circuit with existing boost converter circuit is superior choice to achieve high voltage conversion ratio and less switching voltage stress. In general DC–DC converters are used to improve the input voltage and subsequently DC–AC converters are used to convert high voltage DC to AC. Boost operation is performed in DC–DC conversion. Among these power electronic devices DC–DC converters are highly effective for DC voltage regulation and to improve the efficiency of renewable energy systems. Appropriate selection of the DC–DC converter is an important factor that has a significant contribution to the overall performance of the power systems. Besides, the selection of an efficient DC–DC converter topology, for its optimum operation integration of a suitable control technique is equally important. The proposed SSHGC is incorporated with Luo super lift voltage multiplier circuit for wide voltage conversion and MLI is developed with switched-capacitor technique. Two capacitors are used to generate seven-levels output with a triple boost. The structure of the proposed DC–DC–AC converter is shown in Fig. 1. Voltage gain is achieved in both SSHGC and MLI.

The paper describes the structure and operating modes of the SSHGC in Sect. 2. Proposed multilevel DC–AC circuit configuration and operating modes are described in Sect. 3. Analysis of the DC–DC–AC converter with parameter design is discussed in Sect. 4. The simulation and experimental results of the cascaded SSHGC and MLI are presented in Sect. 5. Conclusion with features of the cascadedSSHGC and MLI is described in Sect. 6.

2 Analysis of Single Switch High Gain Converter

The structure of the SSHGC is shown in Fig. 2. PV module is connected to low voltage DC input port and MLI is connected in high voltage output port. The output power of the PV module depends on the intensity of the light fall on the PV module and the output voltage of the PV module is varying manner. The Inductor L_1 and capacitor C_1 act as an LUO super lift circuit. To achieve a wide conversion range, Inductor L_2 is integrated with LUO super lift circuit. The Diode D_1, D_2, and D_3 are connected with an Inductor L_1, L_2, and C_1. The filter capacitor (C_F) is connected across the output DC port, which helps to operate the MLI with a constant voltage. The operating modes of SSHRC are shown in

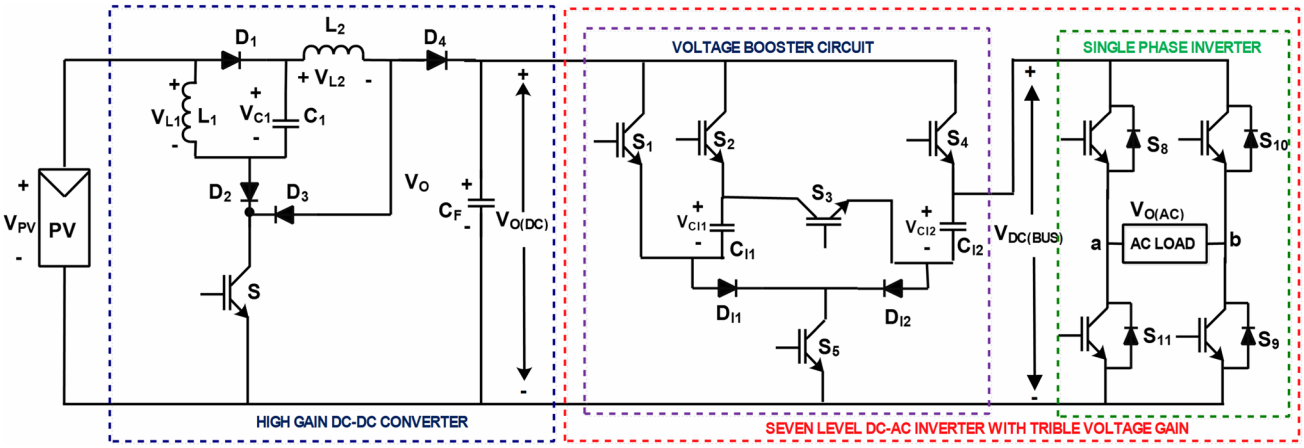


Fig. 1 Proposed DC–DC–AC converter

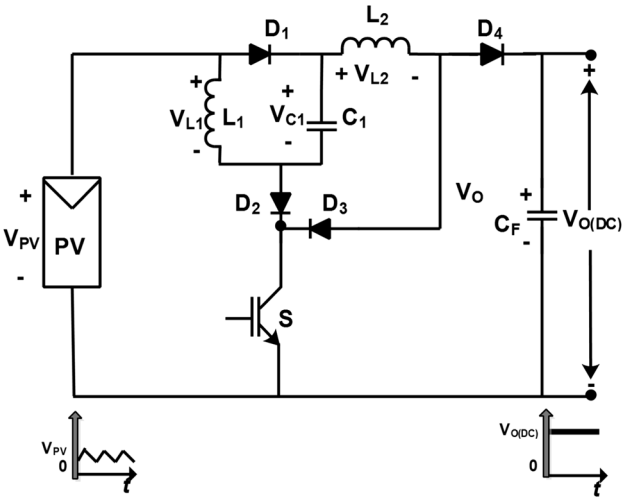


Fig. 2 Structure of SSHGC

Fig. 3a and b. D_4 is connected between the high gain circuit and output port in order to reduce reverse current flow.

The equivalent circuit of Mode-I operation of SSHGC is shown in Fig. 3a. The Switch *'S'* starts conduction at the time of t_1, The PV voltage makes the Diodes D_1, D_2, and D_3 as forward biased. PV current starts to flow through the L_1, L_2, C_1. L_1, L_2, C_1 are connected in parallel with PV Module through Diodes D_1, D_2, and D_3. L_1, L_2, and C_1 are being charged by harvested solar power. The current flowing through the PV (I_{PV}) is equal to the sum of the current in inductors L_1, L_2, and capacitors C_1. Diode D_4 is reverse bias, consequently, the load is disconnected from the high gain circuit. During the Mode-I capacitor, C_F is responsible for providing load power. Switch S is turned on up to Inductors L_1, L_2, and Capacitor C_1 are sufficiently charged. Mode-I ends at the time of t_2 and Mode-II begins. Mode-II operation of the proposed converter is shown in Fig. 3a, During

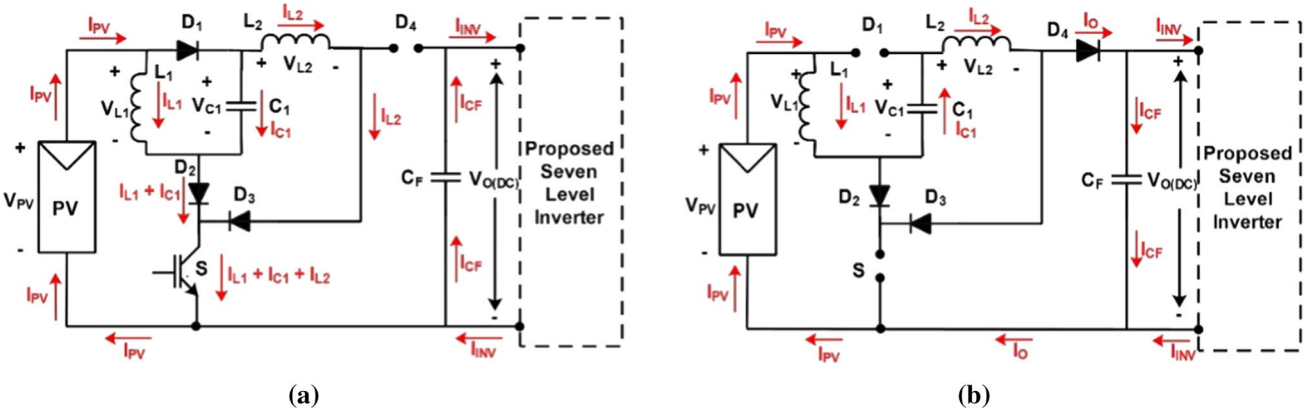


Fig. 3 Mode of operation of SSHGC converter **a** Mode-I (S is ON) and **b** Mode-II (S is OFF)

the mode Switch *'S'* is turned off, the polarity of L_1 and L_2 reversed due to their degradation current, subsequently, D_1, D_2, and D_3 are reverse biased. Diode D_4 is forward biased and C_1, L_1, and L_2 are connected in series with PV and output port.TheL_1, L_2, and C_1 are being discharged. The voltage across the output port($V_{0(DC)}$) is equal to the sum of V_{PV}, V_{L1}, V_{L2}, and V_{C1}. Capacitor C_F is being charged. The Mode-II ends at the time of t_3. The SSHGC voltage gain and design considerations are analysed in chapter-4.

3 Boost Seven-Level Inverter with Triple Voltage Gain

The proposed MLI circuit is shown in Fig. 4. The MLI is designed with a voltage booster and an inverting circuit. The MLI is connected in series with SSHGC. The capacitors C_{I1} and C_{I2} are employed to perform boost operations. The capacitors C_{I1} and C_{I2} are frequently charged from SSHGC output power and discharged through the load to achieve triple voltage gain. The SSHGC output voltage ($V_{DC(BUS)}$)is raised to $2V_{O(DC)}$ and $3V_{O\,(DC)}$with the help of Capacitors C_{I1} and C_{I2}. Five IGBT switches (S_1 to S_5) are used to construct the MLI and the switches are connect the capacitors C_{I1} and C_{I2} with SSHGC output and load. Voltage booster circuits operate in 4 modes, and each mode boosts an SSHGC output voltage with a different voltage level. The circuit model of each mode is shown in Fig. 5a to d. The output of Voltage booster circuits is connected with inverting circuit. Diode D_{I1} and D_{I2} protect the capacitors from self-discharging, and it is forward bias during Mode-I and reverse bias in the rest of the mode. The inverting circuit is connected between the DC bus and AC load. The inverting circuit is made with four IGBT switches (S_6 to S_9). Four anti-parallel diodes connected with IGBT are to allow freewheeling current during operates in inductive loads. The switch S_6, S_7 are positive groups S_8, S_9, are a negative group, and it is operated by load frequency.

Mode-I The equivalent circuit model of Mode-I is shown in Fig. 5a. Switches S_2, S_4, and S_5 are getting pulses and the rest of the switches are in voltage boosting and the inverting circuit is turned off. D_{I1} and D_{I2} are forward biased and allow the current to flow from SSHGC to Capacitors C_{I1} and C_{I2}. The capacitors C_{I1} and C_{I2} are connected across the SSHGC output and are charged independently. The capacitor C_{I1}current is flowing through S_2, D_{I1}, S_5, and capacitor C_{I2} current are flowing through S_4, D_{I2}, and S_5. Capacitor charge current is desired by the State of Charge (SOC) of the capacitors, and it is controlled by Pulse Width Modulation (PWM) technique. Switch S_2, S_4 are subjected to PWM pulses. The maximum charging voltage of the capacitor is SSHGC output voltage ($V_{DC(BUS)}$). During Mode-I, SSHGC output power is only used to charge the capacitors. The voltage across the DC bus is $V_{DC,}$ and the load voltage (V_{OAC}) is zero. Figure 6

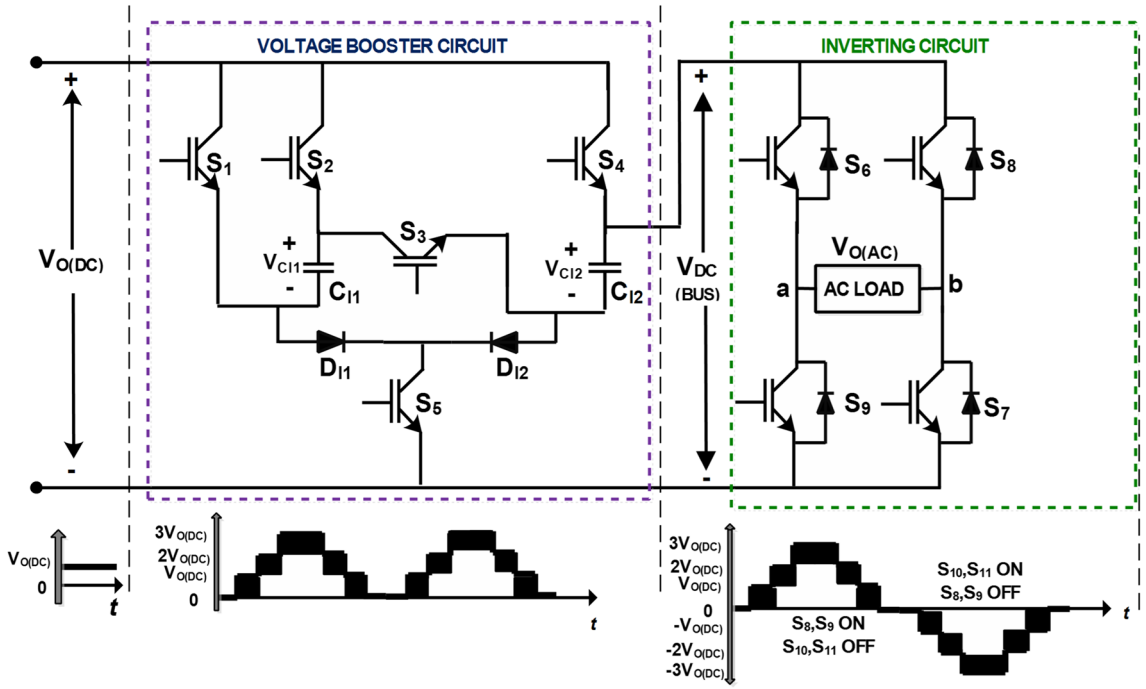


Fig. 4 Circuit configuration of DC–AC multilevel inverter

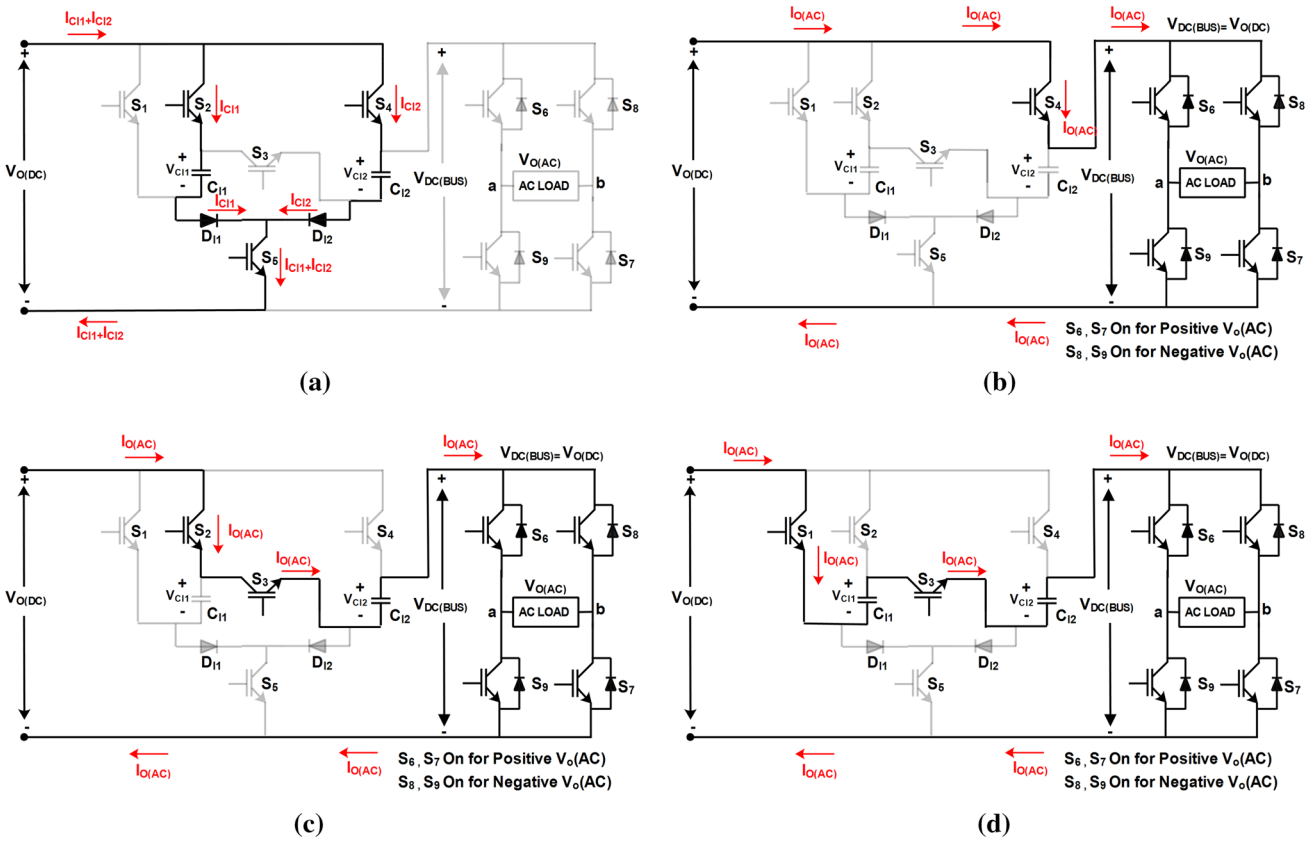


Fig. 5 Equivalent circuit of multilevel inverter **a** Mode-I **b** Mode-II **c** Mode-III and **d** Mode-IV

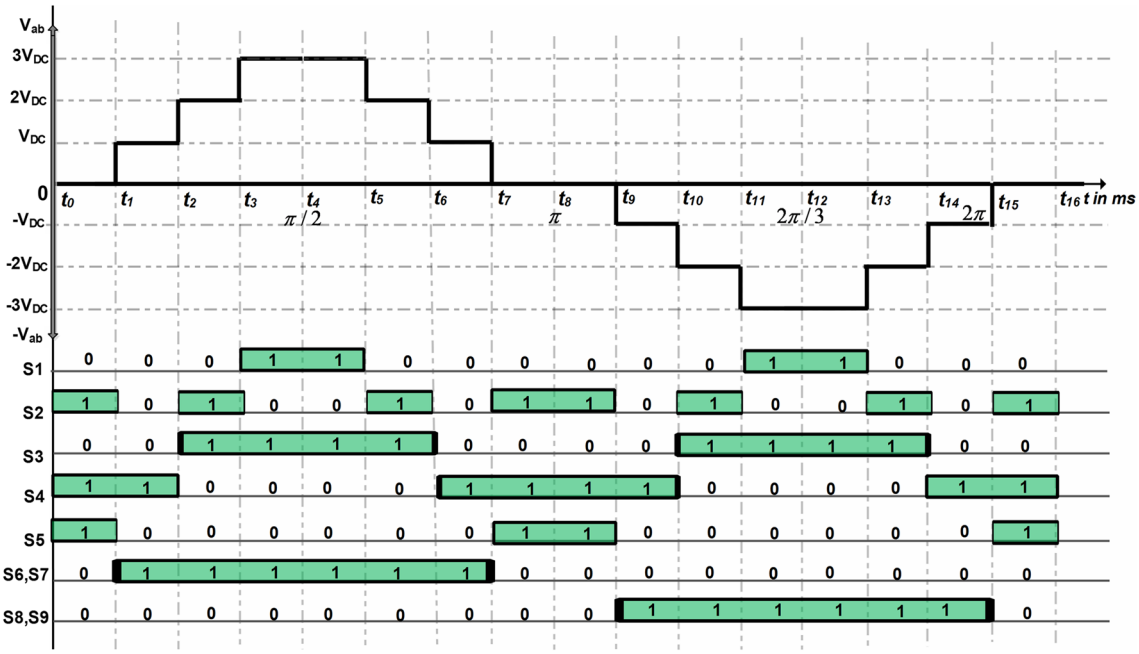


Fig. 6 Switching sequence of the proposed MLI

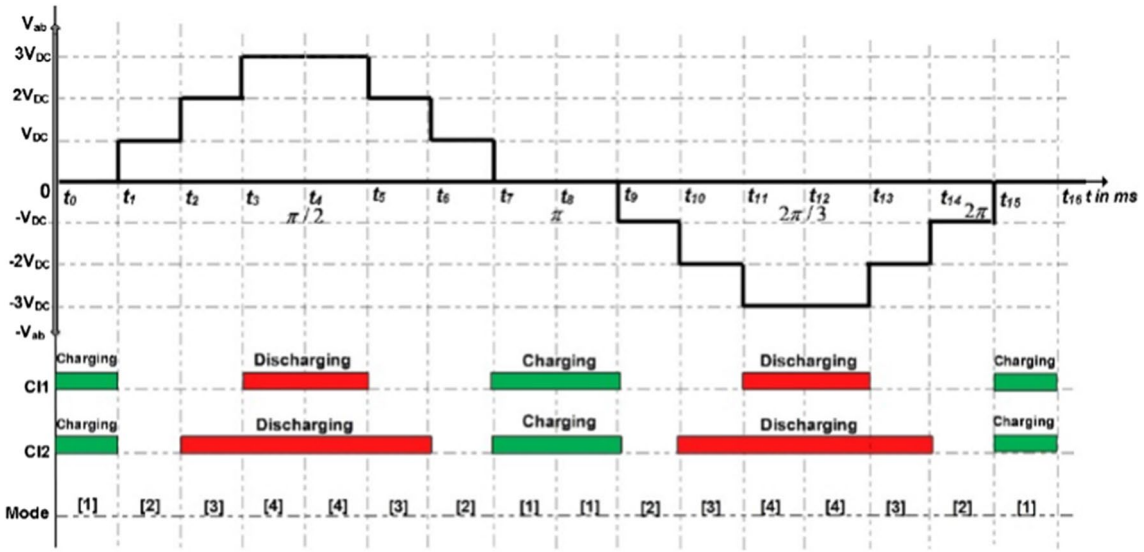


Fig. 7 Charging and discharging waveform of capacitors

shows the switching pulses of each switch in one complete cycle and Fig. 7 shows the charging and discharging profile of each capacitor in one complete cycle.

Mode-II During this mode, the voltage across the DC bus is maintained as MLI input voltage ($V_{O\,(DC)}$). The equivalent circuit model of Mode-I is shown in Fig. 5b. During the mode, Switch S_4 and inverting circuit, positive or negative group switches are operate based on the output voltage. Inverters are subjected to SPWM control to enhance the performance of the inverter. Generally, single-phase two-level inverters are having two legs and switching pulses apply to positive or negative groups, each leg built with two serially connected switches. DC Bus voltage is applied across each leg and load is connected in between the legs. DC bus voltage of the conventional inverters are constant and switches are directly controlled by SPWM. The proposed MLI DC Bus voltage is varying from 0 to $3V_{O(DC)}$, in consequence, SPWM control is limited to apply in inverting circuits. Upon that SPWM is applied to the voltage booster circuit in the proposed MLI. Switch S_4 is subjected to SPWM.

Mode-III During this mode, the voltage across the DC bus is maintained as $2V_{O(DC)}$. *The* Sum of Input DC voltage and capacitor C_{I2} (V_{CI2}) has appeared across the DC bus. The equivalent circuit of Mode-III is shown in Fig. 5c, Switches S_2, S_3 and corresponding inverting circuit switches (either positive or negative group) are operating. Capacitor C_{I2} is connected between the input of the inverter and DC Bus. V_{CI2} is being discharged and the voltage across the capacitor C_{I2} is equal to $V_{O(DC)}$). During the period, the voltage across the DC bus seemed as $2V_{O\,(DC)}$, SSHGC, and CapacitorC_{I2} are responsible to provide the load power. SPWM pulses were applied to switch S_2 and S_4 to withstand the voltage across the DC bus in the range between $V_{O(DC)}$ and $2V_{O(DC)}$.

Mode-IV During this mode, the voltage across the DC bus is maintained as $3V_{O(DC)}$. Sum of Input DC voltage, capacitor C_{I1} (V_{CI1}), and capacitor C_{I2} (V_{CI2}) appear across the DC bus. The equivalent circuit of *Mode-IV* is shown in Fig. 5d, Switches S_1, S_4, and corresponding Inverting circuit switches are operated.C_{I1} and C_{I2} are connected in series between the input of the inverter and DC bus. Capacitors C_{I1}, C_{I2}, and SSHGC are responsible to provide load power. The sum of V_{CI1}, V_{CI2}, and $V_{O(DC)}$) is appeared across DC bus voltage and it is maintained as $3V_{O(DC)}$. The capacitors C_{I1} and C_{I2} and are being discharged. SPWM pulses are applied to switches $S_1$and S_2 in order to control AC load voltage. DC bus voltage is maintained in between $2V_{O(DC)}$ and $3V_{O(DC)}$.

The capacitors are charged during Mode-I and both the capacitors are independently charged from SSHGC output power. The charging and discharging waveform of the Capacitors in MLI is depicted in Fig. 7.The charged capacitors are discharged in Mode-III and Mode-IV. The charging current of the capacitors C_{11} and C_{12} are caused to produce current ripples. The filter capacitor connected in SSHGC is supported to reduce the MLI input voltage and current ripple, The capacitors C_{I1} and C_{I2} are allowed to get a charge from the source during output voltage ($V_{O(AC)}$) is equal to zero.

The capacitors C_{I1} and C_{I2} are provide the load power with SSHGC at one complete cycle is *T/*7 and 2*T/*7respectively. SSHGC alone operate the load during the output AC voltage $V_{O(AC)}$ is equal to $V_{O(DC)}$ and $-V_{O(DC)}$, Along with the SSHGC output, the capacitor C_{12} operates the load at the time of $V_{O(AC)}$is equal to $2V_{O(DC)}$, and $-2V_{O(DC)}$. Along with the SSHGC output, the capacitors C_{I1} and C_{12}operates the load at the time of $V_{O(AC)}$ are equal to $3V_{O(DC)}$and $-3V_{O(DC)}$. The stored energy required to operate the AC load in capacitor C_{I1}

is less than C_{I2}. Two different capacitor values are selected for C_{I1} and C_{I2}. The design consideration of capacitors C_{I1} and C_{I2} is discussed in Sect. 4. The value of C_{I2} is higher than C_{I1}. Voltage sag across the capacitor C_{I1} and C_{I2} during the discharge period has degraded the performance of the AC output, a well-designed control algorithm is used to overcome the issues.

4 Analysis of Proposed SSHGC and MLI Systems

The proposed system consists of SSHGC and MLI stages. The voltage gain of the SSHGC is obtained based on the assuming average inductor voltage at steady state is zero and the SSHGC is operated in continuous conduction mode (CCM). During the Mode-I operations, change in the current of inductor L_1 is formulated as

$$\frac{di}{dt} = \frac{V_{PV}}{L_1}.kT \tag{1}$$

where the SSHGC converter input voltage is V_{PV}, k is the duty cycle of the Switch S, and T is the time period. During Mode-II operation, change in inductor current is formulated as

$$\frac{di}{dt} = \frac{(V_{0(DC)} - V_{PV})}{L_1}(1-k)T \tag{2}$$

where V_0 is the output voltage of SSHGC.

Equating Eqs. (1) and (2)

$$V_{PV}.k = (V_{0(DC)} - V_{PV})(1-k) \tag{3}$$

Rearranging the Eq. (3) to find steady mode voltage gain (V_0/V_{in})

$$\frac{V_{0(DC)}}{V_{PV}} = \frac{3-2k}{1-k} \tag{4}$$

The Voltage gain of SSHGC is compared with other converters to evaluate the performance of the proposed converter. The voltage gain comparison of various duty ratios is made with classical boost, SEPIC, and Super lift Luo converter. The results are depicted in Fig. 8. The results show the voltage gain of SSHGC is higher than other converters at any duty cycle.

The boost inductor L_1 and L_2 are

$$L_1 = L_2 = \frac{(V_{PV} \times D_S)}{f_S \times \Delta I_L} \tag{5}$$

where V_{PV} is input PV voltage, D_S is duty ratio, fs is switching frequency, and ΔI_L is a change in inductor current. While calculating L_1 and L_2 minimum values of D_S is selected to confirm the CCM operations.

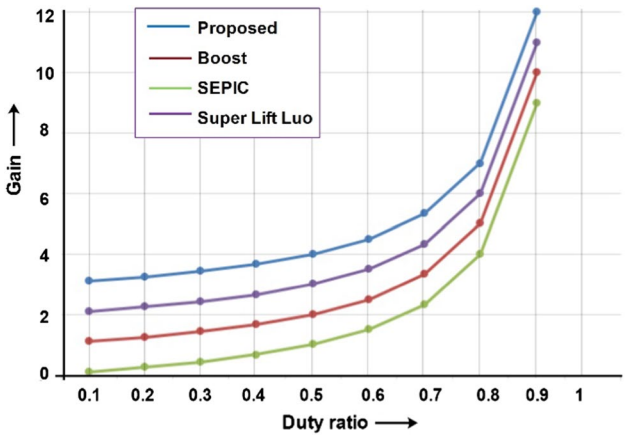


Fig. 8 Voltage gain comparison of proposed SSHGC with Boost, SEPIC, and Luo Converters

The capacitor C_1 stores the energy from the PV module during S is ON stare and connected series with the load during S is OFF to release stored energy. During Mode-II, the output current is flowing through capacitor C_1.

The value of the capacitor

$$C_1 = \frac{I_{O(DC)} \times (1 - D_S)}{f_S \Delta V_{C1}} \tag{6}$$

where $I_{O(DC)}$ is the output current, ΔV_{C1} is a change in capacitor voltage. A high Ds value is selected for calculating C_1 to reduce voltage ripples.

The voltages variation during operation across MLI capacitors are degrade the performance of the inverter. The capacitor C_{I1} is discharged during t_1 to t_5 and t_9 to t_{12}. The capacitor C_{I2} is discharged during t_3 to t_4 and t_9 to t_{10}. During this period, changes in electric charges in capacitors depend on the load current and power factor.

Load active power

$$P_L = V_{0(AC)}.I_{O(AC)} \cos\theta \text{ Watts} \tag{7}$$

where θ is the phase angle between load voltage and current. Cos θ is the power factor of the load.

Active power required for one time period to operate AC load is $P_{L(T)} = P_L \times T$ Watts and one cycle (Capacitor charge and discharge) is

$$P_{L(C)} = \frac{P_L \times T}{2} \text{ Watts} \tag{8}$$

where T is a time period of load fundamental frequency f.

Maximum energy stored in a capacitor is

$$W_C = \frac{C \times (V_C^2)}{2} \text{ Joules} \tag{9}$$

where Vc is Voltage across the capacitor, the amount of Energy transfer is estimated as

$$W_C = \frac{C \times (V_{C(S)}^2 - V_{C(f)}^2)}{2} \text{ Joules} \tag{10}$$

where $V_{C(S)}^2$ is an initial voltage across the capacitor and $V_{C(f)}^2$ is a final voltage across the capacitor.

The relationship between power and energy is

$$P_C = \frac{Wc}{dt} \text{ Watts.} \tag{11}$$

dt is discharging time.

At constant load, the power delivered by the capacitor is

$$P_C = \frac{C \times (V_{C(S)}^2 - V_{C(f)}^2)}{2.dt} \text{ Watts.} \tag{12}$$

Change in voltage across capacitors

$$\Delta Vc^2 = (V_{C(S)}^2 - V_{C(f)}^2) \text{ Volts.} \tag{13}$$

From Eq. (12) The value of capacitor

$$C = \frac{2.P_C.dt}{(V_{C(S)}^2 - V_{C(f)}^2)} \text{ Farad.} \tag{14}$$

The load power requirement is fulfilled by input DC supply, Capacitor I_{C1}, and Capacitor I_{C2}. One cycle is split into eight sectors, out of eight sectors, two sectors are used to charge the capacitors C_{I1} and C_{I2}, and six sectors are delivering power to load. The remaining two sectors DC supply alone provides load power. DCsupply and Capacitor I_{C2} are shared load power during two sectors. DC supply, Capacitor C_{I1}, and Capacitor C_{I2} are shared load power during two sectors. DC supply, C_{I1}, and C_{I2} are fulfilled the total load power requirement in the ratio of 6:4:2 respectively.

Power delivered to load by one complete cycle by

$$\text{DC source is } P_{L(DC(C))} = \frac{P_L \times T}{12} \text{ Watts} \tag{15}$$

$$\text{Capacitor CI}_1 \text{ is } \quad P_{L(CI1(C))} = \frac{P_L \times T}{8} \text{ Watts} \tag{16}$$

and

$$\text{Capacitor CI}_2 \text{ is } \quad P_{L(CI2(C))} = \frac{P_L \times T}{4} \text{ Watts} \tag{17}$$

The value of

$$C_{I1} = \frac{2 \times P_L \times T}{8(V_{CI1(S)}^2 - V_{CI1(f)}^2)} = \frac{P_L \times T}{4(\Delta V_{CI1}^2)} \text{ Farad} \tag{18}$$

and

$$C_{I2} = \frac{2 \times P_L \times T}{4(V_{CI2(S)}^2 - V_{CI2(f)}^2)} = \frac{P_L \times T}{2(\Delta V_{CI2}^2)} \text{ Farad} \tag{19}$$

where ΔV_{CI1} and ΔV_{CI2} are changes in capacitors voltage during discharge. Low ΔVc, reduced voltage sag in output AC voltage.

The performance analysis of the proposed MLI is tabulated in Table 1 to highlight their relative distinctions. Essential parameters like voltage gain, number of input DC sources, number of semiconductor switches, and Output AC voltage level is compared and tabulated. The major shortcoming of the latest MLI topologies presented in [28–30] is the requirement of more than one DC source. Minimum three DC sources are required to produce seven-level output. Higher voltage levels of MLI AC voltages to reduce THD and ensure smooth operations. The topologies presented in [27] are used three H-bridge circuits and more quantity of semiconductor switches. The proposed MLI is developed with only 9 semiconductor switches to achieve seven levels of voltage output with triple voltage gain by using a single source.

5 Simulation and Experimental Result

Matlab simulation and hardware are realised to analyse the superiority of the proposed SSHGC and MLI system. Experimental analysis is carried out with a 200 W load. 24 V, 200 Watts module is used to feed DC power to the SSHGC converter. Modified P&O MPPT technique is applied to ensure maximum power utilisation of PV module. The SSHGC is developed with a High-speed IGW60N60H3 IGBT with a switching frequency of 25 kHz. The Photo image of the Hardware Prototype of the Proposed System is shown in Fig. 18. The SSHGC input PV voltage (V_{PV}) and current (I_{PV}). The simulation and experimental results are shown in Figs. 9, 10, 11, 12 and 13. The input DC voltage of SSHGCis maintained as 24 V and the current is 8.2 A. Isolation level of the PV module is set to 1000 W/M^2, the temperature

Table 1 Comparison of proposed MLI with other latest MLI

Reference	DC sources used	Output Level	Semiconductor switches	Voltage gain
Proposed boost seven level inverter	1	7	9	3
Ref. [27]	1	7	16	3
Ref. [28]	3	7	10	1
Ref. [29]	4	13	10	1
Ref. [30]	4	17	10	1

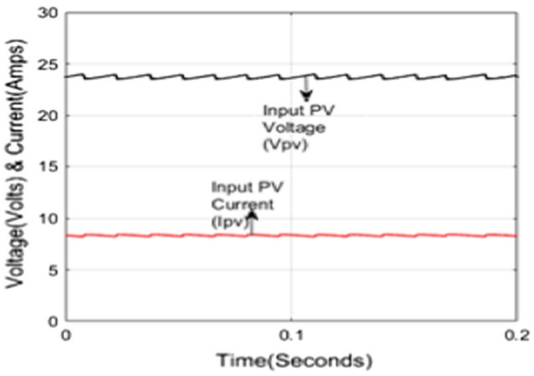


Fig. 9 Simulation of SSHGC input voltage and current

is 25^0 C and 200 Watts power is fed to SSHGCconverter. Small variation has arisen in input voltage and current Due to MPPT.

The L_1 and L_2 values are selected as100 mH and the C_1 is 200 µF, 63 V are used. The voltages waveform across the L_1, L_2, and C_1, are shown in Fig. 10. The voltage across the $L_1$and L_2 are positive at Mode-I. During the period PV energy is stored in inductors L_1, L_2, and C_1. The voltage across the L_1 and L_2 are negative at Mode-II. During the period stored energy in inductors L_1, L_2 and C_1 are transferred to load. The voltage across the capacitor and inductors currents is always positive. Charging and discharging voltages are equal in both the inductors. Change in capacitor voltage $\left(\Delta V_{C1}\right)$ during operation is degrade the voltage gain performance of the SSHGC.

The waveform of SSHGC output voltage ($V_{O(DC)}$) and Current ($I_{O(DC)}$) simulation waveforms are shown in Fig. 11

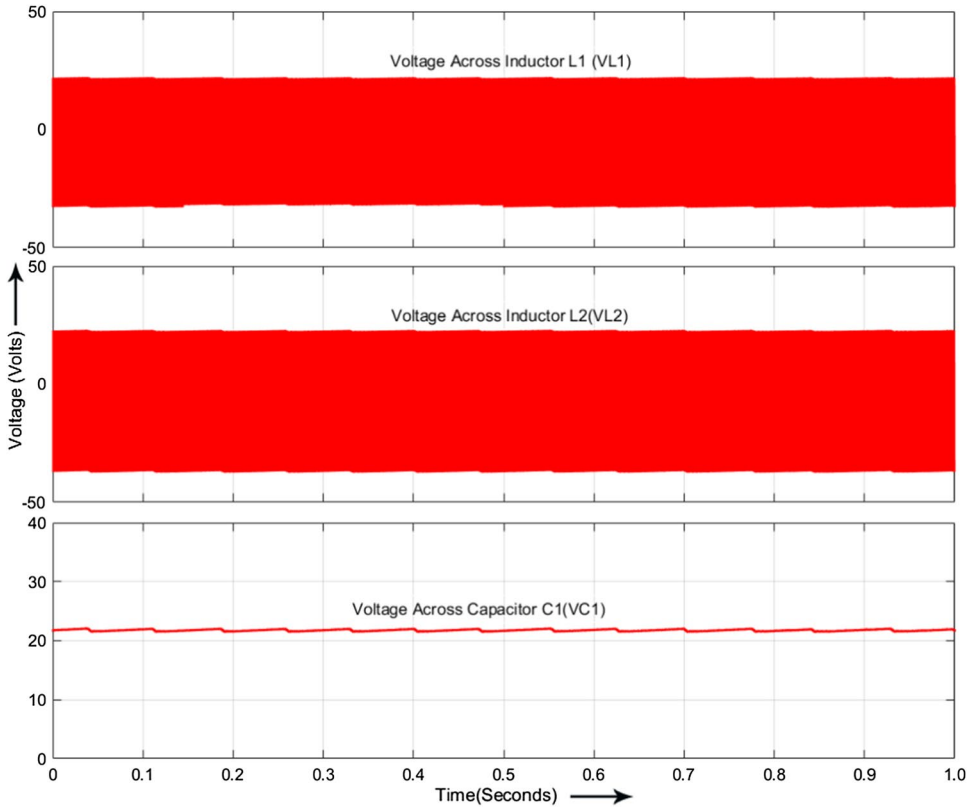


Fig. 10 Voltage across L_1, L_2, and C_1

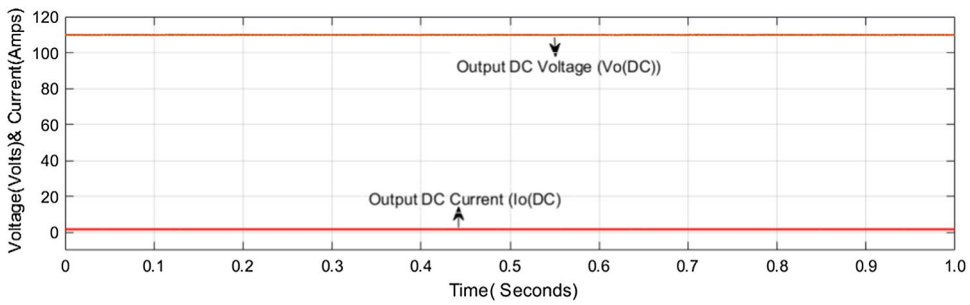


Fig. 11 Simulation result of SSHGC output voltage ($V_{O(DC)}$) and current ($I_{O(DC)}$)

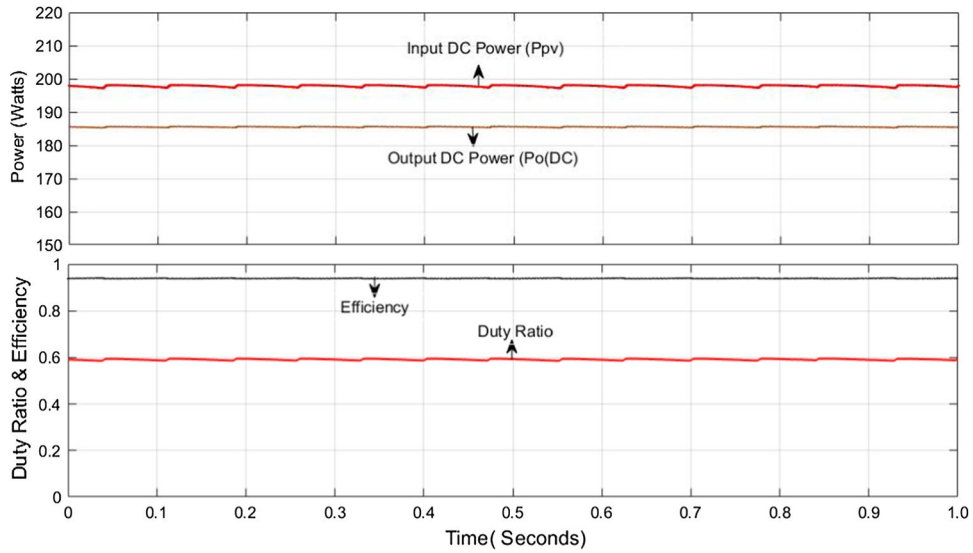
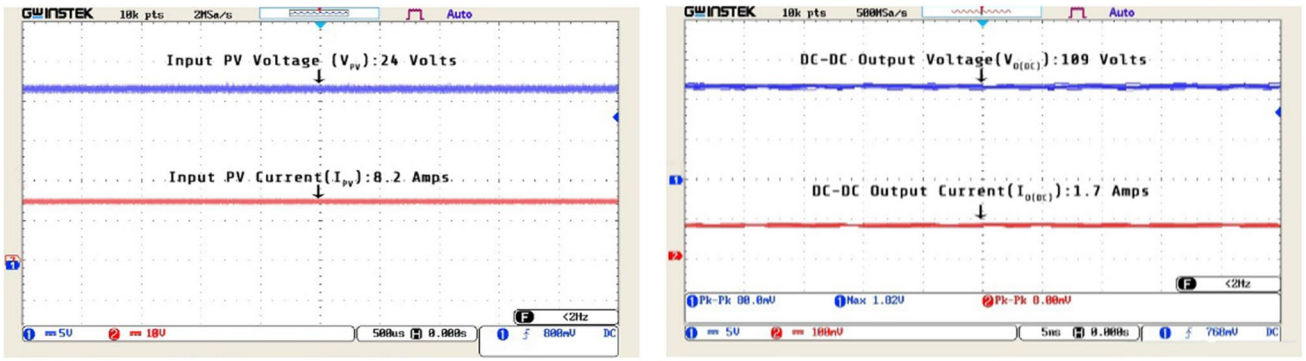


Fig. 12 SSHGC converter power, efficiency, and duty ratio



(a) **(b)**

Fig. 13 Hardware result of SSHGC converter **a** input voltage (V_{PV}) and current **b** output voltage ($V_{O(DC)}$) and current ($I_{O(DC)}$)

and experimental waveforms are shown in Fig. 13b. MPPT algorithms are operated in SSHGC with a duty ratio of 0.6. The gain of the SSHGC is.

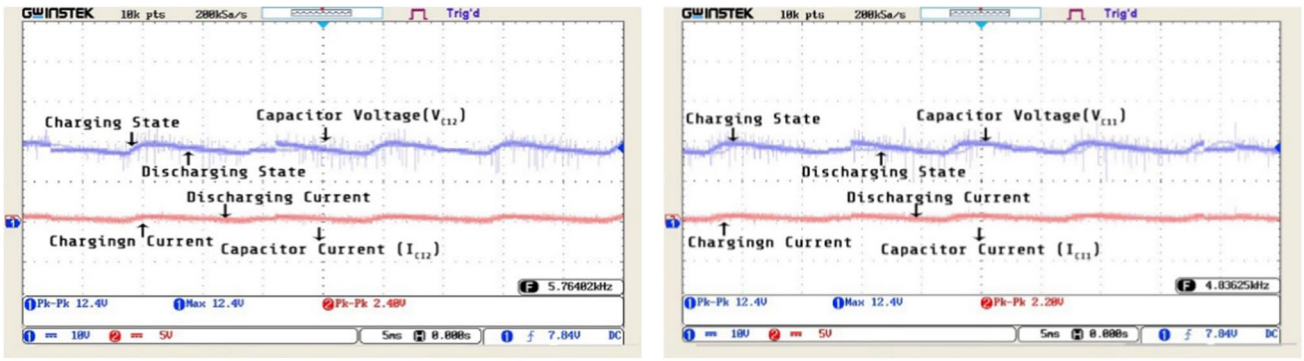
$$\frac{V_0}{V_{in}} = \frac{3-2k}{1-k} = \frac{3-2\times(0.6)}{1-0.6} = 4.5$$

The input voltage V_{PV} is 24 V and the voltage gain of the SSHGC is 4.5. The output voltage and current reach to 109 V and 1.7 A respectively.1000 µF, 200 V filter capacitor is used.

Proposed SSHGC power and efficiency curves in the maximum power point condition are shown in Fig. 12. 200 W solar power is fed to SSHGC, and the output port power is measured as 185 Watts. The efficiency of the SSHGC converter is achieved as 92.5%.

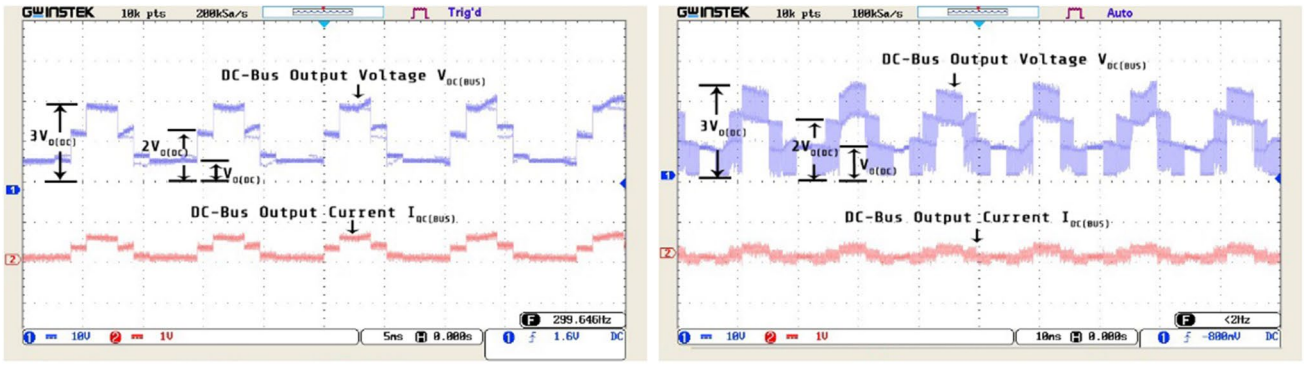
The output power of the SSHGC converter is fed to the proposed MLI. The capacitors C_{I1} and C_{I2} are used to increase the gain and level of MLI. Capacitors C_{I1} and C_{I2}values are obtained by using Eqs. (18) and (19). Active load power and time period are deliberated to calculate C_{I1} and C_{I2}. The value of C_{I1} and C_{I2} are 500 µF, 200 V and 1000 µF, 200 V for 200 W, 50 Hz load. The voltage rating of the capacitors are selected based on the SSHGC output voltage, electrolyte capacitors are selected for a C_{I1} and C_{I2}. The voltage and current in capacitor C_{I1} and C_{I2} are shown in Fig. 14. During charging, the voltages and currents of the capacitors are positive and negative for discharging. Ten percentage of change in the capacitor voltage (ΔVc) is allowed during discharging.

The Voltage across DC Bus is shown in Fig. 15. During the period t_0–t_1, t_7–t_9, and t_{15}–t_{16} are capacitors C_{I1} and C_{I2} are getting a charge from the SSHGC. The voltage across the DC bus is equal to $V_{O(DC)}$. The voltage across C_{I2} is appeared across DC Bus and during the charging mode load is disconnected through switches S_1, S_2, S_3, and S_4. The switches S_1, S_2, S_3, and S_4 are operated to connect the capacitors with the DC bus to produce DC bus voltage is



(a) **(b)**

Fig. 14 Voltage and current **a** capacitor C_{I1} **b** capacitor C_{I2}



(a) **(b)**

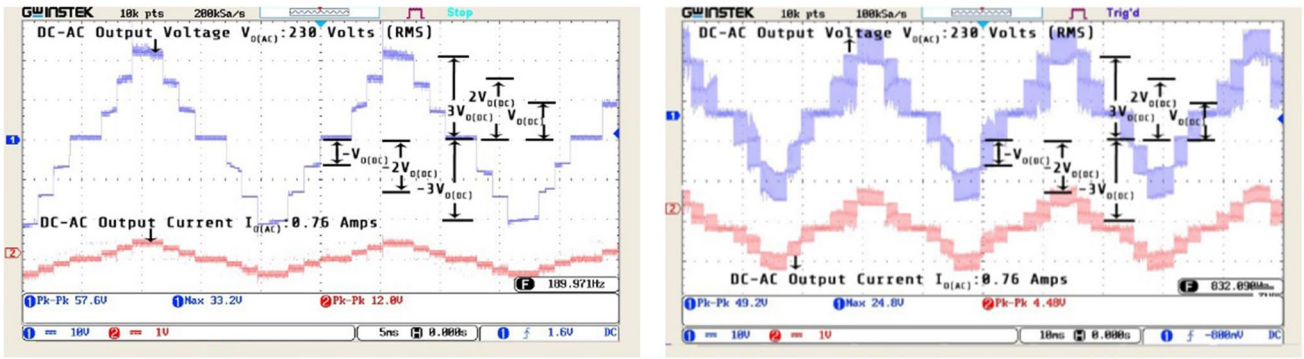
Fig. 15 DC bus voltage and current **a** constant switching pulse **b** SPWM

equal to $V_{0(DC)}$, $2V_{0(DC)}$, and $3V_{0(DC)}$. DC bus voltage when the constant switching pulses are applied to switch S_1 to S_4 is shown in Fig. 15a. When the switches are enabled with constant pulses, the voltage across the DC bus is seemed as $V_{0(DC)}$, $2V_{0(DC)}$, and $3V_{0(DC)}$.SPWM is used to improve the efficiency of the system and the THD of the AC output is also reduced. Switches S_6, S_7, S_8, and S_9 are used to convert the DC bus voltage into AC voltage. SPWM pulses are applied to switches S_1, S_2, S_3, and S_4.

Figure 15b shows the DC bus voltage when the SPWM pulses are applied to switch S_1 *to* S_4. During the period (t_1–t_2) the SPWM pulse applied to switch S_4 and the DC bus voltage exist between $V_{0(DC)}$ and Zero, (t_2–t_3) SPWM pulses are applied to S_2 and S_4. The switch S_4 gets the complementary pulse of S_2, (t_3–t_4) SPWM pulses are applied to S_1 and S_2. The switch S_2 gets the complementary pulse of S_1. During the period t_2–t_3, the voltage across the DC bus exists between $V_{0(DC)}$ and $2V_{0(DC)}$, the period between t_3–t_4 the Voltage across DC bus exists between $2V_{0(DC)}$ and $3V_{0(DC)}$.

The output load voltage and load current across the resistive load are shown in Fig. 16a and b. Load is connected across the output of the seven-level inverter. Figure 16a shows the load voltage and current when constant pulses to switches S_1–S_4. Figure 16b shows the load voltage and current when the SPWM pulses to switches S_1–S_4. In both cases, the load voltage and current are in phase. Small voltage variation in the output voltage is existed due to the voltage variation of capacitors during discharge.

The DC–AC inverting system, output AC power should meet the IEEE Std 519. The percentage of THD value is essential in DC–AC inverter design. The AC voltage and current should be less than 3% of THD value in order to drive all kinds of AC load. More THD value creates undesirable factors like harmonics and power quality issues. THD Analysis is performed in the proposed inverter and results are shown in Fig. 17. The results show the THD value is 0.18% when it feeds the AC power to a resistive load (Fig. 18).



(a) (b)

Fig. 16 AC output voltage and current **a** constant switching pulse **b** SPWM

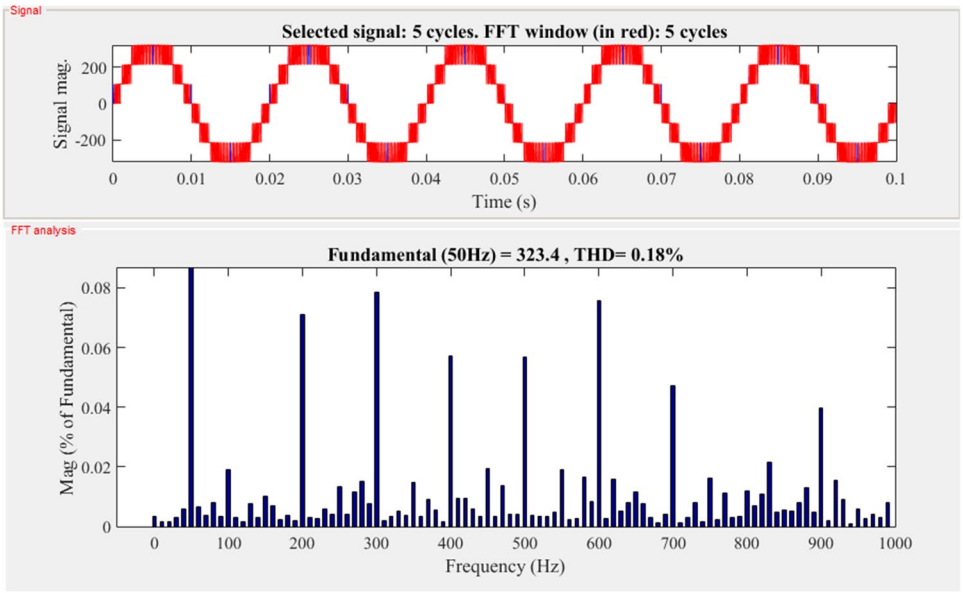


Fig. 17 THD analysis of load voltage

6 Conclusion

A high gain DC–DC–AC converter is proposed. Gain is achieved in both DC–DC and DC–AC Conversion. The comparative gain analysis shows the significance of the proposed SSHGC. P&O algorithm is used to extract maximum Power from PVM. The output of the DC–DC converter is fed to MLI. The proposed inverter has the unique future of triple voltage gain and generates seven-level AC output. The switching capacitor technique is used in the inverter circuit in order to achieve more voltage gain. The hardware prototype is designed to validate the proposed system. The Experimental results are verified with theoretical analysis and simulation results. SPWM technique is used to control the inverter to improve the quality of output AC voltage. The maximum voltage gain of the DC–DC

Fig. 18 Hardware prototype of the proposed system

converter is 12, and DC–AC Inverter is 3. The overall voltage gain of the proposed system is 36. The efficiency of the DC–DC converter is 92.5%, and the DC–AC inverter is 93%. The overall efficiency of the system is 86%. THD of the AC output is 0.18%. The significant advantage of the proposed DC–DC–AC converter is its simple topology, the excellent tackling capability of MPPT control, Voltage gain is achieved in DC–DC and DC–AC stages. The proposed DC–DC–AC system is suitable for PV-based standalone and grid-connected systems.

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