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ORIGINAL ARTICLE

A Novel Sliding Mode Based UPQC Controller for Power Quality Improvement in Micro-Grids

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Abstract
This paper presents a novel State Observer Based Sliding Mode controller for UPQC inverters to enhance the power quality in microgrids. In the proposed control scheme, Enhanced extended state observer was applied on a standard sliding mode controller to boost its disturbance rejection capability. The controller was designed to be robust against parameteric and external uncertainties. Further, affordable UPQC-grid integration scheme suggested where the photovoltaeek system could be connected to the network via UPQC inverters. Using the suggested configuration the active and reactive power injection capability was added to UPQC along with its commonly known advantages. Extensive MATLAB Simulink-based theoretical and experimental studies were conducted in different scenarios to verify the efficiency of the proposed method in improving the power quality indices. Using UPQC with the proposed control scheme shows the better performance than the current traditional UPQC controllers in voltage sag reduction and Harmonics minimization. The main feature of the proposed controller included its accuracy and fast tracking response.

Keywords Power quality · Micro-grid · UPQC · Inverter · Sliding mode control

1 Introduction

Reductions in greenhouse gas emissions, competition policies, diversification of energy sources, and global power requirements have given rise to the interest in micro-grid (MG) schemes [1]. Use of distributed generation units imposes various power quality related problems in distribution networks such as voltage sag or swell, reverse power flow, voltage imbalances, harmonic distortion, and interruptions [2]. The high penetration of renewable power generating resources interfaced with power electronic devices in microgrids along with increased none-linear loads has attracted the attention to develop dynamic and adjustable solutions to cope with the power quality problems. In this regard, use of custom power devices such as UPQC can provide effective means for addressing poor power quality in grids connected or islanded MGs.

The UPQC employs two active power filters (APF) (voltage source inverters) which are connected to a DC link capacitor. One of these two APFs is connected in series with the AC line, while the other is connected in shunt with the same line [3]. To eliminate negative sequence currents and harmonics shunt, an active filter will be in operation with series active filter reducing voltage distortion and imbalances. Several research works have been conducted on control schemes for UPQC's filters for obtaining flexible control algorithms and fast tracking response to obtain the inverters' switch control signals [4–6]. Artificial Intelligence (AI) methods are currently under extensive application in this regard to offer global optimum or closer global optimum values for switching signals. In [7], genetic algorithm (GA) was applied to determine the parameters of the shunt and series active filters. The artificial neural network (ANN) was considered as a tool to design control circuitry for UPQC in distribution network in [8]. The AI tools are able to give solutions to power system problems if the problem features and the AI tool features match each other. Further, depending on the initial values, hardware dependence, premature convergence, and tracking local optimum are the demerits

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that reduce trust in an AI-based controller performance [9, 10].

There are also a number of classical control schemes for UPQC. In [11], a mixed linear quadratic regulator with an integral action control technique was applied to a UPQC to keep regulation and stability under sever load variations. Elsewhere, [12] presented a classic discrete-time control model for a three-dimensional space vector pulse width modulation (3D-SVPWM) to be used with a dual UPQC, for obtaining a fixed commutation frequency and a low computation cost. Classical approaches for obtaining optimum control use time-consuming trial and error and provide sub-optimal control when several parameters are to be optimized at the same time.

This paper presents real-time control of a unified power quality conditioner using second-order ESO-based sliding mode controller (ESOSM) to improve the power quality of MGs. Distinguishing features of the sliding mode control such as insensitivity to bounded matched uncertainties, order reduction of sliding motion equations, decoupling design procedure, and zero-error convergence of the closed-loop system are the main motivations for choosing ESOSM as the UPFC control method [12].

Besides, numerous research projects carried out to improve fabrication technology, evaluation and test scheduling of semiconductors in control circuitry. The results of these projects can easily be implemented in UPQC's control circuits. In [13, 14] different techniques for minimizing test time in system on chip (SoC) overviewed and new methods introduced to reduce production costs of controlling microchips by minimizing the test time of each SoC.

The controllers proposed for UPQCs have always relied on a fixed grid frequency [15, 16]. Since grid frequency variations in MGs are larger than those experimented in classical distribution networks, they must be considered in the controller designation. In the proposed control scheme, not only variations of angular frequency of the grid but also the other model uncertainties such as smoothing inductor L and parasitic phase resistance r are fully considered. The main contributions of the paper can be summarized as follows:

- Introduction of an effective technique for regulating DC-link voltage and testing its significance.
- Implementation and evaluation of the proposed method and the PQ problem compensating performances to be analyzed in different scenarios.

Comparative analysis of the effectiveness of the proposed methods and conventional methods.

2 Problem Formulation

2.1 System Dynamic

The general configuration of UPQC is shown in Fig. 1, where the series and shunt voltage source inverters (active filters) are connected via a DC-link energy storage capacitor on the DC side. To eliminate negative sequences' current and harmonics shunt, an active filter will be in operation where the series active filter reduces voltage distortion and imbalances. The power transfer between the network and DG resources in interconnected and separated mode can be expressed by Eqs. (1) and (2) respectively:

$$P_{gri} + P_{DG} = (P + Q + H)_{load} + P_{loss} + P_{series} + P_{Storage} \quad and \quad (Q + H)_{shunt} = -(Q + H)_{load} \tag{1}$$

$$P_{DG} + P_{Storage} = (P + Q + H)_{load} + P_{loss} \quad and (Q + H)_{shunt} = -(\mathrm{Q} + H)_{load} \tag{2}$$

where P, Q, and H represent active, reactive, and harmonic powers. The dynamic equations of system in the d − q synchronous reference frame can be written as:

$$L\frac{di_{inj_d}}{dt} = -ri_{inj_d} + \omega Li_{inj_q} + u_{load_d} - MU_{DC} \tag{3}$$

$$L\frac{di_{inj_q}}{dt} = -ri_{inj_q} + \omega Li_{inj_d} + u_{load_q} - MU_{DC} \tag{4}$$

$$C\frac{dU_{DC}}{dt} = M\left(i_{inj_d} + i_{inj_q}\right) - i_{load} \tag{5}$$

where u_{load_d} and u_{load_q} represent load voltages, U_{dc} is the DC-link voltage, i_{inj_d} and i_{inj_q} denote the injected current of the shunt active filter, M is the switching functions, and ω is the main grid angular frequency. Reduced number of equations,

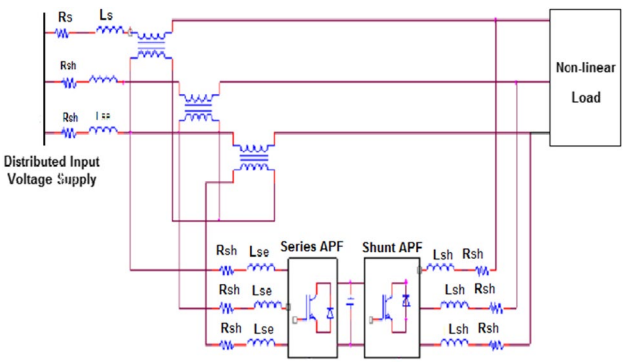

Fig. 1 General structure of UPQC

less complexities, and easier control tasks have been the main motivations to use d − q synchronous reference frame in this paper.

2.2 UPQC Integration Strategy and Modeling

There are several strategies to connect a UPQC to the grid. The integration scheme of UPQC to the MG in this paper has been inspired by [17] where the placement, integration, capacity enhancement, and real-time control of the UPQC are investigated. In the proposed method, the photovoltaic system and its storage devices are connected to the grid through UPQC inverters (Fig. 2). Use of this strategy will be economically helpful as high cost of application has always been considered the UPQC drawback [18]. In addition, in this scheme the UPQC will be capable of injecting active power to the network in the case of any changes in the load demand, utility power delivery failure, or variations in the other DG generations. The next section will further discuss that the controller design is such that any changes in the load side active power will be considered as a disturbance and will be attempted to be compensated.

To achieve the same behavior with the real system, common assumptions in parameter uncertainties in UPQC modeling have been avoided in this paper. To guarantee controller robustness, parameters' uncertainties in the system and UPQC converters model are fully considered using the following formulations:

$$L = L_0 + \Delta L, r = r_0 + \Delta r, \omega = \omega_0 + \Delta\omega \tag{6}$$

where L_0, r_0, and ω_0 are nominal values of smoothing inductor, parasitic phase resistance, and the angular frequency of the grid, respectively. Also, ΔL, Δr, and $\Delta\omega$ are their variation which represent parametric uncertainties.

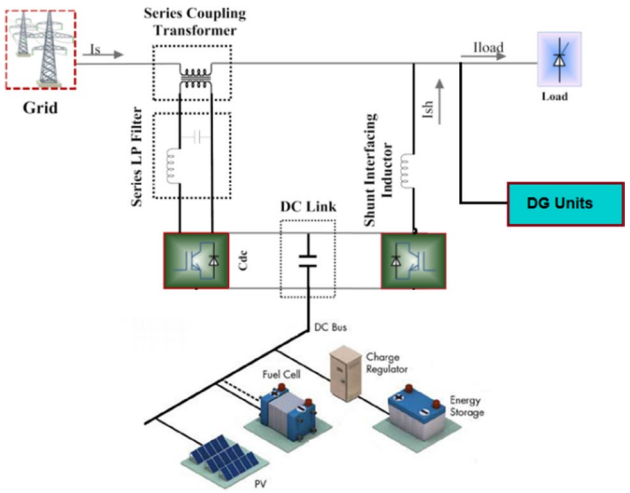

Fig. 2 UPQC integration Scheme

2.3 Control Objectives

The first problem of control is to produce a suitable shunt filter injected current (i_{inj}) to eliminate harmonics in the load side current. i_{inj} is controlled indirectly by processing the actual source current and the estimated reference current. The reference value for i_{inj_d} should be determined such that the DC-link current remains constant. The more it is constant, the more linear the system will be.8 Further, i_{inj_q} should be regulated so that it injects a desired compensating reactive power. Thus, tracking reference values by i_{inj_d} and i_{inj_q} is the first control objective. At the same time, as the second control objective, the DC component of the DC-link capacitor voltage should be driven to its reference value.

3 Controller Design

In the MG structure, there are various kinds of disturbances such as parametric uncertainties, load variations, and changes in generation of the other DG units. Thus, the controller should have strong disturbance rejection ability to meet the control objectives efficiently. In the proposed controller, two controlling loops are implemented consisting of an inner loop for current tracking and voltage regulation loop, the outer loop. Super twisting algorithm (STA) is applied in the inner loop to ensure the quick convergence of i_{inj_d} and i_{inj_q} to their reference values. Extensive state observer is designed to estimate variations of the load power which is accounted as an external disturbance. Using estimated disturbance, a parallel STA regulates the DC link capacitor voltage.

3.1 Basic STA

The sliding mode controller changes the dynamics of the nonlinear system by applying a control signal pushing the system's orientation to slide along a desired sliding surface. In the sliding mode control, uncertainties and disturbances are addressed efficiently without any need to understand the precise model of the system to extract control rules [19].

Sliding mode control scheme includes two steps: selecting the sliding surface in the state/error space, called the switching function, so that the sliding motion would satisfy the control specification, and selecting a control law which makes the selected sliding surface desirable to force the system trajectories slide on the surface. The general designation of a sliding mode control would be as follows:

$$\dot{x}_i = x_{i+1},\ i = 1, 2, \ldots, n-1 \tag{7}$$

$$\dot{x}_n = F(t, x, u) + D$$
$$y = x_1,$$

where $x = \left[x_1 + x_2 + \ldots x_n\right]^T$ represents the system state vector,u is the control input, F(t, x, u) denotes nonlinear continues function with a known structure, y is the system output vector, and D is external disturbance.

To accomplish the control objective, s and its derivatives should be forced to zero.

$$\dot{s} = \frac{\delta}{\delta t}s(t, x) + \frac{\delta}{\delta x}s(t, x)[a(x) + b(x, u)] \tag{8}$$

$$s = \frac{\delta}{\delta t}\dot{s}(t, x, u) + \frac{\delta}{\delta x}\dot{s}(t, x, u)[a(x) + b(x, u)] + \frac{\delta}{\delta u}\dot{s}(t, x, u)\dot{u} = \varphi(t, x, u) + \gamma(t, x, u)\dot{u} \tag{9}$$

To ensure stability of the control action, the following boundary conditions must be satisfied:

$$0 < \Gamma_m < \gamma(t, x, u) < \Gamma_M \tag{10}$$

$$-\Phi \le \varphi(t, x, u) \le \Phi \tag{11}$$

Under foregoing conditions, the control law of a super-twisting sliding mode controller is obtained as follows:

$$u = u_1 + u_2 \tag{12}$$

$$\dot{u}_1 = -\alpha \text{sign}(s) \tag{13}$$

$$u_2 = -\lambda |s|^{\frac{1}{2}} \text{sign}(s) \tag{14}$$

Using boundary conditions, α and λ can be calculated as:

$$\alpha > \frac{\Phi}{\Gamma_m}, \lambda^2 \ge \frac{4\Phi}{\Gamma_m^2}\frac{\Gamma_M}{\Gamma_m}\frac{\alpha + \Phi}{\alpha - \Phi} \tag{15}$$

3.2 Enhanced Extended State Observer

Extended state observer (ESO) has been implemented in the control scheme to deal with uncertainties and rejection of external disturbance simultaneously. Feed forward compensation of the control law by ESO improves tracking performance and disturbance rejection ability of the control system. The key to ESO design is to consider the external disturbance as an additional state of the dynamic system. Accordingly, system dynamics (7) is extended as follows:

$$\dot{x}_i = x_{i+1}, \quad i = 1, 2, \ldots, n-1 \tag{16}$$

$$\dot{x}_n = F(t, x, u) + x_{n+1}$$
$$\dot{x}_{n+1} = \varepsilon(t)$$
$$y = x_1,$$

where $\varepsilon(t)$ is the derivative of D.

Motivated by the design theory in [20], the proposed linear ESO will be proved and designed in this section. To design the ESO, Eq. (5) can be restated as:

$$C\frac{dV_{dc}}{dt} = \frac{1}{V_{dc}}(p^* - pload) \tag{17}$$

where, $p^* = i_d v_d + v_q i_q$ and $pload = V_{DC} I_{LOAD}$.

The proposed linear ESO has the following state space representation:

$$C\dot{z} = p^* - d(t) \tag{18}$$

$$C\dot{\hat{z}} = p^* - \dot{\hat{d}}(t) + \beta_1(z - \hat{z}) \tag{19}$$

$$\dot{\hat{d}}(t) = -\beta_2(z - \hat{z}) \tag{20}$$

where β_1 and β_2 are positive gains and should be chosen such that system remains constant. The error dynamic can be stated as:

$$\dot{\varepsilon} = A\varepsilon + \Psi \tag{21}$$

where, $\varepsilon = \left[\varepsilon_z, \varepsilon_d\right]^T$, $A = \begin{bmatrix} -\frac{\beta_1}{C} & -\frac{1}{C} \\ \beta_2 & 0 \end{bmatrix}$ and $\Psi = [0\ h(t)]^T$.

3.3 Current Tracking Loop

For a fixed operating point, the transfer function of an inverter can be expressed as: 8

$$K_C = \frac{\nabla I_{DC}}{\nabla i_{inj}} = 3\left(\frac{u_{sh} - c_{sh}u_{sh}s - 2i_{inj}R_{sh}}{L_{DC}I_{DC}s}\right) \tag{22}$$

The block diagram of the current control loop is illustrated in Fig. 3. The characteristic equation of the current control loop has been proved in 8 and can be rewritten as:

$$1 + (K_p + \frac{K_i}{s}) \times 3 \times \left(\frac{u_{sh} - c_{sh}u_{sh}s - 2i_{inj}R_{sh}}{L_{DC}I_{DC}s}\right) = 0 \tag{23}$$

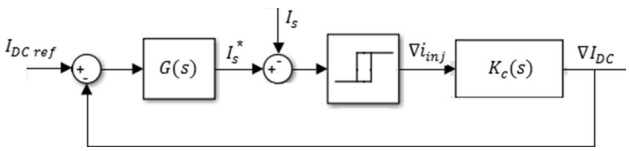

Fig. 3 Block diagram of current control loop

K_p determines the current response and K_i defines the damping factor of the current control loop.

4 Simulation and Results

To validate the effectiveness of the proposed control system, MATLAB/Simulink based simulation was conducted in this section for investigating the voltage sag and current harmonics compensation capability of the UPQC. The system parameters utilized for simulation are listed in Table 1.

A comprehensive analysis was done in two different scenarios:

Scenario I: in this scenario, harmonics elimination capability of UPQC under highly nonlinear loading condition was examined while there was no voltage sag. Since there was no voltage deviation in the load voltage (no fault condition), the series inverter operated in the standby mode and as shown in Fig. 4, no voltage was injected by this inverter. Meanwhile, the shunt converter was in operation to eliminate the current harmonics. Figure 5 illustrates the load current, injected current, and source current respectively. It is evident that because of the presence of UPQC current harmonics have been compensated effectively. After compensation, as can be seen in Fig. 6, the total harmonic distortion (THD) in source current has been low i.e. 0.61% as compared to that of the load current i.e. 25.08% (Fig. 7). Table 2 compares the UPQC performance in harmonic filtration in this scenario under a simple PI controller, enhanced phase-locked loop controller [EPLL] [21], and SOSM controller. While the load current in all cases is found to be content of all odd harmonics, providing THD of 25.08%, THD of source current has been reduced to 8.53%, 2.71%, and 1.79% using PI, EPLL, and SOSM controllers respectively. Table 3 reports the harmonic contents of the load side current and source

Table 1 Study system parameters

System	Parameter	Value
Power system parameters	Line to line nominal voltage	11 kV
	frequency	50 HZ
	Line impendence	0.0015 + j0.078 Ω
	Linear load	5.5 kw + j5.5 kvar
	Nonlinear load	101 + j130.66 Ω
Series APF	Filter resistance	0.047 Ω
	Filter capacitor	300 μf
	Filter inductor	1.56 mH
	Nominal power	800 kVA
Shunt APF	Filter inductor	0.4 mH
	DC-link capacitor	40 mF
	DC-link nominal voltage	1700 v

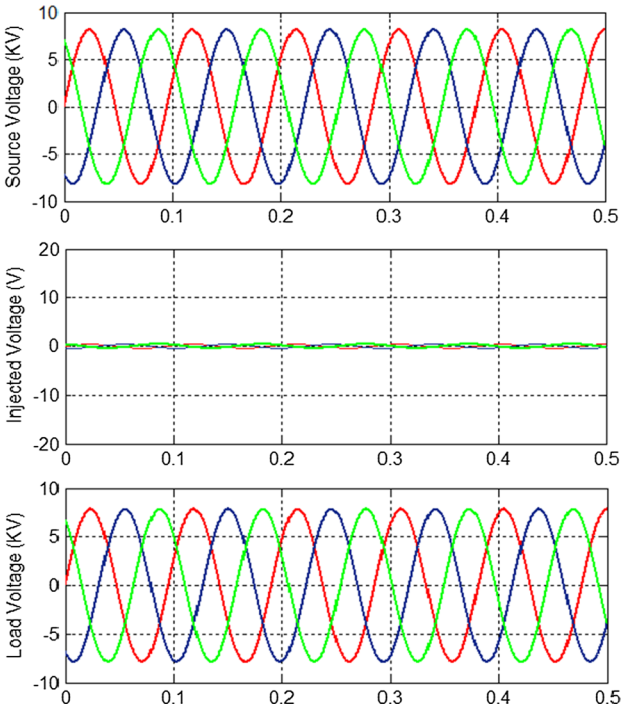

Fig. 4 Source, load and injected voltage for scenario I

current for phase A in the presence of the UPQC with the proposed controller. The values of this table are obtained by FFT analysis of the load and source currents (Figs. 8, 9). The DC link voltage wave-form is demonstrated in Fig. 6. In addition to normal advantages of implementing UPQC in grids, the power injection capability of the proposed configuration is obvious in Fig. 7. The load, source, series and

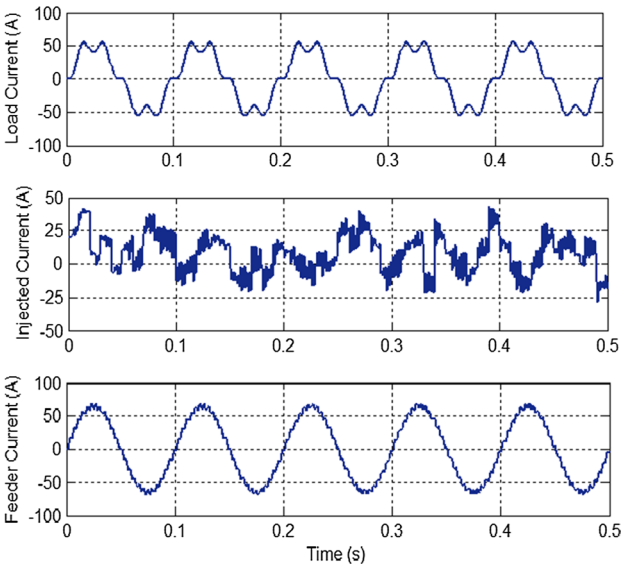

Fig. 5 Feeder, load and injected current of phase A for scenario I

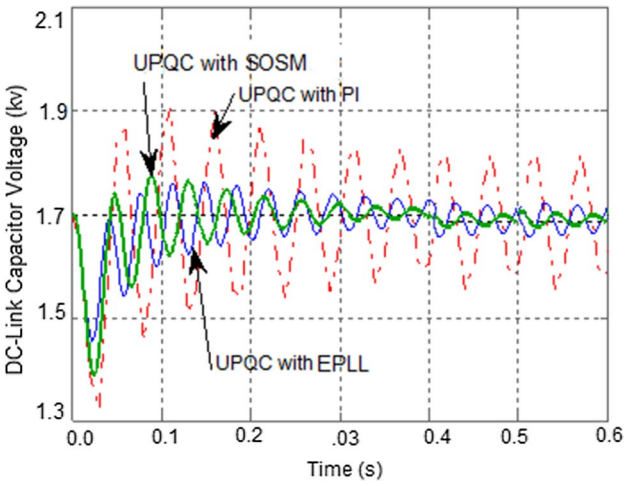

Fig. 6 DC-link Capacitor Voltage for scenario I

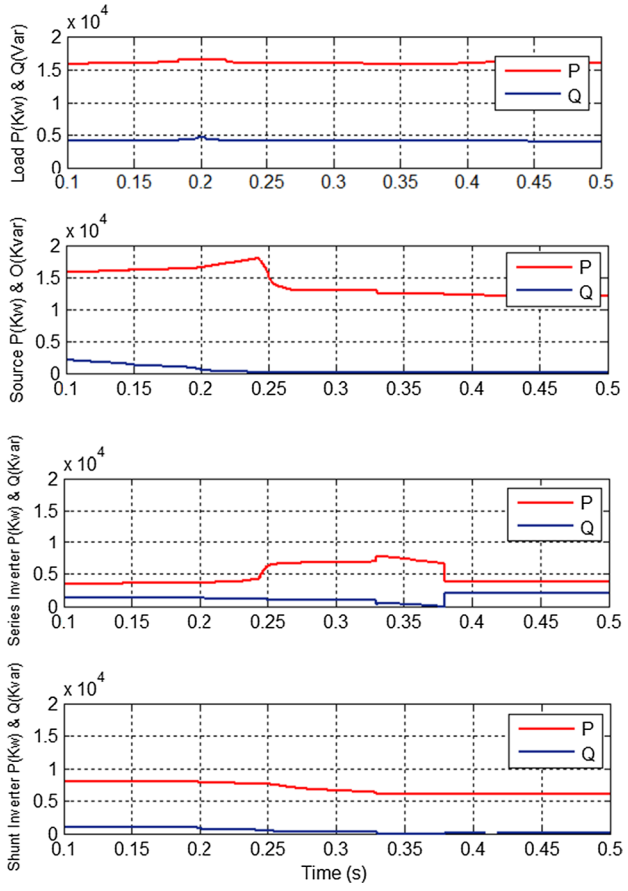

Fig. 7 Load, Source, series and shunt inverter active and reactive power for scenario I

shunt inverters injected active and reactive power is illustrated in Fig. 7.

Scenario II: harmonic elimination and voltage sag compensation of controller with voltage sag under nonlinear loads was investigated in this case. To evaluate single phase and three-phase sag compensation capability of the proposed configuration, a supply disturbance has been simulated and analyzed to decrease the peak voltage value by 30% from 0.2 to 0.4 s. The simulation results for single phase sag have been demonstrated in Figs. 10, 11 and 12. The injected voltage under single-phase sag conditions by the proposed UPQC configuration is displayed in Fig. 10. It can be seen that when the voltage is below its normal value, an effective compensation has been done and the load voltage has risen to its required level. The supply current under the sag condition and the load current with mitigated sag and compensating current are shown in Fig. 11. The DC-link voltage wave-form is revealed in Fig. 12. As can be seen, the DC-link voltage drop due to sag condition has been eliminated and has reached its nominal value.

Simulation results for 3-phase sag have been demonstrated in Figs. 13, 14 and 15. The source, load and injected (in-phase) voltage in the 3-phse sag condition is shown in Fig. 13. Similar to the previous section, the 3-phase voltage sag has been successfully compensated and the load voltage has reached its permissible set point. The DC link voltage wave-form is also demonstrated in Fig. 14. The load, Source, series, and shunt inviter active as well as reactive power are shown in Fig. 15.

5 Experimental Setup

In order to validate the efficiency of proposed control scheme, an experimental setup was conducted in the well-equipped distribution level laboratory of Shiraz Electricity Distribution Company (SHEDC). The setup consisted of a PV simulator module and a set of FARATEL 240v, 42AH battery storage connected to a 3 phase 400v test grid through UPQC inverters (Fig. 16). Key features and specifications of PV simulator are stated in Table 4.

A programmable RISC type micro-controller and 32-bit floating-point digital signal processor of inverters enabled us to reload the provided MATLAB based control program. The component of the inverters' cabinet is shown in Fig. 17. To extract and analyze the parameter values, the FTU-P100 remote control unit (RTU) was applied. FTU-P100 is a load break switch control unit enabling us to measure and

Table 2 Comparison of the PI, EPLL and SOSM Controllers performance

Harmonic order	≤ 5			≤ 9		
Type of controller	PI	EPLL [21]	SOSM	PI	EPLL [21]	SOSM
Load current THD	27.82%	27.82%	27.82%	27.63%	27.63%	27.63%
Source current THD	8.69%	2.73%	1.7945%	8.55%	2.68%	1.7945%

Table 3 Harmonic contents of Load and source currents of Phase-A

Harmonic order	Load current (%)	Source current (%)
1	100	100
2	0.004	0.117
3	0.002	0.299
4	0.005	0.091
5	19.383	0.946
6	0.007	0.282
7	12.531	0.287
8	0.002	0.058
9	0.005	0.103
10	0.004	0.795
11	7.001	1.059
12	0.005	0.088
13	5.273	0.247
14	0.001	0.077
15	0.01	0.225
16	0.003	0.130
17	3.112	0.398
18	0.002	0.149
19	2.366	0.146
20	0.001	0.149
Total harmonic distortion %	25.08	1.7945

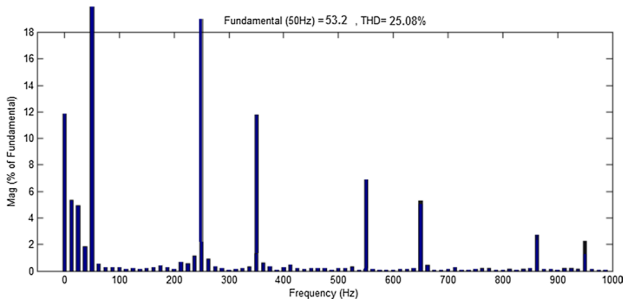

Fig. 8 FFT analysis of load current

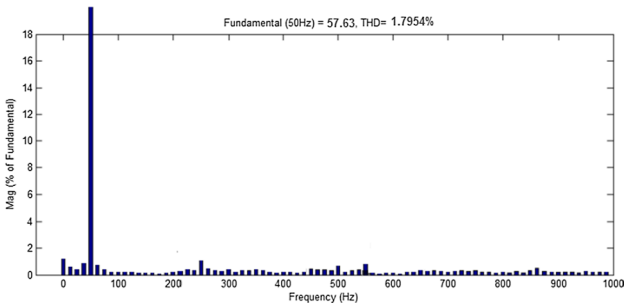

Fig. 9 FFT analysis of source current

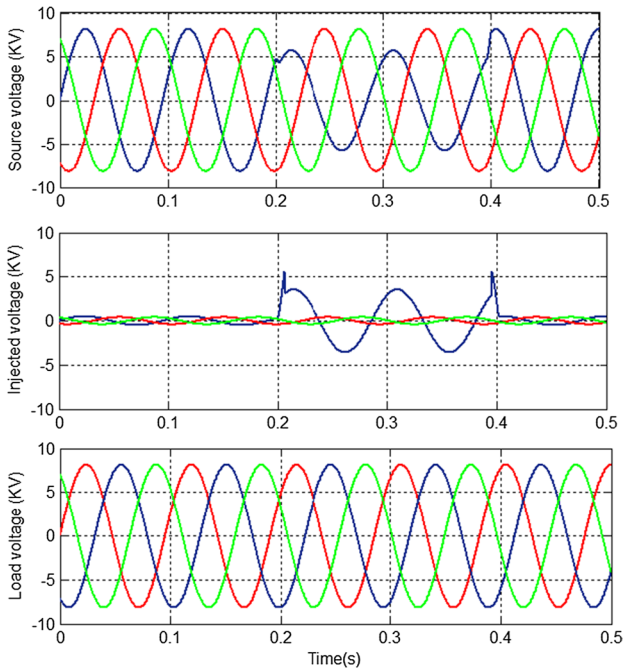

Fig. 10 Load, Source and series converter injected current for scenario II (single phase sag)

manipulate the magnitude and phase angle, true RMS, harmonics and THD of current and voltage, as well as the active and reactive power of each phase or three phases. FTU-p100 is equipped with a dedicated PC or notebook operating software (FTU-set) used to display results, configurations, and

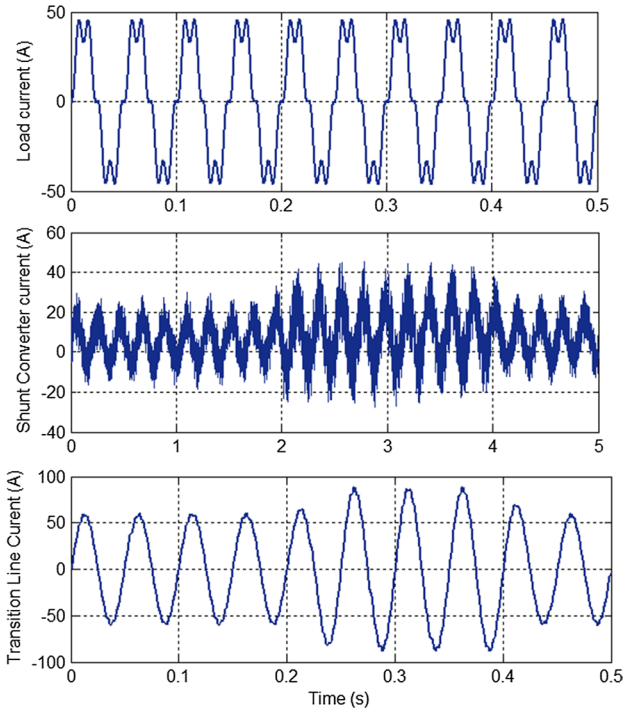

Fig. 11 Load, transmission line and compensation current for scenario II (single phase sag)

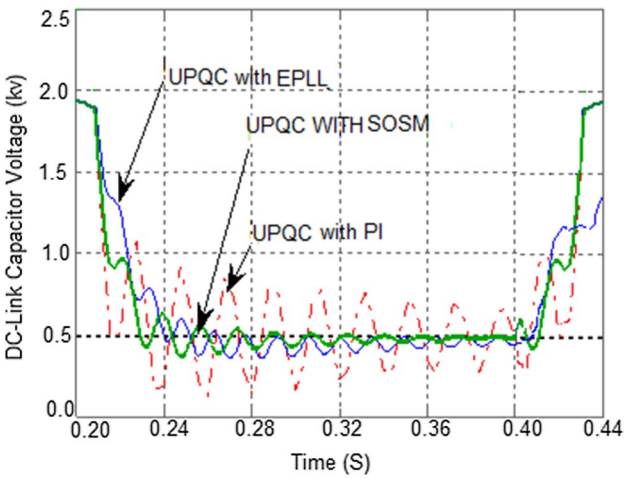

Fig. 12 DC-link capacitor voltage for scenario II (single phase sag)

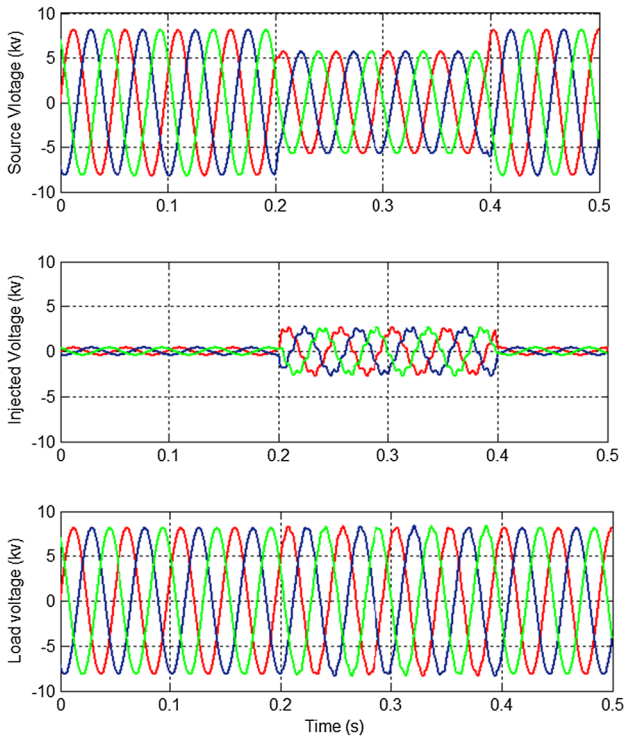

Fig. 13 Source, load and injected (in-phase) voltage for scenario II (3- phase sag)

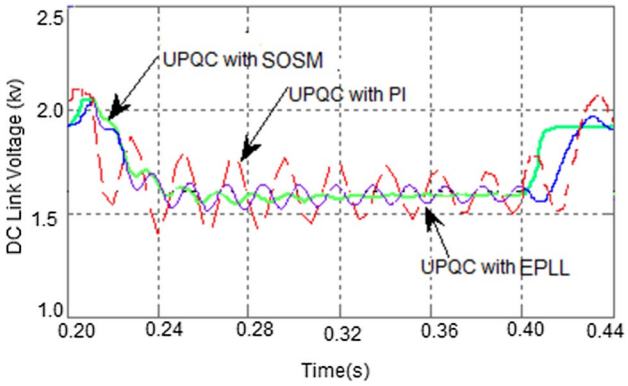

Fig. 14 DC-link capacitor voltage for scenario II (3- phase sag)

fault waveform view. The parameters of the experimental system are stated in Table 5 with the performance of the proposed control method evaluated. In the implemented setup, a nonlinear power electronic based load was connected to the system. As observed in Figs. 18 and 19, the THD of the source current of phase A (because of limited number of CT's in test module only one phase has been analyzed) diminished to 1.02%, while the THD of the load current was measured as 23.87%. Furthermore, a 30% 3-phase voltage sag was established in the voltage source to reveal the function of UPQC. As observed in Figs. 20 and 21 (where x and y axis are respectively time and voltage magnitude), the voltage sag has been compensated effectively.

6 Conclusion

A State Observer Based Sliding Mode (SOSM) control scheme was introduced in this paper to enhance the performance of UPQC in a micro-grid integrated power

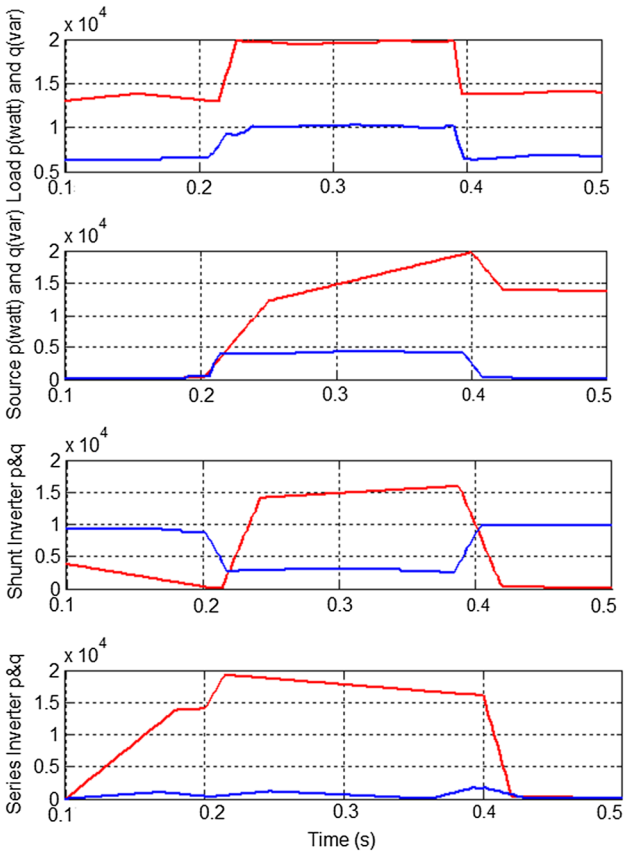

Fig. 15 Load, Source, series and shunt inviter active and reactive power for scenario II (3- phase sag)

Fig. 16 Experimental set up

system. Using the proposed control scheme, the power quality improvement capability of UPQC in the micro-grid improved. THD of the load voltages using the proposed compensation strategy was always kept below the IEEE voltage harmonic limits (IEEE Standard-519, 1992). While the load current in all cases is found to be content of all odd harmonics, providing THD of 25.08%, using proposed

Table 4 Key features and specifications of PV simulator

simulator features	value
Output ratings	
Max. Power	510 W
Voc Max	60 V
Isc Max	0–8.5 A
Programming accuracy at 22 °C ± 5 °C	
Voltage	0.075% + 25 mV
Current	0.2% + 20 mA
Ripple and noise	
Voltage rms, p–p	20 mV rms, 125 mV p–p
Current rms, p–p	2.5 mA rms, 19 mA p–p

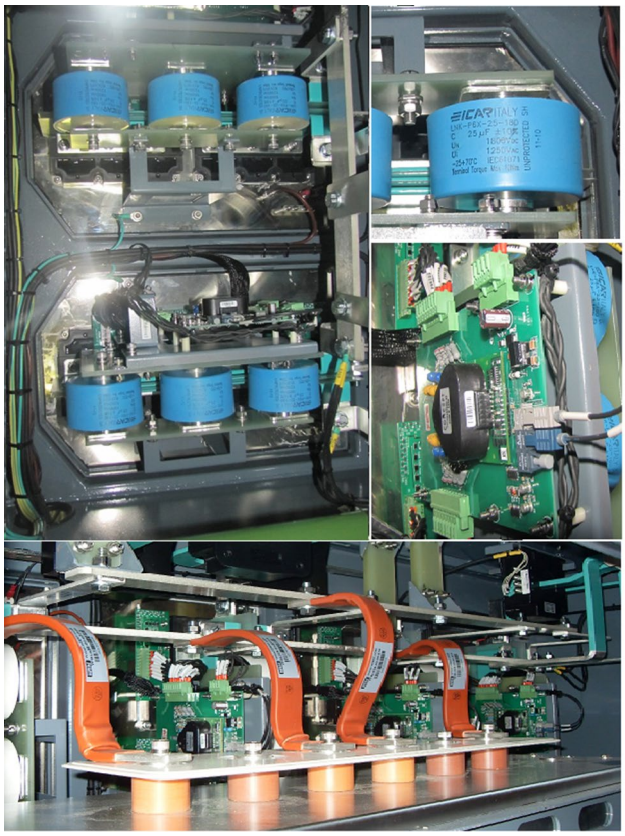

Fig. 17 cabinet boxes

controller THD of source current has been reduced to 1.7945%. Compared with the current traditional and classical UPQC controllers, both single and three phase voltage sags under nonlinear loading were compensated effectively. Results showed that in spite of 30% source voltage sag, load voltage has risen to its required level due to presence of UPQC and designed controller. The simulation results showed the superiority of the method regarding accuracy and tracking speed.

Table 5 Experimental system parameters

Parameter	Value
Source voltage	11 kv
frequency	50 Hz
R load	30 Ω
L load	11.5 mH
Series filter inductance	1.5 mH
Series passive filter resistance	5 Ω
Series passive filter capacitance	25μF
shunt passive filter resistance	5 Ω
shunt passive filter capacitance	4.7 μF
shunt passive filter inductance	3.5 MH
DC-link capacitor	2200 μF

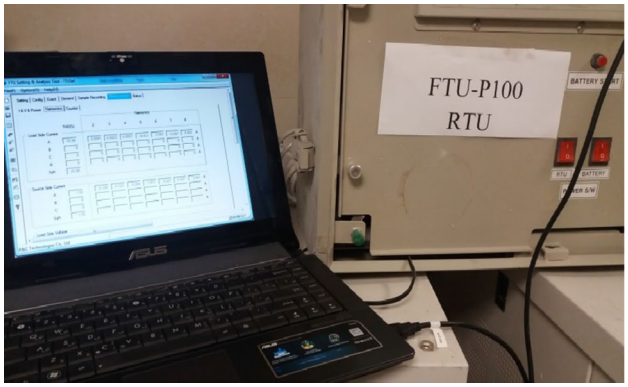

Fig. 18 Load side and source side current harmonic analysis

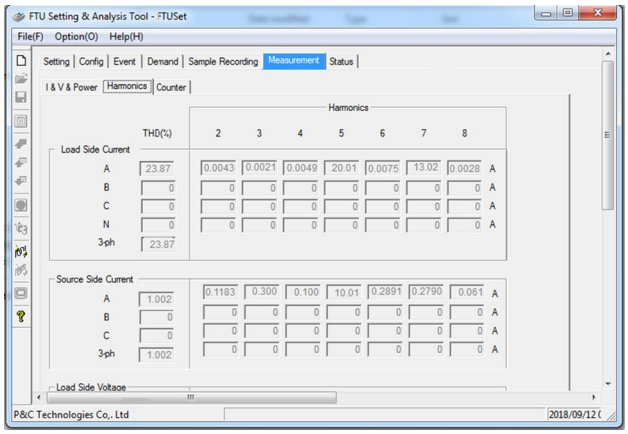

Fig. 19 Load side and source side current harmonic analysis

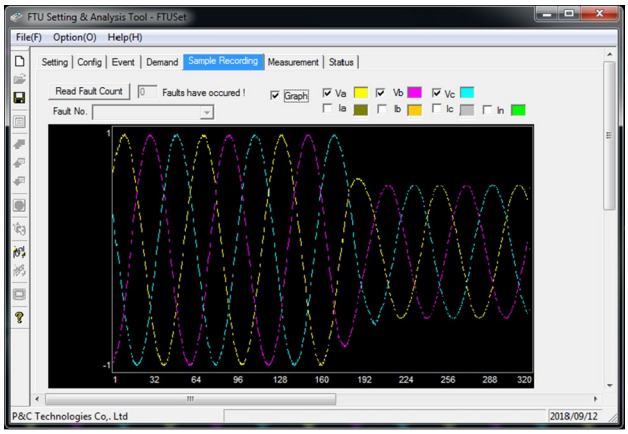

Fig. 20. 3-phase voltage sag in source current

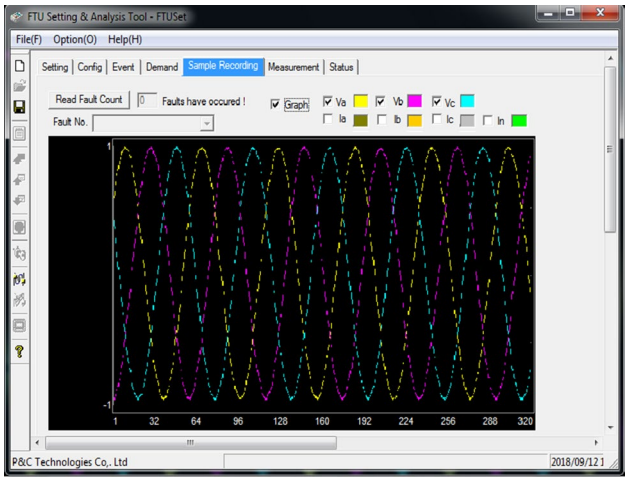

Fig. 21 Compensated source side voltage

References

1. Mohamed FA (2008) Microgrid modeling and online management. PhD dissertation, Dept. of Electronics, Communications and Automation, Helsinki University of Technology, Helsinki, Finland
2. Niknam T, Taheri SI, Aghaei J, Tabatabaei S, Nayeripour M (2011) A modified honey bee mating optimization algorithm for multi objective placement of renewable energy resources. ELSEVIER Appl Energy 88(12):4817–4830
3. Ghosh A, Ledwich G (2002) Power quality enhancement using custom power devices. Power electronics and power systems. Springer, US. https://doi.org/10.1007/978-1-4615-1153-3
4. Bhosale SS, Bhosale YN, Chavan UM, Malvekar SA (2018) Power quality improvement by using UPQC, a review. In: IEEE international conference on control, power, communication and computing technologies, Kannur, India
5. Kesler M, Ozdemir E (2011) Synchronous-reference-frame-based control methods for UPQC under unbalanced and distorted load conditions. IEEE Trans Ind Electron 58(9):3967–3975
6. Khadkikar V (2012) Enhancing electric power quality using UPQC: a comprehensive overview. IEEE Trans Power Electron 27(5):2284–2297

7. Samira D, Haidas M, Othmane A, Chellali B (2007) Optimization of parameters of the unified power quality conditioner using genetic algorithm method. J Inf Technol Control 36(2):242–245
8. Kinhal VG, Agarwal P, Gupta HO (2011) Performance investigation of neural-network-based unified power-quality conditioner. IEEE Trans Power Deliv 26(1):431–437
9. Manivasagam R (2018) Various control strategies for UPQC enhancement to mitigate PQ issues, PhD dissertation, Dept. of Electrical Engineering , Anna Univ., India
10. da Silva SAO et al (2020) Comparative performance analysis involving a three-phase UPQC operating with conventional and dual/inverted power-line conditioning strategies. IEEE Trans Power Electron 35(11):11652–11665
11. Landaeta LM et al (2006) A mixed LQRI/PI based control for three-phase UPQCs. In: 32nd annual IEEE conference on industrial electronics, Paris, France
12. Garces-Gomez YA, Hoyos FE, Candelo-Becerra JE (2019) Classic discrete control technique and 3D-SVPWM applied to a dual unified power quality conditioner. Appl Sci 9(23):5087–5097
13. Do MT (2014) Sliding mode learning control and its applications, Ph.D. dissertation, Faculty of Science, Engineering and Technology, Swinburne University of Technology, Melbourne, Australia
14. Chandrasekaran G, Periyasamy S, Panjappagounder Rajamanickam K (2020) Minimization of test time in system on chip using artificial intelligence-based test scheduling techniques. Neural Comput Appl 32:5303–5312
15. Chakraborty S, Simoes MG (2009) Experimental evaluation of active filtering in a single-phase high-frequency AC microgrid. IEEE Trans Energy Convers 24(3):673–682
16. Khadem SK, Basu M, Conlon MF (2015) Intelligent islanding and seamless reconnection technique for micro-grid with UPQC. IEEE J Emerg Sel Top Power Electron 3(2):483–492
17. Khadem KS (2016) Power quality improvement of distributed generation integrated network with unified power quality conditioner, Ph.D. Dissertation, Dept. Elect. Eng., Dublin Institute of Technology, Dublin, Ireland
18. Ochoa-Giménez M, García-Cerrada A, Zamora-Macho JL (2017) Comprehensive control for unified power quality conditioners. J Mod Power Syst Clean Energy 5(4):609–619
19. Jianxing L, Sergio V, Ligang W, Abraham M, Huijun G, Leopoldo GF (2017) An extended state observer based sliding mode control for three-phase power converters. IEEE Trans Ind Electron 64(1):22–31
20. Zhang Q, Wang C, Su X, Xu DI (2018) Observer-based terminal sliding mode control of non-affine nonlinear systems: finite-time approach. J Frankl Inst 355(16):7985–8004
21. Koroglu T, Bayindir KC, Tumay M (2016) Performance analysis of multi-converter unified power quality conditioner with an EPLL based controller at medium voltage level. Int Trans Electr Energy Syst 26(12):2774–2786

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