Journal of Electrical Engineering & Technology (2021) 16:1445–1455
https://doi.org/10.1007/s42835-021-00680-1

ORIGINAL ARTICLE

A Developed H-Bridge Cascaded Multilevel Inverter with Reduced Switch Count

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Received: 7 October 2020 / Revised: 14 December 2020 / Accepted: 28 January 2021 / Published online: 18 February 2021

Abstract
Multilevel Inverter integrates several Direct Current (DC) sources to produce a single-phase Alternating Current (AC) waveform that can be used to meet the domestic and commercial power demand. This article introduces a novel Multi Source Cascaded Multilevel Inverter with a reduced number of switches for the efficient use of DC voltage sources. The conversion efficiency can be increased by the presented topology which is simple in design to overcome the significant switching losses in the power electronics devices. Optimal Firing Angle and Phase Opposition Disposition Pulse width Modulation Techniques were used to reduce the harmonics at the desired output of the inverter and also to improve the power quality of the presented topology. This article also proposes two Asymmetric Multilevel Inverter Topologies. A comparison has been made, on the number of switches required and the efficiency of the inverters to differentiate the presented Topologies from other topologies of the multilevel inverter. Finally, the performance characteristics of the presented topologies have been designed and investigated using MATLAB Simulation. Simulation results were validated using an experimental setup.

Keywords Modified multilevel inverter · Pulse width modulation (PWM) · Total harmonic distortion (THD) · Optimal firing angle control (OFA) · Power quality

1 Introduction

The energy demand is rising day by day due to the advancement of the industrial sector. To preserve fossil fuels for the future, the scope of energy generation relies heavily on renewable energy sources. The installation of a PV plant in the industry serves non-critical loads, thus reducing tariff stress in the industry [1]. The power extracted from PV is DC that must be converted to AC for further use by integrating it with an inverter. The design of the conventional H-bridge inverter for medium and high load ratings makes the system size larger and more expensive. The Level of THD is also high while combining solar PV with a conventional H-bridge inverter. Multilevel inverters (MLIs) were introduced with different topologies [2] to improve the quality of inverter power. Generally, classified MLI topologies are voltage source inverters (VSI) and current source inverters (CSI) [3]. Some of the notable VSI classified designs are Neutral Point Clamped (NPC), Flying capacitors (FC), and Cascaded H-Bridge (CHB) inverters [4]. The nature of robustness, reliability, and efficiency in the synthesisation of quality output signals makes CHB an appropriate tool for integrating it into the Renewable Energy conversion systems [5]. The CHB can be modeled either in symmetric or asymmetric operating mode. CHB is said to operate in symmetric mode when it has similar DC source as input and produce linear output voltage upon input source voltage. In asymmetric mode, CHB has dissimilar input DC voltage sources and produces either linear or non-linear output depending on the input voltage source [6, 7]. The modified CHB topology is developed to address the problem of non-balancing voltage [8] to reduce the number of switches requirement. An MLI system [9] was designed to operate under symmetrical and asymmetrical operating modes for high voltage applications. MLI structures with the modified H-Bridge Topology were proposed [10, 11] and these topologies use a high number of switching devices. This entire setup is used as a basic unit to generate AC output signals from the DC source. The main objectives of Multilevel Inverters are reducing the number of

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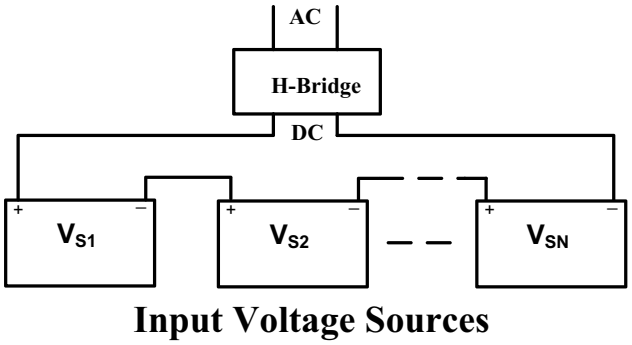

Fig. 1 Schematic drawing of MLI topology

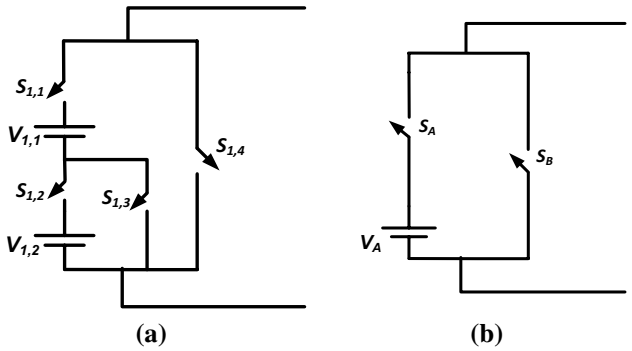

Fig. 2 **a** Basic Module of MSCMLI Topology **b** Level Booster Circuit

switches; Low switching losses; increasing the output voltage levels and reducing the total harmonic distortion. The schematic drawing of generalized MLI with multiple DC sources is presented in Fig. 1.

This article presents a Multi-Source Cascaded Multilevel Inverter (MSCMLI) topology with a reduced number of switches. Without altering the structure and number of switches, the presented topology can be used for both Symmetric Multilevel Inverter (SMI) and Asymmetric Multilevel Inverter (AMI). It consists of 'n' number of basic units that is described by several factors such as the required output voltage, number of levels, Total Harmonic Distortion (THD), number of switches or control drivers, etc. This topology has the advantage of being able to supply the power to load continuously if any of the input sources are in malfunctions.

2 The Recommended Topology

The presented topology has 'n' number of series-connected basic units to supply the required range of output levels. A basic unit consists of two sources V1,1 controlled by a switch S1,1 and V1,2 controlled by a switch S1,2 as shown in Fig. 2a. Both sources are connected with the load if the switch S1,1is turned on and bypassed by the switch S1,3 when the switch $S_{1,1}$ and $S_{1,2}$ are off. Each basic unit will produce an output voltage of ±2VDC when connected to the Load. This circuit employs a level booster module which consists of a voltage source connected with a switch S_A in series as shown in Fig. 2b. A bypass switch S_B is employed to bypass the source to produce zero voltage level in the output.

The general structure of the Multi-Source Cascaded Multilevel Inverter (MSCMLI) topology is given in Fig. 3a which contains 'n' number of basic units and a level booster circuit. Voltage sources used in the first basic unit are $V_{1,1}$ and $V_{1,2}$ while, the voltage sources used in the nth basic unit are represented as $V_{n,1}$ and $V_{n,2}$. The presented topology can be used as a Symmetric Topology if all the input Voltages are equal ($V_{1,1} = V_{1,2} = \ldots. = V_{n,1} = V_{n,2} = V_A = V_{DC}$) and an Asymmetric Topology if the input voltages are unequal. This paper presents a Symmetric topology A_1 and two Asymmetric topologies A_2 and A_3.

The basic parameters of the presented topology are, number of switches S_{switch} and the required number of sources S_{source} is given by (1),

$$S_{SWITCH} = 4_n + 6 \tag{1}$$

The actual requirement of the number of input DC sources is (2),

$$S_{SOURCE} = 2_N + 1 \tag{2}$$

Where n – number of basic units

(1) & (2) are common for the presented symmetric topology A_1 and for the asymmetic topologies A_2 and A_3. The other parameters like the number of output voltage levels (N_{LEVEL}), maximum output voltage (V_{AC}), and total blocking voltage (V_{BLOCK}) are described by the number of basic units 'n' and the number of sources used in the circuit. For the symmetric topology A_1,

$$N_{LEVEL} = 4n + 3 \tag{3}$$

$$V_{AC} = (2n + 1)V_{DC} \tag{4}$$

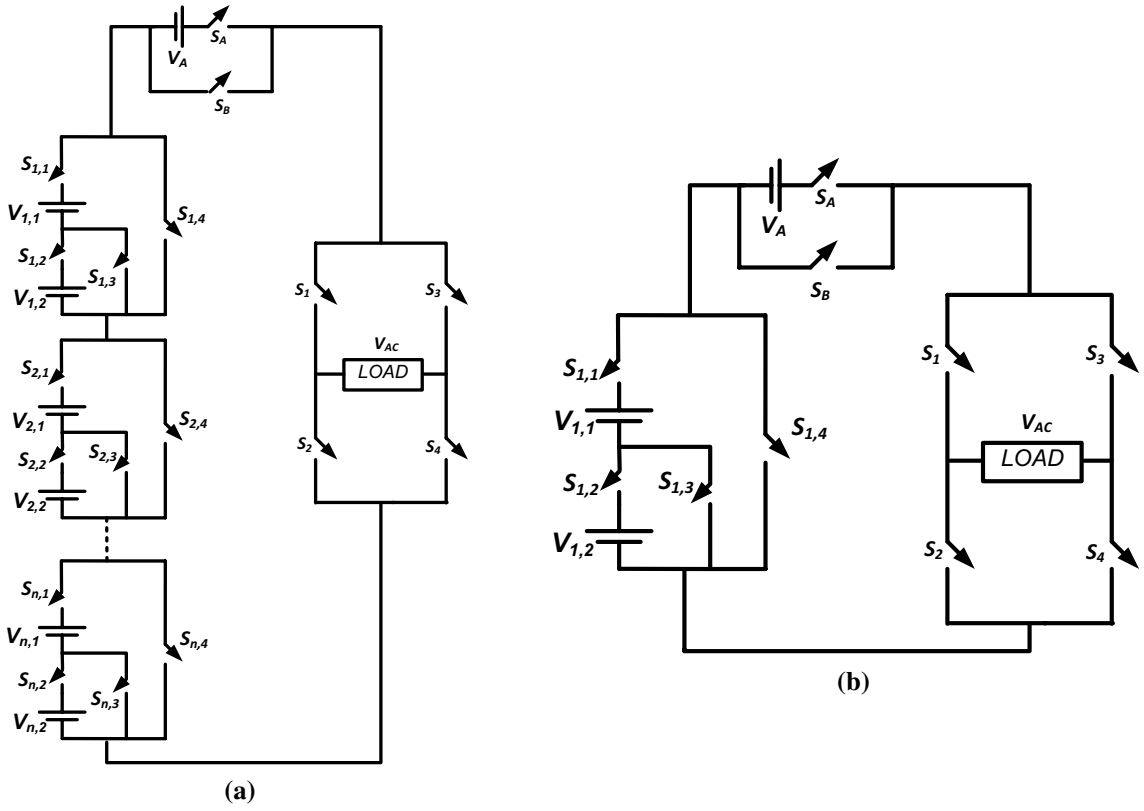

Fig. 3 **a** General structure of Recommended MSCMLI topology with Level Booster Circuit **b** Seven Level circuit

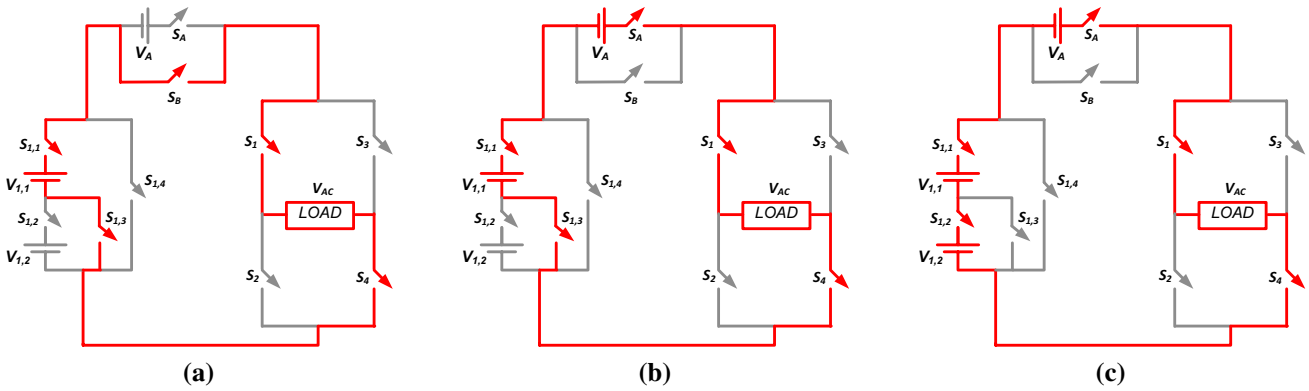

Fig. 4 Operating modes of MSCMLI in Positive Half cycle **a** for output $+V_{1,1}$ **b** for output $+V_{1,1}+ V_A$ **c** for output $+V_{1,1}+ V_{1,2}+ V_A$

Figure 3b shows a seven-level Symmetric MSCMLI topology for n=1 in A_1. It consists of a basic unit and one level booster unit. From (1) and (2), the number of switches and sources of the given topology is described as 10 and 3 respectively. Similarly, (3) and (4) describes that the MSC-MLI topology produces seven levels in the output waveform and the maximum output voltage will be $3V_{DC.}$

Figure 4 shows the three different modes of operation of the presented topology at the positive half cycle of the output voltage. By considering the value of input voltage sources $V_{1,1} = V_{1,2} = V_A = V_{DC}$, this topology can produce an output level of $-3V_{DC}$ to $+3V_{DC}$. Figure 4a shows the operation of A_1 for $+V_{DC}$ output. Only $V_{1,1}$ is connected to the load through $S_{1,1}$ and the other sources are bypassed using $S_{1,3}$ and S_B. $+2V_{DC}$ level is produced by connecting $V_{1,1}$ and V_A through the switch $S_{1,1}$ and S_A while $V_{1,2}$ is not connected as shown in Fig. 4b. Figure 4c shows the operating mode for $+3V_{DC}$ output in which all input sources are connected with the load. During the negative half cycle of output, switches S_2 and S_4 will be turned on for the same modes of operation.

2.1 Harmonic Reduction in MLI

The Selective Harmonic Elimination (SHE) algorithm is implemented, which removes the particular harmonic order by calculating the optimum angles of triggering using mathematical expressions [12]. Literature reviews show that the tailored selective harmonic elimination algorithms can be extracted to reduce THD in multi-level inverters [13–15]. For MLI, different switching angles for each level such as β_1, β_2, β_3, …β_N is desirable for reduction of lower order harmonics and the conditions are as follows,

$$\beta_1 < \beta_2 < \ldots < \beta_{(n-1)} < \beta_N < 90 \tag{5}$$

$$cos(\beta_1) + cos(\beta_2) + cos(\beta_3) + \ldots + cos(\beta_N) = (N_{LEVEL} - 1) * M_a/2 \tag{6}$$

Where,

N_{LEVEL} – Number of output levels.

$$N = \frac{N_{LEVEL} - 1}{2} \tag{7}$$

M_a – modulation index and the equation expressed as

$$M_a = \frac{V_R}{N.V_{DC}} \tag{8}$$

Where, V_R – Reference Voltage

V_{DC} – Input Voltage

The expression to evaluate the lower order harmonics is given by the equation (9),Where,

$$V_h(t) = \sum_{h=3,5,7,\ldots} \frac{4V_{in}}{n\pi}\left[\cos\left(h\beta_1\right) + \cos\left(h\beta_2\right) + \cos\left(h\beta_3\right) + \ldots. + \cos\left(h\beta_N\right)\right] \tag{9}$$

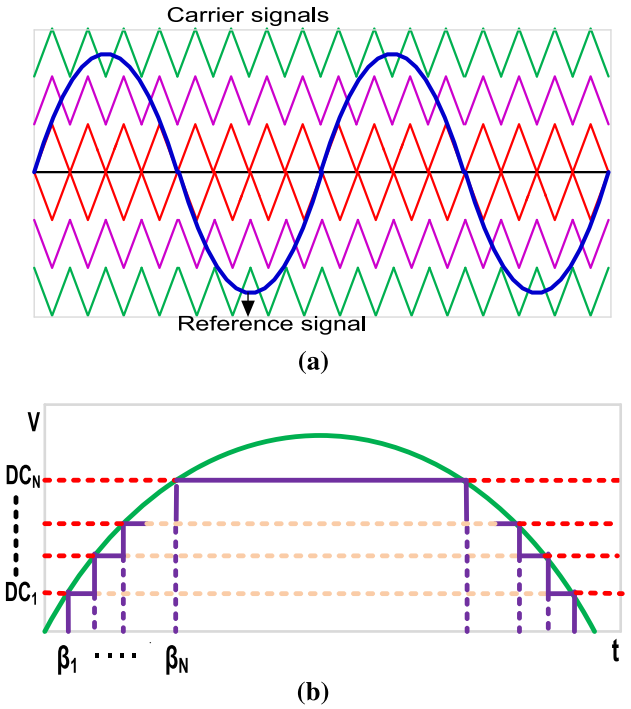

Fig. 5 Generation of gate pulse for the MSCMLI using the comparison of carrier and reference sinusoidal signal in **a** OFA **b** POD

h – Order of the harmonics.

Normally, calculations required for the firing angles are the sum of individual harmonic with all firing angles are considered as zero. For an N_{LEVEL} output voltage, N-1 individual harmonic values can be eliminated using (10). So for the seven-level Symmetric MSCMLI, any two individual harmonic orders can be eliminated.

$$\sum_{h=3,5,7,\ldots} \frac{4V_{in}}{n\pi}\left[\cos\left(h\beta_1\right) + \cos\left(h\beta_2\right) + \cos\left(h\beta_3\right) + \ldots. + \cos\left(h\beta_N\right)\right] = 0 \tag{10}$$

2.2 Control Strategy

Reduction in THD and lowered switching losses improve the quality of output voltage significantly. To achieve a distortion-less output voltage, a higher rate of switching control strategy is essential. Hence, the recommended topology use Phase Opposition Disposition (POD) has to reduce the power loss in the inverter circuit and reduce the

THD. In this method, 'N' values of triangular waveforms with equal phase-amplitude are compared with a sinusoidal reference waveform of fundamental frequency or grid frequency. Using(5), the seven-level MSCMLI topology, three triangular waveforms are compared with the reference waveforms as shown in Fig. 5a and we get three pulses with firing angles β_1, β_2, and β_3. In addition to that, the Optimal Firing Angle Control (OFA) strategy is also used to compare the performance of the presented MLI schemes. OFA strategy works on fundamental frequency and generates the triggering gate signals for semiconductor switching devices. This method generates the gating signals by taking the reference signal as pure sine waveform with fundamental frequency or grid frequency and compared with the required DC voltage levels as shown in Fig. 5b. The advantage of using the OFA strategy is that it avoids synchronizing problems when used in grid-connected systems. The determined gating signals with required firing angles achieved from OFA and POD schemes are used for the MSCMLI system to obtain the required stepped output voltage waveform with the reduced THD. From (5) to (10), for the proposed 7-level symmetric MLI, the 7th and 11th order harmonics are mitigated by calculating suitable firing angles β1, β2, and β3.

The reference DC voltage for the respective firing angle is calculated in OFA based on the following expression,

$$DC_i = M_a V_R sin(\beta_i) \tag{11}$$

Where, i = 1, 2,….N,M_a – modulation index, and β – Required firing angle, $N = \frac{N_{LEVEL}-1}{2}$, V_R – Maximum value of sine reference voltage

From (11), it is described that three DC voltage levels are required to compare with a sine wave to produce the firing angles β_1, β_2, and β_3 using the OFA method.

2.3 Efficiency Calculation

The efficiency of the MSCMLI is calculated to compare its performance with other topologies of MLI. The efficiency of MLI is determined by accounting for the conduction loss and the switching loss in the power electronic devices. The total losses (P_T) of the inverter circuit in a cycle is given by [16],

$$P_T = \sum_{n=1}^{N_{IGBT}} P_{c,IGBTn} + P_{SW,Tn} + \sum_{n=1}^{N_{DIODE}} P_{c,Dn} + P_{SW,Dn} \tag{12}$$

Where, $P_{c,IGBT}$ – conduction loss of IGBT
$P_{SW,T}$ – switching loss of IGBT
$P_{c,D}$ – conduction loss of Diode
$P_{SW,T}$ – switching loss of Diode

It is inferred from the above expression that the losses continue to increase on increasing the power electronic devices in the system. The efficiency of the inverter circuit is determined by (13) after including the conduction and switching losses.

$$\eta = \frac{P_L}{P_L + P_T} \times 100 \tag{13}$$

Where output power, $P_L = \frac{V_{rms}^2}{R}$ and the V_{rms} denotes the output rms voltage of the inverter. Hence, the reduction in switches in the inverter reduces the switching losses associated with it and increases the efficiency of the inverter. Taking the prescribed values of the parameters, the theoretical efficiency of the inverter is 98.6%, with a maximum output voltage of 300V.

Table 1 Multi-source Cascaded Multilevel Inverter (MSCMLI) Algorithm with Related Parameters

Proposed algorithms	Amplitude of DC voltage sources	N_{LEVEL}	V_{AC}	V_{BLOCK}
Symmetric, A_1	$V_A = V_{1,j} = V_{2,j} = V_{n,j} = V_{DC}$ $j = 1,2$	$4n+3$	$\pm (2n+1)\, V_{DC}$	$(8n+3)V_{DC}$
Asymmetric, A_2	$V_A = V_{DC}$ $V_{1,j} = V_{2,j} = V_{3,j} = V_{n,j} = V_{DC}$ $For\ j = 1$ $V_{1,j} = V_{2,j} = V_{3,j} = V_{n,j} = 2.V_{DC}$ $for\ j = 2$	$6n+3$	$\pm (3n+1)\, V_{DC}$	$(13n+3)V_{DC}$
Asymmetric, A_3	$V_A = V_{DC}$ $V_{1,j} = V_{2,j} = V_{3,j} = V_{n,j} = (n+1)\, V_{DC}$ $For\ j = 1,2$	$11+4\sum_{K=2}^{N}(k+1)$	$\pm (5+2\sum_{K=2}^{N}(k+1))$	$(6n^2+8n+5)V_{DC}$

Table 2 Switching sequence for A_2 and A_3 asymmetric algorithms with one basic module (n=1)

Algorithm A_2							*Algorithm A_3*					
V_{AC}	$S_{1,1}$	$S_{1,2}$	$S_{1,3}$	S_A	S_B	*H-Bridge*	$S_{1,1}$	$S_{1,2}$	$S_{1,3}$	S_A	S_B	V_{AC}
0			*on*		*on*	S_1&S_4 ON			*on*		*on*	*0*
$V_{1,1} = +V_{DC}$		*on*			*on*				*on*	*on*		$V_A = +V_{DC}$
$V_{1,1} + V_A = +2V_{DC}$		*on*		*on*				*on*			*on*	$V_{1,1} = +2V_{DC}$
$V_{1,1} + V_{1,2} = +3V_{DC}$	*on*				*on*			*on*		*on*		$V_{1,1} + V_A = +3V_{DC}$
$V_{1,1} + V_{1,2} + V_A = +4V_{DC}$	*on*			*on*			*on*				*on*	$V_{1,1} + V_{1,2} = +4V_{DC}$
							on			*on*		$V_{1,1} + V_{1,2} + V_A = +5V_{DC}$
0			*on*		*on*	S_2&S_3 ON			*on*		*on*	*0*
$-V_{1,1} = -V_{DC}$		*on*			*on*				*on*	*on*		$-V_A = -V_{DC}$
$-(V_{1,1} + V_A) = -2V_{DC}$		*on*		*on*				*on*			*on*	$-V_{1,1} = = -2V_{DC}$
$-(V_{1,1} + V_{1,2}) = -3V_{DC}$	*on*				*on*			*on*		*on*		$-(V_{1,1} + V_A) = -3V_{DC}$
$-(V_{1,1} + V_{1,2} + V_A) = -4V_{DC}$	*on*			*on*			*on*				*on*	$-(V_{1,1} + V_{1,2}) = -4V_{DC}$
							on			*on*		$-(V_{1,1} + V_{1,2} + V_A) = -5V_{DC}$

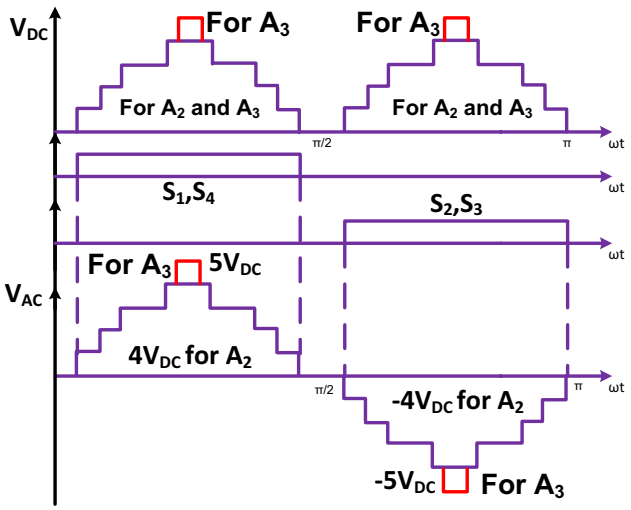

Fig. 6 output waveform of Asymmetric Topologies A_2 and A_3 for n=1

3 Asymmetric Topologies

This paper presents Two Asymmetric Topologies A_2 and A_3 based on the structure shown in Fig. 3a, in which the input voltage sources have unequal magnitudes. Table 1 shows the basic parameters like the output voltage Levels (N_{LEVEL}), the maximum value of output voltage (V_{AC}), and total blocking voltage (V_{BLOCK}) of the presented algorithms based on the number of basic units 'n'.

For n=1 in all presented algorithms, the basic parameters of Asymmetric Topology A_2 will be

$N_{LEVEL} = 6(1)+3 = 9$ and $V_{AC} = [3(1)+1]V_{DC} = 4V_{DC}$

and the basic parameters of Asymmetric Topology A_3 will be $N_{LEVEL} = 11$ and $V_{AC} = 5V_{DC}$

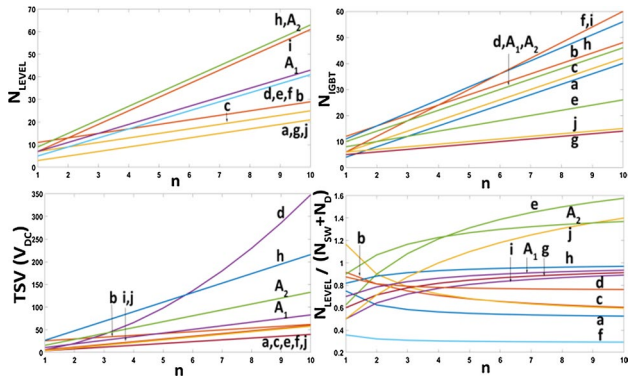

Fig. 7 Comparison of A1 and A2 with contemporary MLI topologies

Table 2 gives the switching sequence for a 9-level inverter derived from asymmetric mode A_2 and for an 11-level inverter derived from asymmetric mode A_3 as per Table 1. Eventhough the number of basic modules required is the same for A_2 and A_3, the number of output voltage levels is higher for A_3. Figure 6 shows the output voltage waveforms of Asymmetric Topologies A_2 and A_3. It shows that A_3 has two more levels than A_2 which has nine levels for the single basic module used.

4 Comparison with other Topologies

In the recommended topologies, the number of switches and diodes count is less when compared with other topologies of MLI as discussed in the literature as shown in Table-3. The graph is plotted between the number of DC sources versus the number of switches required and the number of levels versus the number of switches. The recommended topology is compared with the other topologies

such as DCMLI, FCMLI and CHB MLI [4], modified MLI-b [17] modified MLI-c [18], modified MLI-d [19], modified MLI-e [11], modified MLI-f [20], modified MLI-g [21], modified MLI-h [22], modified MLI-i [23] and modified MLI-j [24]. Since the number of switches and the number of sources is equal in all suggested algorithms, only two algorithms A_1 and A_2 are considered for comparison shown in Fig. 7. The MLI-d and f structures use bi-directional switches so that a single bi-directional switch is considered to be two unidirectional switches. MLI- g and i use diodes in the structure to produce multiple levels in the output regardless of having a good level to source ratio and a single source.

Table 3 Comparison of Device count for symmetrical and Asymmetrical configurations

Topologies	N_{LEVEL}	$N_{SOURCES}$	N_{IGBT}	N_{DRIVER}	N_D
CHBMLI	*2n+1*	*n*	*4n*	*4n*	-
b	*2n+9*	*n+4*	*4n+8*	*4n+8*	-
c	*8n+5*	*n*	*4n+2*	*4n+2*	-
d	*8n+1*	*3n*	*4n+6*	*2n+6*	-
e	*2n+1*	*n*	*n+6*	*n+6*	-
f	*4n+1*	*2n*	*6n*	*6n*	*8n*
g	*2n+1*	*n*	*n+4*	*n+4*	*n-1*
h	*6n+3*	*3n+1*	*5n+6*	*5n+6*	-
i	*6n+1*	*n*	*6n*	*6n*	*2n*
j	*2n+1*	*n*	*n+5*	*n+5*	-
A_1	***4n+3***	***2n+1***	***4n+6***	***4n+6***	**-**
A_2	***6n+3***	***2n+1***	***4n+6***	***4n+6***	**-**

Bold values indicate the proposed topologies of authors

The comparison shows that the number of switches required for a given number of DC sources is lower for the recommended topology when the number of sources is four or more. Figure 7 shows the number of levels for the given number of switches for the recommended topology with the topologies suggested in various articles. As mentioned earlier, the number of levels in symmetrical topology A_1 is higher than other topologies mentioned in the literature. The number of output levels is almost doubles in A_1concerning other topologies. As A_2 is concerned, it has the same number of switches as A_1 and the output level is higher since it has asymmetric input sources. Another asymmetric algorithm A_3 is not considered for comparison because it is also having an asymmetric structure and it gives a very high number of output levels for the given number of switches which is practically difficult to achieve. Apart from the conventional comparisons, the MSCMLI inverter has equal load sharing and bypassing capabilities when any one of the inputs malfunctions. The other topologies that have these capabilities are CHB and MLI-e. In the view of the number of switches, drivers, levels, and blocking voltage concerned, the presented topology is a good alternative for the conventional MLIs and the other topologies presented in the works of literature compared. Table 3 gives a comparative analysis of the different topologies for Number of Levels (N_{LEVEL}), Number of Sources ($N_{SOURCES}$), and number of switches (N_{IGBT}), Number of Drivers (N_{DRIVER}), and Number of Diodes (N_{DIODE}) with respect to number of basic units (n)

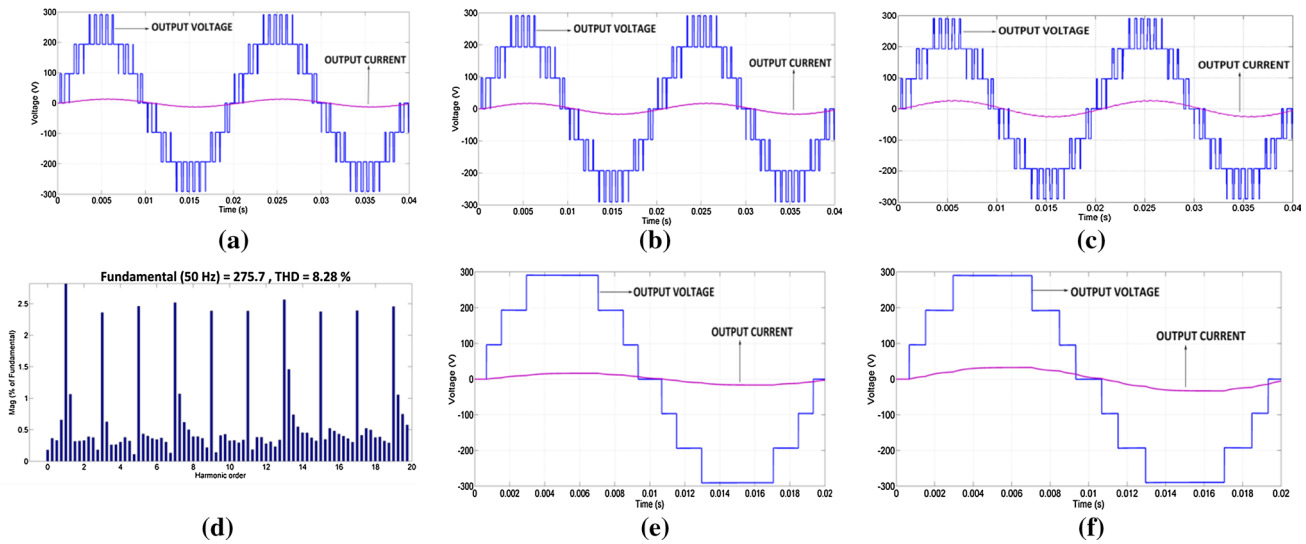

Fig. 8 **a-c** Output voltage and current waveforms of A_1 with POD PWM for various load conditions **d** THD spectrum of the Symmetric topology A_1 **e-f** Output voltage and current waveforms with OFA PWM for various load conditions

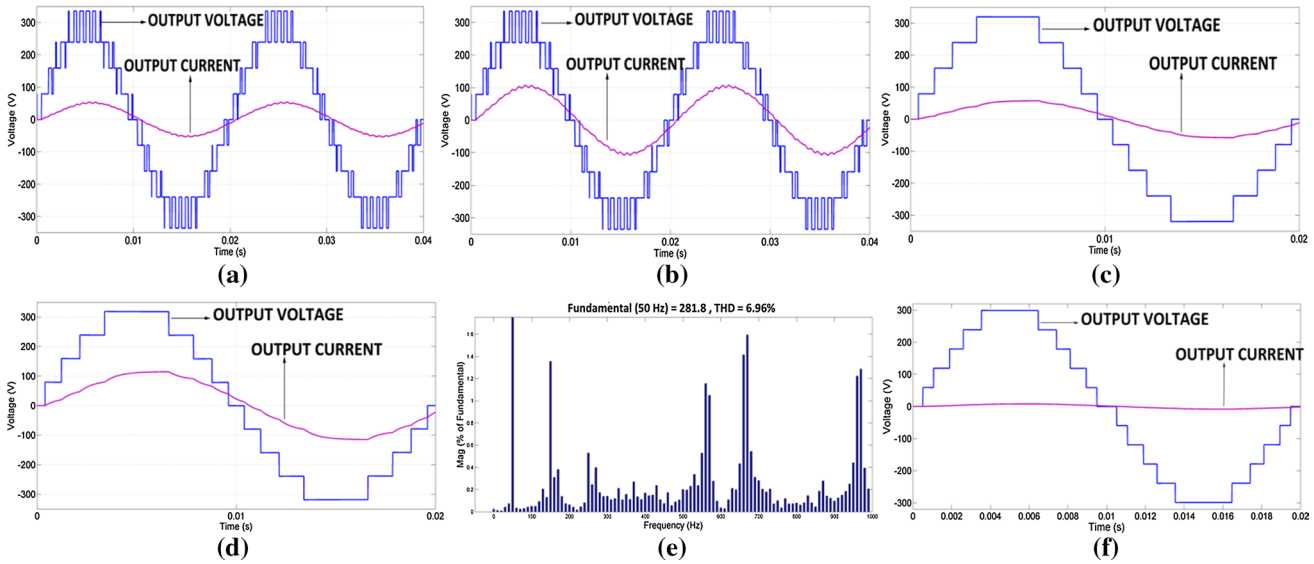

Fig. 9 output voltage and current waveforms of AMI-A_2 (**a**, **b**) with POD-PWM at 100% and 50% Load conditions (**c**, **d**) with NVL-PWM at 100% and 50% Load conditions (**e**) THD spectrum of A_2 (f) output voltage and current of A_3

Table 4 Fundamental Voltage and %THD values of SMI topology for various PWM methods

M_a	POD PWM		OFA PWM	
	V	%THD	V	%THD
1	292.1	10.39	292.1	10.49
0.9	275.7	8.28	275.5	9.01
0.8	243.2	9.67	243.0	10.12
0.7	223.3	10.36	223.1	10.96
0.6	191.2	12.02	191.0	12.74

5 Results and Discussion

The simulation circuit with hardware setup of the recommended 7-Level symmetric topology and 9-level asymmetric topology are developed and results are discussed in this section.

5.1 Simulation Results and Discussion

The simulation model of the recommended 7-level SMI circuit is modeled using MATLAB using the input sources voltage V_{DC} = 100V in each section and the R-L loads R=200 Ω and L=35mH. POD PWM and OFA PWM technique were adopted to generate gate signals and to produce a 7-level waveform at the output. The OFA scheme uses the standard or load frequency to minimize the output frequency deviation, while the POD has a higher carrier frequency suitable for minimization of THD. The output voltage and current waveforms of the recommended 7-level SMI with POD-PWM technology subject to different load conditions are shown in Fig. 8a-c with a THD value of 8.28% as shown

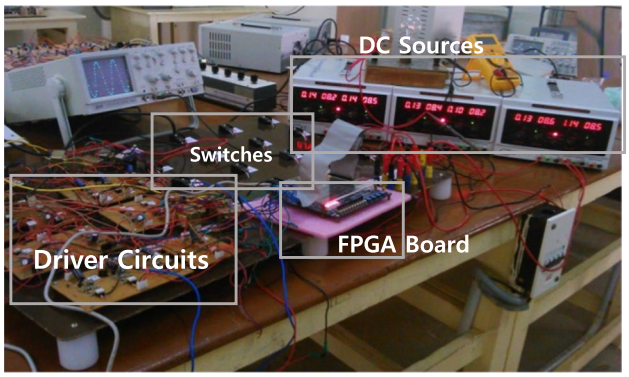

Fig. 10 Hardware prototype of the MSCMLI topology

in Fig. 8d. It is clearly described from the waveforms shown that the switching transients have been reduced in output and the current waveform is smooth. To improve visibility, the current waveform is amplified. Figure 8e-f show the waveform of the output voltage and current under various load conditions using the OFA technique. Figure 8e portrays load voltage and load current values under maximum load condition and Fig. 8f displays the load voltage and load current values under the half load condition of the system proposed. Besides, the magnitude of the voltage is the same as the 300 V peak value at each degree of load conditions. From both examples, the load current is sinusoidal like waveform. This indicates that the suggested method has reduced distortion and that the harmonics are not present in the output waveforms.

Figure 9 depicts the output of algorithm A_2 with one basic module and a level booster. Figure 9a and b portray

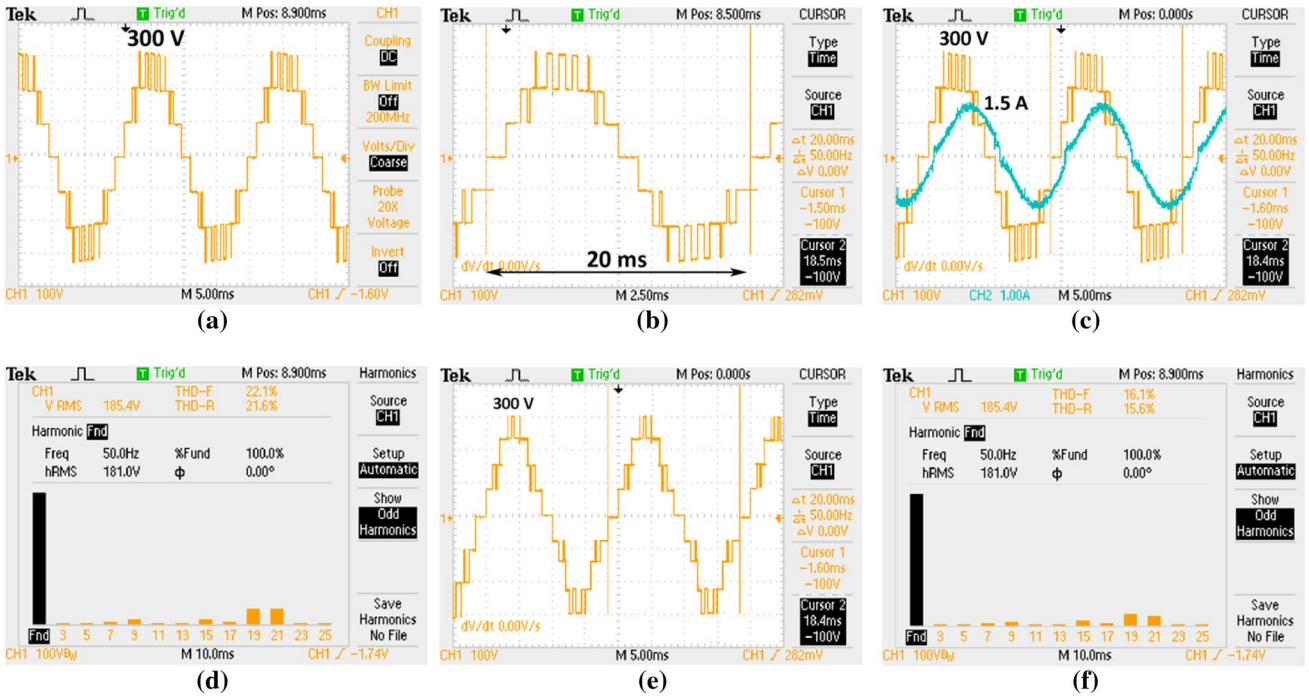

Fig 11 **a-c** Output voltage and current waveforms for the symmetric topology A_1 with POD-PWM **d** THD spectrum of A_1 **e** output voltage of the asymmetric topology A_2 **f** THD spectrum of A_2

load voltage and load current values under maximum load and half load conditions respectively with the POD-PWM scheme. Figure 9c and d show the output of Asymmetric MLI structure A_2 full load and half load conditions respectively for NVL-PWM method employed for same operating conditions. Figure 9e depicts the voltage harmonic spectrum of asymmetric topology A_2 at full load condition. The THD value of A_2 is 6.96% in comparison with the THD value of 8.28 % for A_1. Figure 9f shows the output voltage and current waveform for A_3 algorithm with the output voltage of 11 levels.

Table 4 represents a comparison between the fundamental voltage THD value with the presented PWM strategies like, (a) Phase Opposition Disposition (POD) technique & (b) Optimal Firing Angle Control (OFA) technique against several modulation indices. From this table, it is clear that the suggested POD method is having a better THD value in comparison with other methods and it is proven that the proposed method is minimizing the harmonics present in the output voltage with a reduced number of switches. This guaranteed the effectiveness of the recommended method. The minimum value of Total Harmonic Distortion (THD) is 8.28 as described earlier is taken at a modulation index of 0.9 by using the POD-PWM method.

5.2 Hardware Results and Discussion

To validate the results of the MATLAB simulation, the experimental hardware setup is developed and the trigger gate pulses are generated using the FPGA SPARTAN kit as shown in Fig. 10. Among other microcontrollers, FPGA is chosen for its ability to troubleshoot loops and parallelism. FPGA produces gating pulses using VHDL code with the help of software called ALTERA QUARTUS-II Version 7.2. The experiment was performed with each $V_{DC} = 100V$ with R-L load condition. The output voltage of the recommended 7-level SMI is shown in Fig. 11a which has an amplitude of 300V. From Fig. 11b, the output voltage has a period of 20ms

Table 5 Comparison of simulation and hardware parameters

Parameters	Simulation		Hardware	
	A_1	A_2	A_1	A_2
Number of sources	3	3	3	3
Input voltage(s)	100 V	75V, 150V	100 V	75V, 150V
Number of levels	7	9	7	9
Number of switches	10	10	10	10
Maximum output voltage	300 V	300 V	300 V	300 V
THD %	8.28	6.96	22.1	16.1
Switches	IGBT	IGBT	IRF840	IRF840
Tool	Simulink		FPGA	

for a single cycle hence the output frequency is equal to the power frequency 50Hz. The current waveform of the recommended 7-level SMI is shown in Figure 11c, which has an amplitude of 1.5A current for a load of 200Ω and 35mH. This waveform has less distortion and near sinusoidal. Harmonic analysis of recommended SMI is shown in Fig. 11d. The THD value of output voltage is 22% for an RMS value of 184.4V. The output voltage has higher THD levels as compared with simulation results; it is because of the practical conditions.

Figure 11e indicates the output voltage waveform of the Asymmetric MSCMLI topology A_2, which follows the sinusoidal reference waveform of the reference voltage of the POD-PWM technique and thus reduces the filtering requirements at the output stage. Finally, Fig. 11f shows the THD value of A_2that is 16% forthe output voltage of 300V at full load. The harmonic analysis shows the 19^{th} and 21^{st} order harmonics are more dominant and can be eliminated using filters.Losses were calculated for the inverter designed with the following parameters [17] $V_T = 2.5V$, $V_D = 1.5V$, $R_T = 0.85$, $R_D = 0.15$, $\lambda = 1$, $t_{on} = t_{off} = 2ms$. Practically, with a loss of 16W on the circuit, the overall efficiency of the system is 96.4% for an input voltage and a current of 300 V and 1.5 A respectively. From the waveforms, it is clearly stated that the THD values have been reduced by increasing the number of levels in the circuit. The output current is also nearly sinusoidal waveform with fewer distortions.

5.3 Comparisons of Simulation and Hardware Results

The simulation and hardware results were analyzed and compared for the same load conditions. From the Table 5, one can understand that the Simulation and hardware parameters of the symmetric topology A_1 and asymmetric topology A_2 are same. The maximum obtained output voltage is also equal but the hardware THD % only higher than the simulation result. This THD can be reduced by designing passive filter for the given circuit. This extension work will be carried out as a future scope.

6 Conclusion

This article presented a seven-level Symmetric Multi-Source Cascaded Multilevel Inverter (MSCMLI) topology with a reduced number of switches. The simulation results of the presented topologies under various load conditions were executed and the results were drawn up. The hardware setup was implemented to verify the output of the simulation and the results were analyzed. The absence of bidirectional switches is the primary advantage of the MSCMLI topology that reduces the overall switch count, driver requirement and switching losses in the inverter circuit. Moreover, the symmetric MSCMLI was compared to the other topologies presented in the literature. Eventhough the number of sources is equal in all SMI topologies, the simplicity and of the presented topology reduces the complexity of the control algorithms during the implementation of the hardware prototype. In addition to that, the MSCMLI would have the bypassing capacity to supply the load if there is a problem with any of the switches in the level circuit. This article also presented a nine level and eleven level asymmetric topologies that increase the number of levels without increasing the number of basic units.Simulation and hardware outputs were presented and analysed for the AMI topology.THD values were also compared for the simulation and harware findings. Performance of the presented topologies have been verified with two different PWM techniques and the POD-PWM produced the lesser THD value.The MSCMLI topology can be used in renewable energy integration applications where there are discrete DC sources with fewer electronic switches.

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