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ORIGINAL ARTICLE

Design and Implementation of New Topology for Solar PV Based Transformerless Forward Microinverter

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Abstract
Recently, transformerless inverters play a vital role for single phase low voltage solar photovoltaic (PV) system due to low cost, lesser weight, small size and high efficiency. However, the leakage current produces electromagnetic interferences, current distortion on the grid with additional losses which affects the performance of the inverter. In this paper, a new inverter topology, to deal with the problem of leakage current is proposed. The various conventional H6 topologies are simulated, compared and evaluated based on the leakage current, performance and safety with the proposed inverter topology. This work focuses on transformerless inverter which is best suitable for module integrated converter (MIC) or microinverter. The proposed topology is employed with unipolar sinusoidal pulse width modulation, and it can reduce the common mode (CM) current. The performance analysis is carried out on different topologies using MATLAB/Simulink environment and the proposed inverter experimentally verified on a 150 W prototype. Based on the analysis, simulation and experimental results, the comparison also presented for future reference.

Keywords CM current · Ground leakage current · MIC · Safety · Solar PV · Unipolar switching

1 Introduction

The solar photovoltaic (PV) energy source became a significant and crucial renewable energy in the energy market around the globe, and it is proliferating. This growth is due to constant improvement regarding efficiency, power, reliability etc. Currently, microinverter is a developing solar inverter technology which enhances the efficiency and higher power output. Inversion process of the microinverters is up to the panel level which increases efficiency and custom-made power generation of the PV array. This diminishes the adverse effect of solar PV module mismatch and improves the overall efficiency of the solar energy system. It also enables, module level parameter monitoring, more comfortable and quick installation, design flexibility and safety than conventional inverters. However, high installation and maintenance cost are the main factors impacting the global microinverter market growth, and the other impacting factors are shown in Fig. 1. In the field of microinverter, technological advancements to increase the performance and rapid rise in government funding for renewable energy projects will provide more significant opportunities in the market growth.

The single-phase microinverters dominated than the three-phase due to its application in the domestics. Due to the high energy conversion and flexibility, grid-connected microinverter dominates the global market [1, 2].

The solar PV grid-tied inverters with the transformer are operated at grid frequency which is bulk in size, high cost, less durability and produce more losses. The transformers with low frequency (LF) limits the control of the grid current of the inverter and especially at low load. It will not inject reactive power into the grid due to the transformer magnetization, and it offers poor power factor. The LF transformer might deliver the loss of 2% of the total power loss. The advantage of the transformer with high frequency (HF) is the reduction of size and weight, and it provides the galvanic isolation. The overall efficiency of the system is slightly higher than LF transformer-based inverter with more conversion stage [3, 4].

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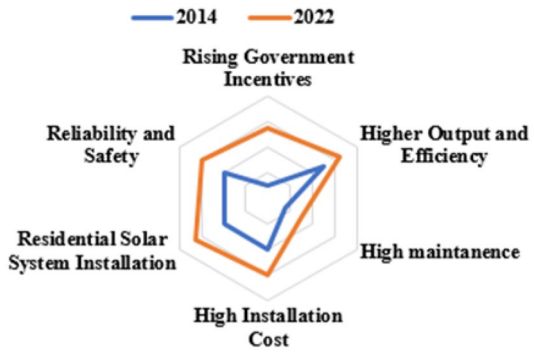

Fig. 1 Factors impacting the microinverter growth

The next generation of the grid-tied inverter is transformerless solar PV based inverter, and it offers higher reliability, efficiency, cost but the non-isolated inverter is having common mode voltage or leakage current issues between the PV and the grid. The stray capacitance formed due to the non-isolated connection which will develop the fluctuations in common mode voltage, and it introduces the ground leakage current, grid current ripple and electromagnetic interferences (EMI). According to German standard DIN-VDE 0126-1-1, disconnection of PV inverter is necessary within 0.3 s if the leakage current exceeds 30 mA (refer Table 1) [5–8].

To address the leakage current issue, this paper proposes a new H6 transformerless inverter topology with bypass circuit connected between A and B points of the inverter which provides freewheeling path when the bridge semiconductor devices are switched off and separates the solar PV module from the grid during the freewheeling period. The organisation of this paper as follows: Sect. 2 discusses the operation and analysis of the existing inverters. Section 3 explains the proposed inverter operation and its control strategies. The simulation results and hardware results are presented in Sects. 4 and 5 respectively. Section 6 concludes the paper.

Table 1 Leakage current value as per DIN VDE 0126-1-1 standard

Ground leakage current in mA	Grid disconnection time in seconds
30	0.3
60	0.15
100	0.04

2 Existing Transformerless Inverter Topology

The single-phase inverter is grounded at the AC side is the essential consideration for the transformerless inverter. Out of various topology, zero-state decouple topology will decouple the solar PV module during the freewheeling period from the grid, and it clamps the short circuit output voltage [9]. In the following sub-section, the outline of the conventional inverter topology and leakage current analysis is discussed.

2.1 Ground Leakage Current Analysis

Due to the electrically chargeable surface area in PV module, a capacitance created between the PV and the common ground. This parasitic capacitance creates the side effects depends on factors like the PV module, the structure of the frame, weather condition, humidity, dust etc. This capacitance varies based on the manufacturers of the PV module [10]. For example, multi-crystalline BPSolar MSX120 PV array has 75 nF/kW and thin film modules having 1000 nF/kW due to the metallic sheet which is enough for conduction of current to the common ground at the device switching frequency as shown in Fig. 2.

This leakage current depends on the inverter topology and the modulation strategy. For the analysis, a traditional single-phase full bridge inverter is considered. The equivalent CM model for the grid-tied full bridge inverter at the initial and final stage is shown in Fig. 3. Due to the parasitic capacitance, the alternating CM voltage circulates the high ground leakage current. The CM voltage is expressed as V_{cm}, and current i_{cm} is presented in Eqs. 1 and 2 respectively.

$$V_{cm} = 0.5(V_{AN} + V_{BN}), \tag{1}$$

$$i_{cm} = C_{pv}\frac{dV_{cm}}{dt}. \tag{2}$$

The differential voltage of the inverter is given in Eq. 2,

$$V_{dm} = V_{AN} - V_{BN}. \tag{3}$$

From Eqs. 1–3, the pulse voltage V_{AN} and V_{BN} is expressed in Eqs. 4 and 5 respectively.

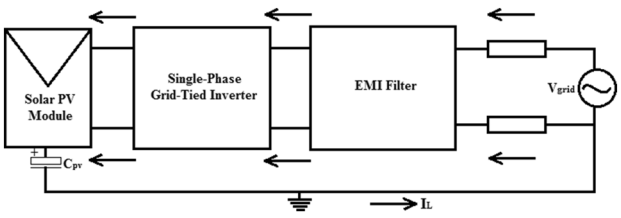

Fig. 2 Ground leakage current path of the grid-tied inverter

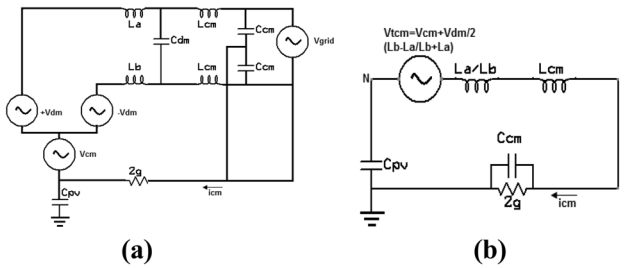

Fig. 3 The equivalent model; **a** initial stage, **b** final stage

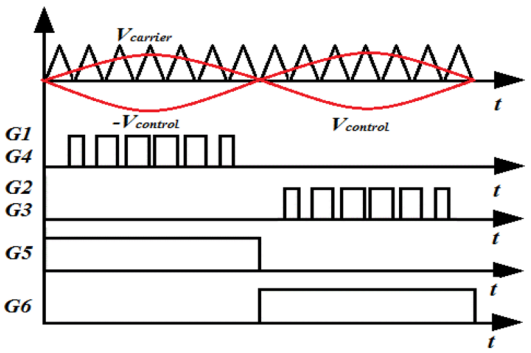

Fig. 4 Sequential logic diagram for generation of gate signal

$$V_{AN} = \frac{1}{2}V_{cm} + V_{dm}, \tag{4}$$

$$V_{BN} = \frac{1}{2}V_{cm} - V_{dm}, \tag{5}$$

where V_{AN} and V_{BN} are the pulse voltages between the points of the bridge leg and the DC negative terminal N, C_{pv} is the PV module parasitic capacitance.

From the Fig. 3b, the total CM voltage for single-phase full bridge transformerless inverter is derived and presented in Eq. 6.

$$V_{tcm} = V_{cm} + \frac{V_{dm}}{2}\frac{L_b - L_a}{L_a + L_b}, \tag{6}$$

where L_a and L_b are the grid filter inductors. L_a and L_b are equal in magnitude for the full bridge inverter family. Therefore, the Eq. 6 is modified as Eq. 7.

$$V_{tcm} = V_{cm} = 0.5(V_{AN} + V_{BN}) = \text{Constant}. \tag{7}$$

CM voltage is calculated from Eq. 7 and it is different for various topology and the modulation strategy. So, the modulation strategy is carefully designed to minimize the leakage current for the transformerless inverter. There are two modulation strategies are commonly used for full bridge inverter. In unipolar modulation strategy, when the diagonal switches (1 and 4) are turned ON, the CM voltage is expressed in Eq. 8 and when the switch 1 is turned OFF and switch 4 and 3 is turned ON, the CM voltage is expressed in Eq. 9.

$$V_{cm} = 0.5(V_{AN} + V_{BN}) = 0.5(V_{dc} + 0) = 0.5V_{dc}, \tag{8}$$

$$V_{cm} = 0.5(V_{AN} + V_{BN}) = 0.5(0 + 0) = 0. \tag{9}$$

In bipolar modulation strategy, when the diagonal switches (1 and 4) are turned ON, the CM voltage is expressed in Eq. 10 and when switch 1 and 4 are turned OFF and switch 2 and 3 are turned ON, the CM voltage is expressed in Eq. 11.

$$V_{cm} = 0.5(V_{AN} + V_{BN}) = 0.5(V_{dc} + 0) = 0.5V_{dc}, \tag{10}$$

$$V_{cm} = 0.5(V_{AN} + V_{BN}) = 0.5(V_{dc} + 0) = 0.5V_{dc}. \tag{11}$$

In the unipolar scheme, the CM voltage various from $0.5V_{dc}$ to 0 which will produce the heavy leakage current. At the same time, in the bipolar scheme, CM voltage is constant and it eliminates the leakage current problem. But, it increases the switching loss and current ripple. The unipolar scheme is beneficial in terms of filter size and less voltage ripple but the leakage current is increased. So, it is better to combine both the schemes. The structure of the circuit is modified by providing the additional device for the freewheeling path.

2.2 Analysis of the Conventional Grid-Tied Inverters

Many interesting topologies have been developed in last few years in order to solve the above-said problems. The family of grid-tied H6 solar PV inverter with/without ground leakage current issue is presented in the literature [3, 7, 10–13]. For the analysis, H6 transformerless inverter proposed in [7] is considered for discussion in this section. The sequential logic diagram for sinusoidal pulse width modulation (SPWM) is shown in Fig. 4. In which, G1–G6 is the gate driving pulses of the switching device T1–T6. The signals G1–G4 are generated by employing SPWM during the positive/negative half-cycle of the grid voltage. The devices T5 and T6 will work according to the frequency of the grid.

The modes of operation are shown in Fig. 5 and the working of the existing PV grid-connected inverter is discussed.

Mode I During the positive cycle of the grid voltage, T1 and T4 are active and T5 is always ON; the grid current flows through T1–L_a–L_b–T4 and the grid is charged with the input voltage. The current flow is shown in Fig. 5a. The output voltage is presented in Eq. 12.

$$V_{AB} = +V_{dc}. \tag{12}$$

Mode II During this mode, T1 and T4 are turned OFF. The freewheeling path is provided by switching ON T5, and the grid current flows through Grid^-–L_b–T5–D1–L_a–Grid^+ to maintain the inductor current. The grid and inverter

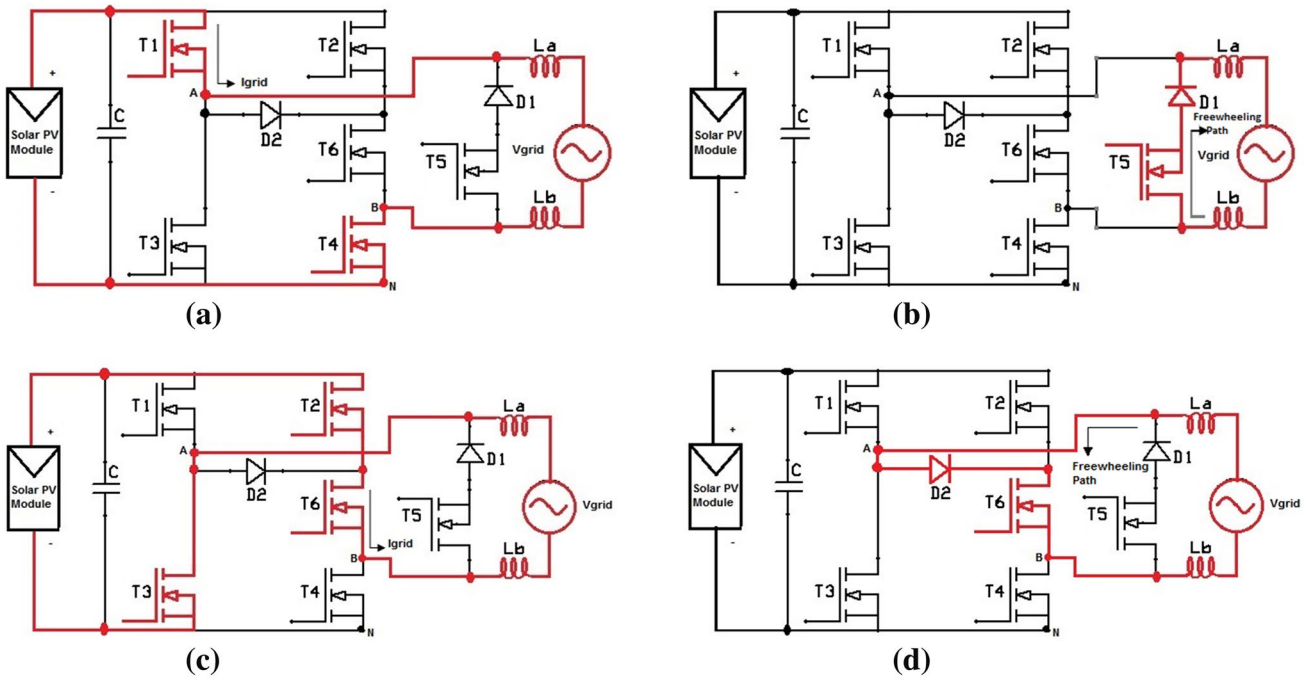

Fig. 5 Modes of operation of the conventional topology; **a** mode-I, **b** mode-II, **c** mode-III, **d** Mode-IV

are isolated during this mode of operation and the current flow is shown in Fig. 5b. The output voltage is expressed in Eq. 13.

$$V_{AB} = 0. \tag{13}$$

Mode III During the negative cycle of the grid voltage, T2 and T3 are active and T6 is always ON; the grid current flows through T2–T6–L_b–L_a–T3 and the grid will be charged with the negative input voltage. The current flow is shown in Fig. 5c. The output voltage is expressed in Eq. 14.

$$V_{AB} = -V_{dc}. \tag{14}$$

Mode IV During this mode, T2 and T3 are turned OFF. The freewheeling path is provided by T6 and the grid current flows through $Grid^{+}$–L_a–D2–T6–L_b–$Grid^{-}$ to maintain the inductor current. The grid and inverter are isolated during this mode of operation and the current flow is shown in Fig. 5d. The output voltage is expressed in Eq. 15.

$$V_{AB} = 0. \tag{15}$$

To determine the CM voltage, during positive cycle, the switch T1 and T4 is ON, the inductor current forced to freewheel through T1, T4, and T5 body diodes and decreased rapidly for enduring the reverse voltage. So, the CM voltage during this period is given in Eq. 16.

$$V_{cm} = 0.5(V_{dc} + 0) = 0.5V_{dc}. \tag{16}$$

During the freewheeling period, T1 and T3 are OFF and the voltage balance is obtained. The voltage clamped between point A and DC ground is half of the output voltage. When T2 and T4 is OFF, the voltage clamped between point B and DC ground is again half of the output voltage. Therefore, the CM voltage is given in Eq. 17.

$$V_{cm} = 0.5(0.5V_{dc} + 0.5V_{dc}) = 0.5V_{dc}. \tag{17}$$

The CM voltage between the midpoint and DC ground does not vary and is kept constant. The CM voltage formed by the DC ground to AC ground is nothing but DC offset layover with low-frequency devices and this circulates the small CM current to the equivalent CM capacitor C_{pv} by keeping capacitor value of 5 nF which allows the current of slightly above 30 mA. To limit the ground leakage current below 30 mA, the inverter structure is slightly modified in proposed topology but the modulation scheme is same as that of the conventional inverter topology.

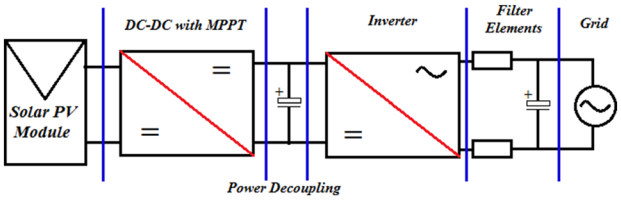

Fig. 6 Functional block of the proposed topology

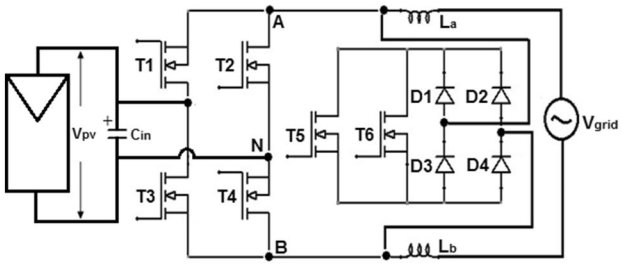

Fig. 7 Proposed H6 inverter topology

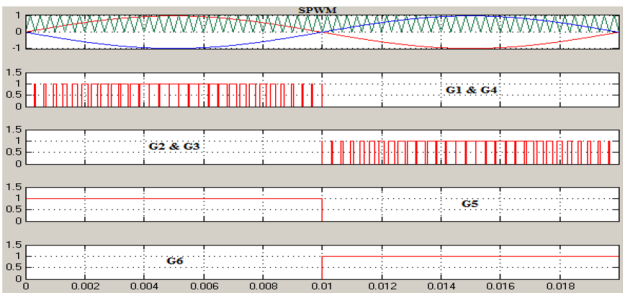

Fig. 8 Modulation scheme for the proposed topology

3 Circuit Configuration and Working of the Proposed Inverter Topology

The analytical approach is very helpful to get a better understanding of the needs, possibilities of topology and constraints of the inverter. The detailed operation of the proposed inverter discussed in the further sub-sections.

3.1 Functional Block of the Proposed System

The functional block diagram for the proposed topology is shown in Fig. 6. It consists of five basic functions to focus towards the power electronic usage. The maximum power point tracking (MPPT) controls the DC output voltage to operate the PV module at their maximum power point (MPP). Since the MPP varies with the insolation, temperature and the shading, it requires sophisticated tracking algorithms. If the inverter introduces a voltage ripple at PV, the ripple has to be kept small. The microinverter use a two-stage topology, in which DC–DC converter is attached between the PV and inverter.

If the inverter uses a voltage source inverter (VSI) for the grid interface, the inverter must have buck-characteristic. If PV module delivers a voltage lesser than the peak value of the grid, the inverter must have boost characteristics and it

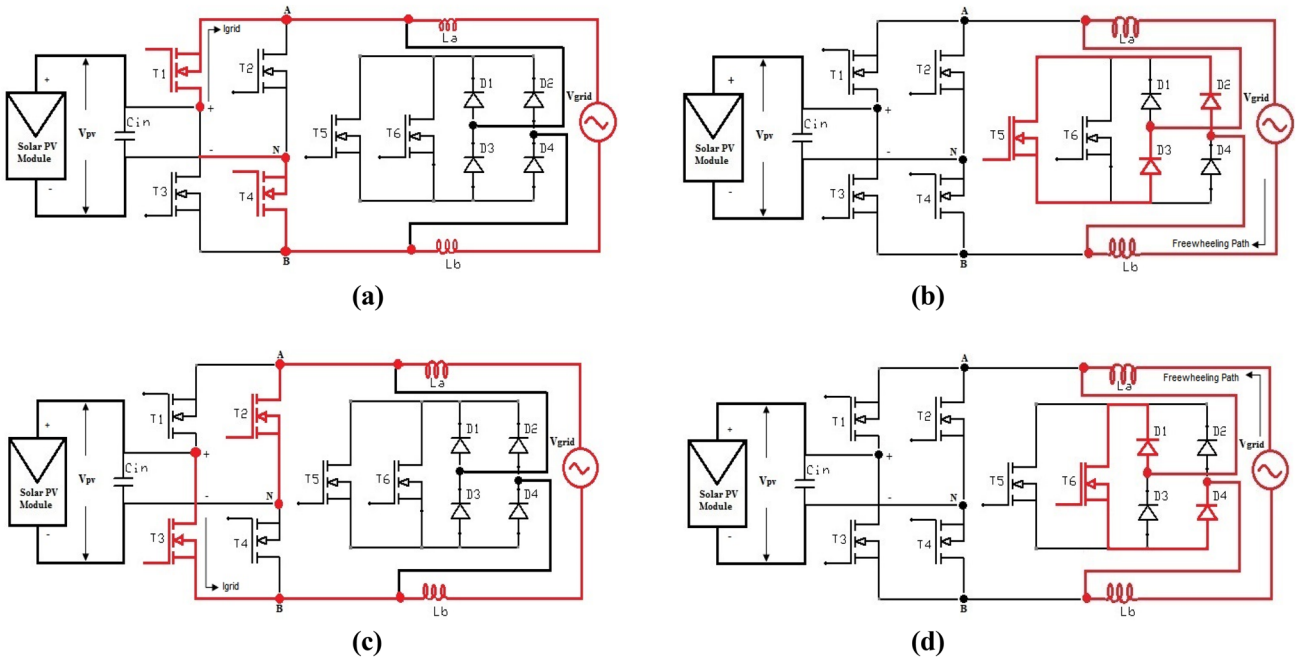

Fig. 9 Modes of operation of the proposed topology; **a** mode-I, **b** mode-II, **c** mode-III, **d** mode-IV

is achieved by the DC–DC converter. In this paper, modified H6 topology is used for the grid interface. The power swinging between DC and AC side of the inverter is decoupled by the electrolytic capacitors.

3.2 Circuit Configuration

The inverter topology is proposed and the structure is modified as shown in Fig. 7. The modulation scheme and switching pulses are shown in Fig. 8. In proposed topology, the freewheeling path is provided by the additional switches and diodes. In Fig. 7, T1–T6 are the MOSFET switches, D1–D4 are freewheel diodes, L_a and L_b are the grid filter inductors.

3.3 Operating Principle of the Proposed Topology

The modes of operation are shown in Fig. 9 and the working of the proposed PV grid-tied inverter is discussed in detail.

Mode I: During the positive cycle of the grid voltage, T1 and T4 are active. The grid current flows through T1–L_a–L_b–T4 and the grid will be charged with the input voltage. Detection of grid frequency and phase angle must be fast to get desired gate signal. The operation in mode-1 is shown in Fig. 9a. The output voltage is expressed in Eq. 18.

$$V_{AB} = +V_{dc}. \tag{18}$$

The CM voltage is given by Eq. 19,

$$V_{cm} = 0.5\left(V_{AN} + V_{BN}\right) = 0.5(V_{dc} + 0) = 0.5V_{dc}. \tag{19}$$

Mode II During this mode, T1 and T4 are turned OFF. The freewheeling path is provided by switching ON T5 and the grid current flows through $Grid^{-}$–L_b–D2–T5–D3–L_a–$Grid^{+}$ to maintain the inductor current. The grid and inverter are isolated during this mode of operation and the current flow is shown in Fig. 9b. The output voltage is expressed in Eq. 20.

$$V_{AB} = 0. \tag{20}$$

The CM voltage during this mode is derived, and it is presented in Eq. 21,

$$V_{cm} = 0.5(0.5V_{dc} + 0.5V_{dc}) = 0.5V_{dc}. \tag{21}$$

Mode III During the negative cycle of the grid voltage, T2 and T3 are active. When T2 and T3 are ON, the grid current flows through T3–L_b–L_a–T2 and the grid will be charged with the negative input voltage. The operation in mode-1 is shown in Fig. 9c. The output voltage is expressed in Eq. 22.

$$V_{AB} = -V_{dc}. \tag{22}$$

Mode IV During this mode, T2 and T3 are turned OFF. The freewheeling path is provided by turning ON T6 and the grid current flows through $Grid^{+}$–L_a–D1–T6–D4–L_b–$Grid^{-}$ to maintain the inductor current. The grid and inverter are isolated during this mode of operation, and the current flow is shown in Fig. 9d. The output voltage is expressed in Eq. 23.

$$V_{AB} = 0. \tag{23}$$

During mode-III and mode-IV, the CM voltage is derived similar to mode-I and mode-II. MOSFETs and fast acting diodes provide the freewheeling path. To achieve zero voltage state, additionally, the diode bridge rectifier and the switch T5 and T6 is connected. The switches share the load during a positive and negative cycle of the grid voltage. It enables to select the heatsink with better thermal management. Therefore, long life and reliable performance are achieved by controlling the device operating temperature within the limits.

3.4 Reactive Power Control Capability

As per the international regulation, definite reactive power should be handled by the grid-connected solar PV inverter because of the stability in grid voltage. According to the German standard VDE-AR-N-4105, the grid-connected solar PV inverter must deliver the power factor of 0.95 lagging to 0.95 leading, if the rating of the inverter is less than 3.68 kVA [11]. The phase shift will be there when the solar PV inverter absorbs or injects the reactive power into the grid. In the negative power region, the grid voltage and current are having opposite polarity so that PWM technique makes the inverter to draw the power in this region. In proposed topology, the extra switches T5–T6 and diodes D1–D4 will be activated during the phase shift between grid voltage and grid current. This operation is enough to inject the reactive power into the grid and maintains three level output voltage with the unipolar modulation scheme. So that, the leakage current is reduced and offers less harmonic distortion.

3.5 Control Strategy of the Grid Connected Inverter

The grid current is regulated as per the grid voltage and active power control. The control block diagram for the topology is shown in Fig. 10. SPWM is implemented with constant

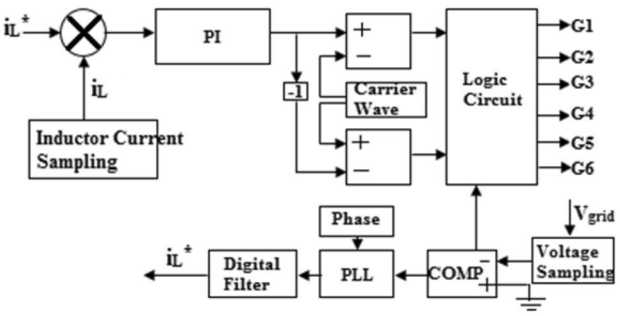

Fig. 10 Control block for the proposed topology

switching frequency which helps to design the digital filter easier. The phase-locked loop (PLL) estimates the phase angle, frequency and the reference current. The frequency and phase angle of the grid need to be detected at the fast rate for accurate generation of the reference signal. So, single phase PLL generates grid synchronous reference square wave signal. The orthogonal voltage is generated inbuilt, and it is filtered without any delay. In the control circuit, a current loop control is used and the PWM signals are generated by comparing the sine wave with the triangular carrier wave. Finally, the logic circuit splits the gate signals G1-G6 for the MOSFET switches.

3.6 Design of Grid Side Filter Elements

The inductor size and the inductor ripple current should be considered when selecting the grid filter inductor. Two identical values of inductors are used in the proposed topology. It has current ripple less than 10–20% of the rated output current. While selecting the inductor, the instant at which the current ripple reaches maximum need to be considered and it is given by the factor expressed in Eq. 24,

$$\Delta I_{factor} = M \sin \omega t - M^2 \sin^2 \omega t, \tag{24}$$

where ω is angular frequency and M is represented as modulation index. The value of ΔI_{factor} for different modulation indices are given in [11] and for the proposed inverter ΔI_{factor} is selected as 0.25. So, the value of the output filter inductor is selected as per the Eq. 25.

$$L = \frac{V_{dc} \Delta I_{factor}}{f_s \times \Delta i_L}, \tag{25}$$

where V_{dc} is the input voltage, Δi_L is the maximum ripple current, f_s is the switching frequency. The higher ripple reduces the inductor size and inductor loss but increases the conduction loss. By selecting the cutoff frequency, the output filter capacitor is calculated as per Eq. 26.

$$C_o = \frac{1}{4\pi^2 f_c^2 L_a}, \tag{26}$$

where f_c is cutoff frequency and L_a is the filter inductor as per Eq. 25. The grid voltage is constant for high switching frequency signal. The variation in the inductor current is given in Eq. 27.

$$\Delta i_L = \frac{(V_{dc} - V_{grid}) \times D \times T_s}{L_a + L_b}, \tag{27}$$

where D is the duty cycle, and V_{grid} is the grid voltage. For high switching frequency period, $V_{grid} = D \times V_{dc}$. When V_{grid} is equal to $V_{dc}/2$, the maximum inductor current is given in Eq. 28. Finally, the selected output filter must meet the condition which is given in Eq. 29.

$$\Delta i_L(max) = \frac{V_{dc} \times T_s}{4(L_a + L_b)} \leq 20\% \text{of } I_{grid}, \tag{28}$$

$$L_a + L_b \geq \frac{0.25 \times V_{dc} \times T_s}{20\% \text{ of } I_{grid}}. \tag{29}$$

3.7 DC–DC Converter with MPPT

The various DC–DC converters topology is proposed and categorized as a buck, boost, buck-boost, CUK (Single Ended Primary Inductor Converter) SEPIC etc. SEPIC converter overcomes the problem in the conventional converter and it can also buck/boost the output voltage. SEPIC based non-isolated converter offers high performance due to the non-inverting output voltage, the converter proposed in [14] is selected in this paper.

To extract the maximum PV power from the module, MPPT algorithms needed to be implemented on the converter. Many tracking algorithms are available, out of which Perturb and Observe (P&O) method, incremental conductance (IC) technique and constant voltage method are the classical methods to vary the duty cycle of the DC–DC converter [15]. The conventional IC algorithm is provided with suitable compensator and it delivers more efficiency than the technique. Finally, the classical IC algorithm with PID compensator is selected in this paper.

4 Simulation Results and Discussion

The software simulation on few H6 topologies is carried out to compare the overall performance with the proposed topology using MATLAB/Simulink software.

Table 2 Simulation parameters for the converter in [14] and the proposed inverter topology

Stages	Parameters for simulation	Ratings
Solar PV	Nominal PV voltage, V_{pv}	36 V
	Parasitic capacitance, C_{pv}	5 nF
Converter in [14]	MOSFET	100 V, 140 A
	Fast recovery diodes	200 V, 8 A
	Output capacitor	470 µF, 450 V
	Switched capacitor	10 µF, 100 V
	Coupled inductor (1:1)	$L_m = 22$ µH
Proposed inverter topology	Grid inductors, L_a and L_b	3.6 mH
	Grid side filter capacitor	10 µF, 450 V
	DC bus capacitor, C_{dc}	470 µF, 450 V
Grid interface	Grid voltage, V_{grid}	220 V
	Grid frequency, F_{grid}	50 Hz

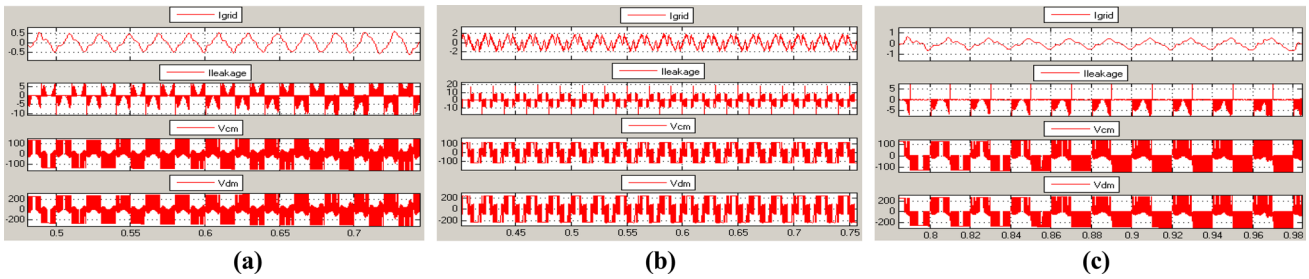

Fig. 11 Simulation waveform of grid current (upper), leakage current (middle-I), CM voltage (middle-II), DM voltage (lower) for conventional inverter topology; **a** H6 transformerless inverter proposed in [7], **b** economic H6 topology proposed in [11], **c** modified H6 topology proposed in [4]

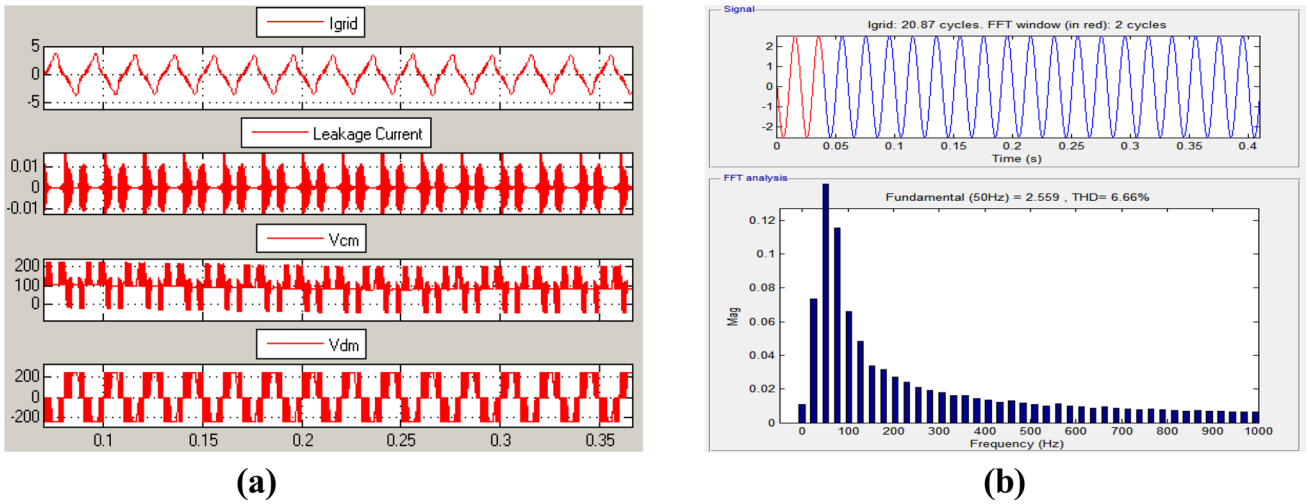

Fig. 12 Simulation of the proposed topology; **a** grid current, leakage current, CM voltage and DM voltage, **b** FFT analysis

4.1 Simulation of the Conventional and Proposed PV Inverter Topology

4.1.1 Conventional Grid-Tied Solar PV Inverter

The topologies discussed in [4, 7, 11] are having good dynamic performance and these are considered for the comparison with the proposed inverters. The solar PV grid-tied inverters are powered by solar PV module through SEPIC converter as discussed. The simulation parameters are listed in Table 2. The grid current, leakage current, CM voltage and differential mode voltage for the conventional inverters are shown in Fig. 11. Comparatively, the inverter proposed in [11] is having good differential mode (DM) characteristics with less ripple in grid current. The modulation scheme for all the topologies is semi-unipolar so that the leakage current is not acceptable according to the standard. To reduce the ripple current, large size filter needs to be used which will increase the loss further and affects the dynamic performance of the inverter.

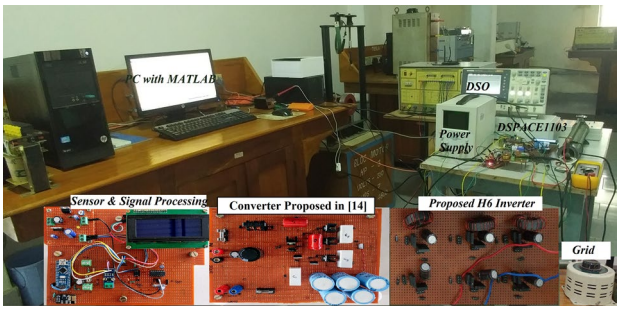

Fig. 13 Experimental setup of the proposed inverter system

The grid current of all the topologies is almost sinusoidal but Fig. 11a has distortion during negative power region, Fig. 11b has distortion during both the positive and negative power region and Fig. 11c has small distortion during positive power region. This distortion is due to the zero voltage vectors are not achieved during the positive and negative power region.

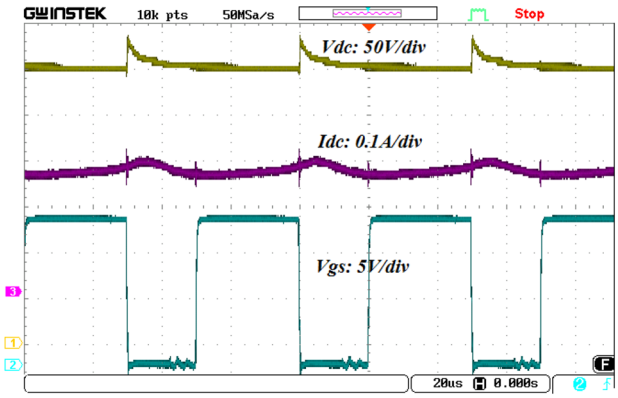

Fig. 14 Front-end DC–DC converter output waveform

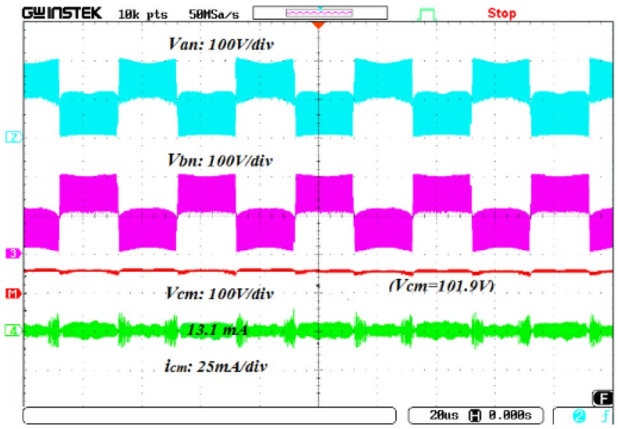

Fig. 15 Proposed inverter output waveform-I

4.1.2 Proposed Grid-Tied Solar PV Microinverter

The voltage sensor senses the grid voltage, and it is given to the single-phase PLL to generate a unity sine wave, and it is in phase with the grid voltage. The single-phase PLL also estimates the frequency and phase angle of the grid system to produce the reference grid current. The PID controller is designed and tuned to control the output current, and it ensures that the inductor current tracks the reference current. The PID controller output is multiplied with a unit sine wave and sent to the comparator. The comparator compares the given sine wave with a carrier wave and generates the gate signals for all the switches. The simulation waveform and FFT analysis of the proposed microinverter are shown in Fig. 12.

The proposed topology has three level output voltage with good DM characteristics and less ripple in grid current. As a result, the filter size reduced. From Fig. 12a, the grid current doesn't have any distortion in both positive and negative power region because of proper achievement of zero voltage vectors.

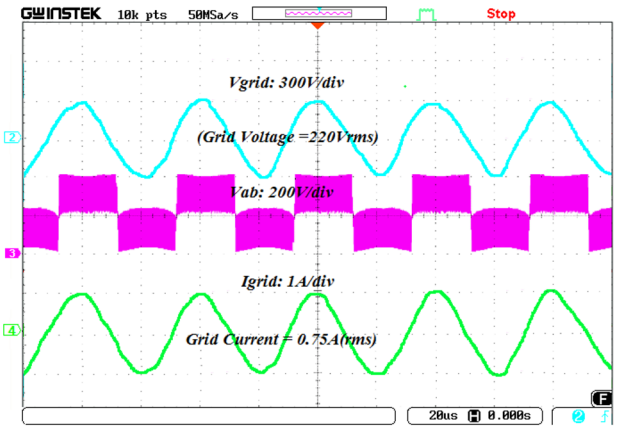

Fig. 16 Proposed inverter output waveform-II

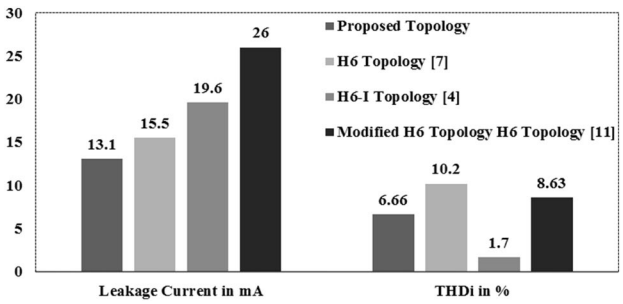

Fig. 17 Ground leakage current and THD_i comparison

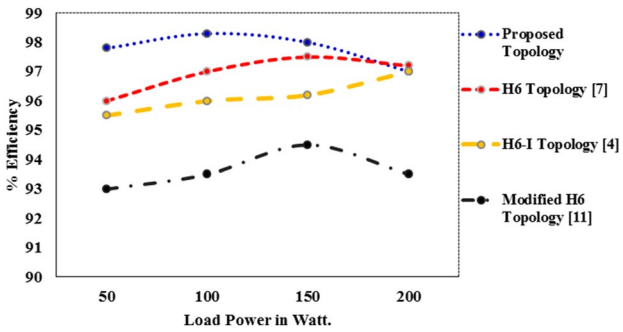

Fig. 18 Efficiency graph

From Fig. 12a, it is clear that CM voltage is maintained constant when the inverter injects the reactive power to the grid.

5 Experiment Results

The experimental prototype is shown in Fig. 13. The prototype is designed for 150 W and the experimental test was carried out. The input voltage to the proposed inverter is derived from the converter in [14] is $V_{dc} = 320$ V and

Table 3 Performance comparison among the conventional and proposed topology

Parameters	H6 in [7]	H6 in [4]	H6 in [11]	Proposed Topology
PWM scheme	Unipolar	Unipolar	Semi-unipolar	Unipolar
$I_{leakage}$ in mA	15.5	19.6	26	12.2
THD_i%	10.2	1.7	8.63	6.66
CM Voltage in V	200 (slight variation)	200 (with spikes)	100 (more variation)	≅ 100 (almost constant)
DM characteristics	Good	Good	Moderate	Good
Safety	Less safe	Less safe	Less safe	Safe

inverter is designed to deliver the output voltage V_{grid} (rms) = 220 V. The converter delivers 320 V at 60% of the duty cycle. The output voltage and output current waveform of the DC–DC converter is shown in Fig. 14, when the converter supplies its power to the proposed grid-tied inverter. The output frequency of the non-isolated inverter is 50 Hz and the input and output capacitor for the inverter is 470 µF, 450 V and 10 µF, 450 V (electrolytic) respectively and the filter inductor L_a and L_b are equal to 3 mH.

The AC source is taken as the grid for the experimental test in the laboratory. The voltage between the points A&B and DC bus negative terminal (V_{AN} and V_{BN}) with the unipolar modulation scheme is shown in Fig. 15 which gives three level output voltage. From the waveform, it is observed that the proposed inverter has unipolar modulation scheme characteristics. In Fig. 15 (refer to CH1), CM voltage is maintained almost constant. Therefore, the inverter delivers minimal ground leakage current.

In the simulation result shown in Fig. 12, while the grid current reaches zero, there is a spike occurs in CM voltage. Since the voltages V_{AN} and V_{BN} are not clamped to half of the SEPIC converter voltage during discontinuous mode, the CM voltage is changed. The inverter voltage, grid voltage and grid current waveforms are shown in Fig. 16. Since the DM voltage signal is a low-frequency signal, it delivers less leakage current.

From the laboratory test results, it can be concluded that the proposed topology reduces the ripple in grid current, leakage current and maintains the CM voltage almost constant and it can be seen in Fig. 17. In addition to less leakage current, the efficiency of the proposed inverter topology is higher than the conventional inverter. The inverter reaches the maximum efficiency of around 98% during 50–120 W as seen in Fig. 18. The performance comparison among conventional topology and proposed topology is given in Table 3.

6 Conclusion

The new topology for the solar PV based grid-tied single phase microinverter is proposed in this paper. This topology overcomes the drawbacks of conventional topologies regarding the leakage current and the efficiency. The ground leakage current is less by maintaining the CM voltage almost constant. The DM characteristics of the topology are good since the inverter and solar PV module is fully isolated during the freewheeling period. Since two switches are involved during the freewheeling period, the switching losses and conduction losses are less. The voltage stress on the switching device is also reduced because the blocking voltage across the switch is half of the input DC voltage. As per the standard DIN VDE 0126-1-1, the inverter circulates ground leakage current less than 35 mA. So, the proposed inverter is best suitable for the grid-tied microinverter rating less than 200 W.

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