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Interleaved step-down converter with capacitor-diode voltage splitter and minimum switches for low current ripple and extra-low voltage ratio

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Abstract
This paper proposes an interleaved step-down converter (ISDC) with a capacitor-diode voltage splitter. Even though the ISDC only utilizes two active switches, it can significantly step down a high input voltage to a much lower level and achieve interleaved current at output and continuous current at input without using an extreme duty ratio. In addition, the ISDC is capable of sharing output current equally between two interleaved paths by controlling the two switches. Therefore, the ISDC has lower current ripples and reduces EMI noise. The ISDC can be easily expanded only by adopting capacitors and diodes for a much higher conversion ratio, avoiding using any active switch. A comprehensive analysis of ISDC is presented, including operation principle, steady-state analysis, design consideration, expendability of the power stage, and converter comparison. A prototype of 500 W is fulfilled to deal with 400-V input and 24-V output, which has verified the accuracy of the theoretical analysis and validated the converter. Experimental results demonstrate that the ISDC achieves a peak efficiency of 92.74% at 350 W and 92.09% at full load. If synchronous rectifiers are employed, the peak efficiency can be up to 94.73%.

Article Highlights

1. Propose a high step-down converter to efficiently draw energy from high-voltage sources for low-voltage load. Furthermore, the converter is expandable to achieve a much lower output voltage.
2. Ensure continuous input and output currents, thereby reducing EMI and volume.
3. Achieve the feature of the common switch to bridge the front-end and downstream circuits to be cost-effective.

Keywords Electric vehicles · High step-down voltage ratio · Interleaved current · Capacitor-diode voltage splitter · Continuous input current · Low output current ripple

Chih-Lung Shen, Pin-Han Chen, Hong-Qing Liu and Yu-Shan Liang have contributed equally to this work.

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1 Introduction

In recent years, electric vehicles (EVs) have gained tremendous because of the advantages of eco-friendliness, low maintenance cost, and autonomous-driving development. In addition, EVs can be in charge of an energy storage bank in smart microgrid systems for energy management. In EVs, various low-voltage loads are essentially equipped and powered by the high-voltage DC bus. Consequently, step-down converters with a high conversion voltage ratio to drop the bus voltage to power in-vehicle equipment have to be adopted [1]. In addition to installation in EVs, high step-down converters also have other various kinds of applications, for instance, supplying data centers [2, 3], LED arrays [4, 5], and DC loads of microgrids [6]. Step-down converters have been enlarging their applications in many fields and becoming a converter design trend.

High step-down converters can be mainly divided into two categories: isolated structures and non-isolated ones. One advantage of isolation configuration is that it can provide the feature of galvanic isolation and obtain a high conversion ratio [7–10]. However, most isolated converters utilize a high turn ratio to carry out a high conversion ratio. Efficiency and leakage inductance consequently become other problems that must be dealt with in converter design. Besides, the feedback control with isolation will also increase the complexity of the circuitry. Non-isolated structures can be a considerable choice for the advantages over isolated ones. In a non-isolated structure, common ground between the input and output can benefit a more straightforward circuit design and feedback accuracy because of noise reduction. Easy to accomplish higher power density is another merit of a non-isolated structure [11–13].

Some buck-derived non-isolation configurations for step-down features are mainly derived from conventional converters [14, 15]. However, the buck-derived converters still cannot drop the input voltage to a much lower level except by utilizing an extreme duty cycle. Merging switched capacitors and coupled inductors into a converter design can be feasible. Nevertheless, some problems probably exist. Adopting switched capacitors will result in relatively lower regulation capability and more switches required [16–19], while coupled inductors lead to a larger size and nonlinearity in high-power applications [20–22]. Besides, more components should be used in the main stage, resulting in more sophisticated circuit structures and lower efficiency.

In high-current applications, interleaved converters are considered owing to the ability to provide more paths for current sharing and ripple suppressing. Based on the interleaving operation, this type of converter intrinsically has the advantages of easy filter design, lower current stress and ripple, and higher power-density achievement. Even with the mentioned benefits, interleaved converters need more passive and active power components, significantly increasing the converter cost and the complexity of the control mechanism, especially in multiphase configurations [23].

In [24], the interleaved converter can step down its input voltage and obtain continuous current at the output. However, it requires a total number of active switches of up to five, and a pulsating current exists at the input. In [25], the converter utilizes switched capacitors and buck-based structures to fulfill the step-down feature and obtain continuous currents at both the input and output sides. Nevertheless, this converter must employ three active switches, and the input and output ports cannot be in common ground. Besides, it lacks expandability for applications that require a much higher voltage conversion ratio.

This paper proposes an interleaved step-down converter (ISDC), as shown in Fig. 1, to overcome the abovementioned problems. The ISDC embeds a capacitor-diode voltage splitter (CDVS) and a buck-derived interleaved circuit (BDIC) to accomplish the features: extra-high voltage conversion ratio, low current ripples at both sides of input and output, minimum active switches required, cost-effectiveness, common ground, equal current sharing, and expandable ability. Capacitors and diodes structure the CDVS without any active switch, which can significantly split a high input voltage. The BDIC is a buck-derived circuit that further lowers the high voltage and ensures that the output current of the converter is continuous with low current ripples. The S_1 in Fig. 1 also serves as a bridge to connect the front-end stage, CDVS,

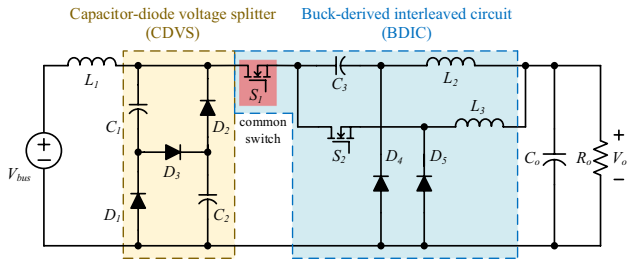

Fig. 1 The proposed interleaved extra-high step-down converter

and the downstream circuit, BDIC, based on which the proposed converter can reduce the employ of active switches to accomplish the minimum switch characteristic.

This paper consists of 8 sections. Section 2 describes the converter operation principle after the introduction in Sect. 1. In Sect. 3, the steady-state analysis of the ISDC is discussed, mainly including voltage gain, voltage stress, and current stress of semiconductors, followed by Sect. 4, which discusses the design consideration of the converter. Section 5 explains the converter expandability, while comparisons with some state-of-the-art topologies are shown in Sect. 6. Section 7 presents and discusses the experimental results measured by a prototype. Finally, Sect. 8 concludes the paper.

2 Converter operation principle

The definition of voltage polarity and current direction of ISDC is depicted in Fig. 2. The ISDC is able to operate over the total duty ratio. That is, duty ratio D ranges from 0 to 1. While D is less than 0.5, the voltage-gain expression of the ISDC is different from that when D is greater than 0.5. While D is less than 0.5, ISDC achieves a superior voltage step-down feature over that in $D > 0.5$. Therefore, $D < 0.5$ is the primary operation range.

In order to simplify the operation description, the following assumptions are considered.

1) All the components are assumed to be ideal, so the ON-resistance $R_{DS(on)}$ of the switches and equivalent series resistance of all passive components can be neglected.
2) The values of all capacitors are assumed to be large enough to keep capacitor voltages constant.
3) The inductances of L_2 and L_3 in the BDIC are identical.
4) The control signals of S_1 and S_2 have the same duty cycle D, and both are less than 0.5 with 180° out of phase.
5) The converter has been operating in a steady-state condition and continuous conduction mode (CCM).

In Fig. 2, the input is the bus voltage $V_{bus,}$ and V_o indicates the output voltage. S_1 and S_2 are power switches, D_1–D_5 denote diodes, C_1–C_3 and C_o are capacitors, and L_1, L_2, and L_3 stand for inductors. While duty ratio D is less than 0.5, the converter operation can be mainly divided into four modes over one switching period, T_s. Figure 3 depicts the conceptual waveforms; meanwhile, Fig. 4 presents the corresponding equivalents of the modes. The converter operation is discussed mode by mode as follows:

Mode 1 [$t_0 < t < t_1$]: This mode begins when S_1 is turned on. During Mode 1, switch S_2 is in the OFF state. Figure 4a shows the related equivalent circuit, in which the diodes D_1, D_2, and D_5 are forward-biased. In addition, the V_{bus} charges C_3, L_1, and L_2, and it also powers the load. At the same time, the capacitors C_1 and C_2 discharge, and the inductor L_3 releases its stored energy to the load R_o. The voltages of C_1 and C_2 are equal, that is, $V_{C1} = V_{C2}$. In addition, the voltages across inductors L_1, L_2, and L_3, v_{L1}, v_{L2}, and v_{L3}, are expressed as $V_{bus} - V_{C1}$, $V_{C1} - V_{C3} - V_o$, and $-V_o$, respectively, which are all constant. The currents i_{L1} and i_{L2} increase linearly, but i_{L3} decreases linearly. Mode 1 will last until switch S_1 is turned off at $t = t_1$.

Mode 2 [$t_1 < t < t_2$]: Mode 2 lasts for t_1 to t_2, in which both switches S_1 and S_2 are OFF. As shown in Fig. 4b, the diodes D_3, D_4, and D_5 are forward-biased, but D_1 and D_2 are OFF. The V_{bus} and the inductor L_1 are in series to charge C_1 and C_2. The voltage across inductor L_1, v_{L1}, is equal to $V_{bus} - V_{C1} - V_{C2}$. Simultaneously, the energy stored in inductors L_2 and L_3 supply the load R_o, and voltages across both inductors are identical, that is, $v_{L2} = v_{L3} = -V_o$. All inductor currents decrease linearly. This mode will end when the switch S_2 is turned on.

Mode 3 [$t_2 < t < t_3$]: The equivalent of Mode 3 is shown in Fig. 4c, in which the switch S_2 is turned on at $t = t_2$, but S_1 remains OFF. Diodes D_3 and D_4 conduct, keeping the same state as in Mode 2, but D_5 is OFF. The V_{bus} and inductor L_1 still charge the capacitors C_1 and C_2; meanwhile, the inductor L_2 forwards its energy to the load. The capacitor C_3 provides stored energy to the inductor L_3. Hence, the voltage of inductor L_3, v_{L3}, equals $V_{C3} - V_o$. When switch S_2 is turned off, Mode 3 ends.

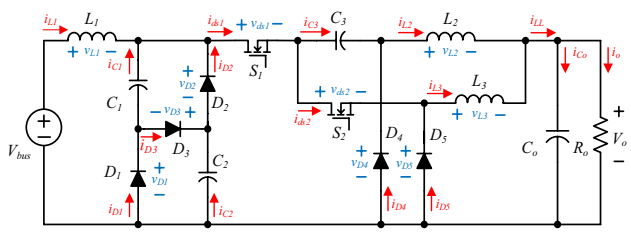

Fig. 2 Definitions of voltage polarity and current direction of the ISDC

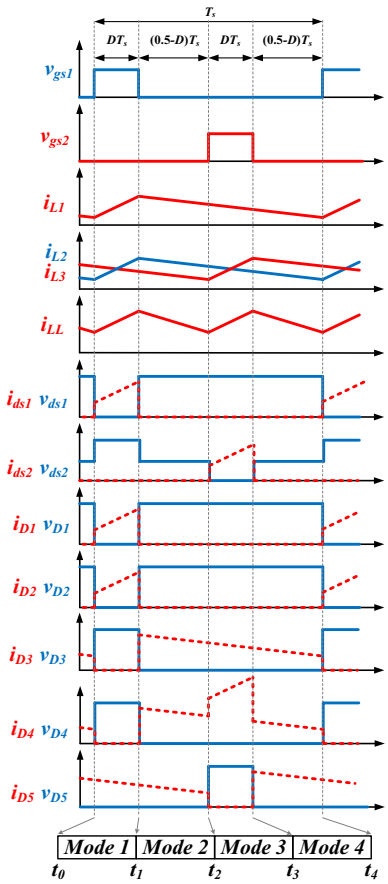

Fig. 3 Conceptual waveforms of the proposed converter in CCM

Mode 4 [$t_3 < t < t_4$]: Both switches S_1 and S_2 are OFF again in this mode. The V_{bus} and inductor L_1 charge capacitors C_1 and C_2, while inductors L_2 and L_3 release energy to the load R_o. As illustrated in Fig. 4d, the current paths resemble that in Mode 2. This mode closes when switch S_1 is turned on again, and converter operation over one switching cycle is completed.

3 Steady-state analysis

In this section, the steady-state analysis of the converter is carried out in the condition that $D < 0.5$. The study includes voltage gain, voltage and current stresses of semiconductors, inductance and capacitance calculation, and converter expandability.

3.1 Voltage gain analysis

As discussed in Sect. 2, the inductors L_1 and L_2 absorb energy in Mode 1 and release their stored energy in the other modes. In addition, the inductor L_3 absorbs energy in Mode 3 and releases its stored energy in the others. Applying the volt-second balance criterion to inductors L_1, L_2, and L_3, respectively, the relationships of (1)–(3) can be accordingly obtained.

$$(V_{bus} - V_{C1})DT_s = (V_{bus} - V_{C2})DT_s = -(V_{bus} - V_{C1} - V_{C2})(1 - D)T_s \tag{1}$$

$$(V_{C1} - V_{C3} - V_o)DT_s = (V_{C2} - V_{C3} - V_o)DT_s = V_o(1 - D)T_s \tag{2}$$

$$(V_{C3} - V_o)DT_s = V_o(1 - D)T_s. \tag{3}$$

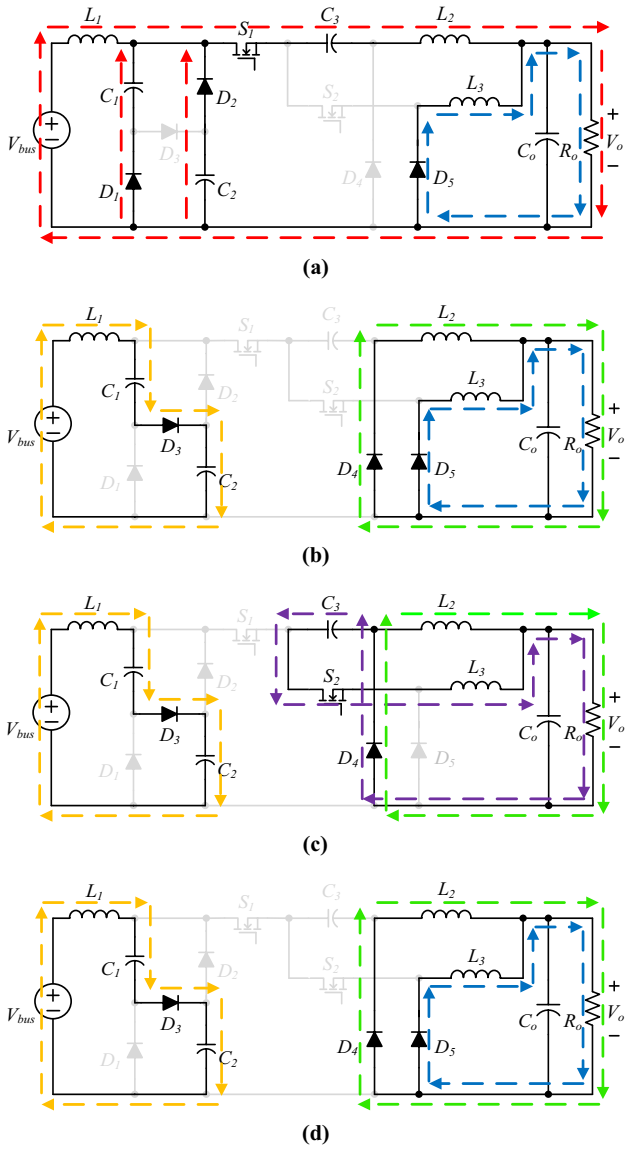

Fig. 4 Equivalent circuit of the proposed converter as $D < 0.5$. **a** Mode 1. **b** Mode 2. **c** Mode 3. **d** Mode 4

The D is the duty ratio of the switches, and T_s denotes the switching period. Solving for V_{C1}, V_{C2}, and V_{C3} from (2) and (3) yields

$$V_{C1} = V_{C2} = \frac{2V_o}{D} \tag{4}$$

$$V_{C3} = \frac{V_o}{D}. \tag{5}$$

Substituting (4) and (5) into (1) can yield the ratio of V_o to V_{bus}, M_{CCM}:

$$M_{\mathrm{CCM}} = \frac{V_o}{V_{bus}} = \frac{D}{4 - 2D}. \tag{6}$$

In (6), the expression of the converter voltage gain is for the condition that D is less than 0.5. The ISDC is able to operate over the full-range duty ratio. As the duty ratio is greater than 0.5, based on a similar procedure of derivation for voltage gain, the expression of the converter voltage gain becomes

$$M'_{CCM} = \frac{V_o}{V_{bus}} = \frac{D^2}{2-D}. \tag{7}$$

For better understanding, the relationship between voltage gain and duty ratio over $0 < D < 1$ of the proposed converter is depicted in Fig. 5, in which it can be observed that $D < 0.5$ has an excellent step-down feature.

3.2 Voltage stresses of semiconductors

Suppose the voltages across capacitors C_1, C_2, and C_3 are considered constant. Referring to Fig. 4a, the voltage stress of S_2, $V_{ds2,stress}$, can be determined, while the voltage stress of S_1, $V_{ds1,stress}$ is found based on Fig. 4c. Then,

$$V_{ds1,stress} = V_{C1} + V_{C2} - V_{C3} = \frac{3V_{bus}}{4-2D} \tag{8}$$

$$V_{ds2,stress} = V_{C1} = V_{C2} = \frac{V_{bus}}{2-D}. \tag{9}$$

To determine the diode voltage stresses for D_1, D_2, and D_5, Fig. 4c is referred to, while Fig. 4a is for the diodes of D_3 and D_4. As a result, the expression of voltage stresses of D_1–D_5 is illustrated as follows:

$$V_{D1,stress} = V_{C2} = \frac{V_{bus}}{2-D} \tag{10}$$

$$V_{D2,stress} = V_{C1} = \frac{V_{bus}}{2-D} \tag{11}$$

$$V_{D3,stress} = V_{C1} = V_{C2} = \frac{V_{bus}}{2-D} \tag{12}$$

$$V_{D4,stress} = V_{C1} - V_{C3} = \frac{V_{bus}}{4-2D} \tag{13}$$

$$V_{D5,stress} = V_{C3} = \frac{V_{bus}}{4-2D}. \tag{14}$$

3.3 Current stresses of semiconductors

According to (6), the ratio of the DC input current and output currents can be expressed as

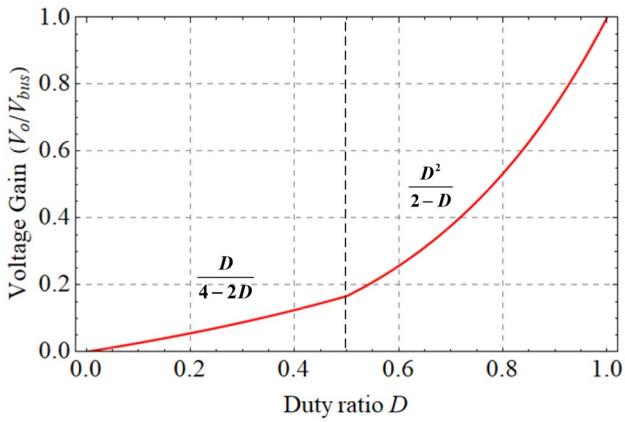

Fig. 5 The relationship between voltage gain and duty ratio over the entire range

$$\frac{I_{bus}}{I_o} = \frac{D}{4-2D}. \tag{15}$$

In ISDC, the average of the inductor current, $I_{L1(avg)}$, is equal to the input current. That is,

$$I_{L1(avg)} = \frac{D}{4-2D} I_o. \tag{16}$$

In addition, while the duty ratios of both switches are equal, the average currents of L_2 and L_3, $I_{L2(avg)}$ and $I_{L3(avg)}$, will be identical and half the output current I_o.

$$I_{L2(avg)} = I_{L3(avg)} = \frac{1}{2} I_o. \tag{17}$$

Therefore, the current stresses of S_1 and S_2 can be determined from Fig. 4a, c, respectively.

$$I_{ds1,stress} = I_{L2(avg)} = \frac{1}{2} I_o \tag{18}$$

$$I_{ds2,stress} = I_{L3(avg)} = \frac{1}{2} I_o. \tag{19}$$

For diodes, the current stresses of D_1 and D_2 can be determined based on Fig. 4a, both of which are half the inductor current of L_1 and can be expressed as

$$I_{D1,stress} = \frac{1-D}{4-2D} I_o \tag{20}$$

$$I_{D2,stress} = \frac{1-D}{4-2D} I_o. \tag{21}$$

While referring to Fig. 4b, the current stresses of D_3 and D_5 will equal the inductor current of L_1 and L_3, respectively. In addition, from Fig. 4b, c, the current stress of D_4 can be determined by the inductor currents of L_2 and L_3. Therefore,

$$I_{D3,stress} = \frac{D}{4-2D} I_o \tag{22}$$

$$I_{D4,stress} = \frac{1}{2-4D} I_o \tag{23}$$

$$I_{D5,stress} = \frac{1}{2} I_o. \tag{24}$$

4 Design consideration

4.1 Boundary condition of inductance

The determination for the inductances of L_1, L_2, and L_3 have to be contacted to ensure that the ISDC can be in CCM operation. The procedure for finding the boundary condition of an inductor is first to derive the expression of its minimum current and then set this value to zero.

The minimum current of L_1, $I_{L1(min)}$, is equal to $I_{L1(avg)}$–$0.5\Delta i_L$. The $I_{L1(avg)}$ is illustrated in (16), and the current change, Δi_{L1}, can be estimated as

$$\Delta i_{L1} = L_1 \frac{dv_{L1}}{dt} = \frac{2(1-D)V_o}{L_1 f_s}. \tag{25}$$

In (25), the f_s stands for switching frequency. Assume $I_{L1(min)}$ is zero. Accordingly, the minimum value of L_1 for CCM operation, $L_{1(min)}$, is thus obtained as

$$L_{1(min)} = \frac{2(2-D)(1-D)}{Df_s}R_o. \tag{26}$$

For L_2 and L_3, which have the same values and share output current equally with interleaving, their current ripple is estimated as

$$\Delta i_{L2} = \Delta i_{L3} = \frac{(1-D)V_o}{L_2 f_s}. \tag{27}$$

Therefore, the minimum inductance to ensure CCM operation will be

$$L_{2(min)} = L_{3(min)} = \frac{(1-D)}{f_s}R_o. \tag{28}$$

If $R_o = 4.6\ \Omega$ and $f_s = 100$ kHz, based on (26), Fig. 6a depicts the relationship between inductance L_1 and duty ratio D. Similarly, according to (28), Fig. 6b illustrates the relationship between L_2 (L_3) and duty ratio D.

4.2 Capacitance

The value of a capacitor directly influences the variation of voltage ripple. As discussed in Sect. 2, capacitors C_1 and C_2 discharge parallelly during Mode 1 and charge in series during the other modes. Therefore, the following relationship holds:

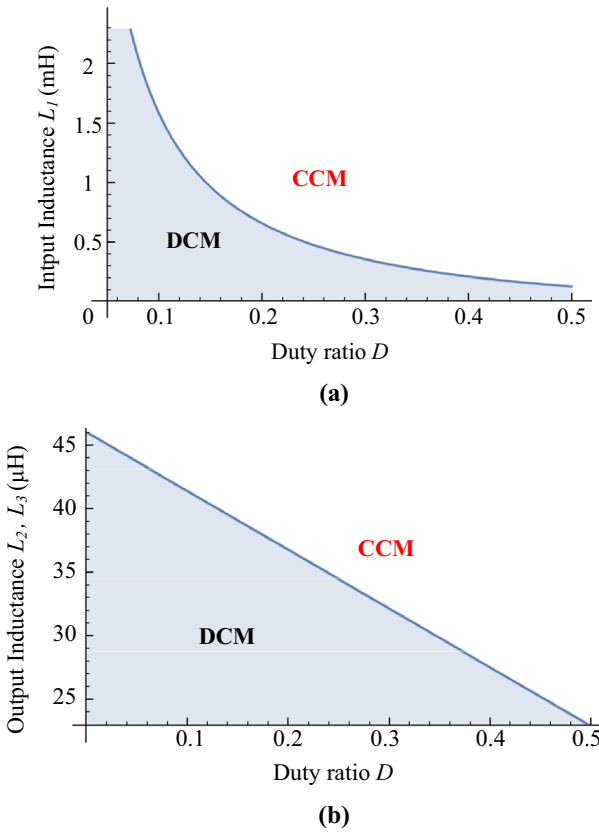

Fig. 6 The relationship between inductance and duty cycle: **a** L_1 and **b** L_2 and L_3

$$C_1\Delta V_{C1} = C_2\Delta V_{C2} = \frac{I_{L2(avg)} - I_{L1(avg)}}{2}DT_s = I_{bus}(1-D)T_s. \tag{29}$$

The capacitor C_3 charges and discharges its stored energy in Mode 1 and Mode 3, respectively.

$$C_3\Delta V_{C3} = I_{L2(avg)}DT_s = I_{L3(avg)}DT_s. \tag{30}$$

As for output capacitor C_o, it absorbs energy in Modes 1 and 3 and releases stored energy in Modes 2 and 4. Then,

$$C_o\Delta V_{Co} = \left(I_{L2(avg)} + I_{L3(avg)} - I_o\right)DT_s = \left(I_{L2(avg)} + I_{L3(avg)} - I_o\right)(0.5-D)T_s. \tag{31}$$

In addition, the DC voltages across the capacitors C_1–C_3 and C_o can be determined by (4)–(6), and the ratio of input current to output current is given in (15). Besides, the average currents, $I_{L1(avg)}$, $I_{L2(avg)}$, and $I_{L1(avg)}$, are calculated as (16) and (17). Then, substituting (15)–(17) into (29)–(31) can yield the estimation of all capacitances, which are summarized as follows:

$$C_1 = \frac{D(1-D)V_o}{\Delta V_{C1}(4-2D)R_o f_s} \tag{32}$$

$$C_2 = \frac{D(1-D)V_o}{\Delta V_{C2}(4-2D)R_o f_s} \tag{33}$$

$$C_3 = \frac{V_o D}{\Delta V_{C3} 2R_o f_s} \tag{34}$$

$$C_o = \frac{(1-2D)V_o}{16L_2\Delta V_{Co}f_s^2} = \frac{(1-2D)V_o}{16L_3\Delta V_{Co}f_s^2}. \tag{35}$$

5 Expandability

The proposed ISDC can achieve a much lower conversion ratio by increasing the number of CDVS cells, as illustrated in Fig. 7. While with m cells of CDVS, the voltage gain of the ISDC in CCM, M_{CCM_m}, is expressed as

$$M_{CCM\_m} = \frac{V_o}{V_{bus}} = \frac{D}{2+2m-2mD}. \tag{36}$$

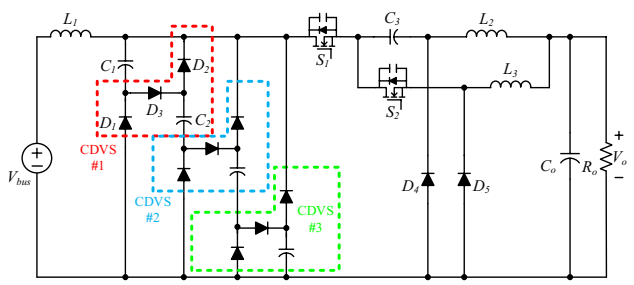

Fig. 7 The ISDC with expandability for achieving a much higher conversion ratio

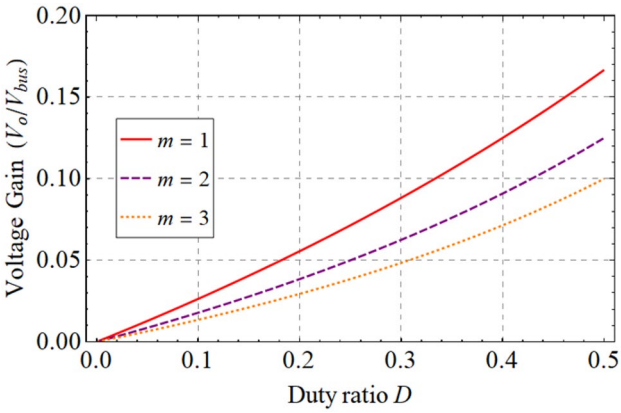

Fig. 8 The curves of the conversion ratio versus duty cycle at different *m*

For example, as shown in Fig. 7, the ISDC contains three cells of CDVS, according to (36), which can obtain a voltage gain of 0.033 under a duty ratio of 0.22. Figure 8 depicts the relationship of the voltage gain and duty ratio under different *m*.

6 Performance comparison

A performance comparison is carried out in this section to illustrate the effectiveness of the proposed converter. Table 1 summarizes the comprehensive comparison with other similar converters in the literature. Assume that turns ratio $n = 1$ for all converters and the proposed ISDC only with a single CDVS. In Fig. 9, the proposed converter can achieve a better step-down feature over a wide duty-ratio range as compared with other similar state-of-the-art converters. In addition, Table 1 describes that the proposed converter has the advantages of the common ground feature, continuous current operation on both sides of input and output, a wide range of duty-cycle processes, and expandability. Compared with the converter in [27], the ISDC can achieve a better step-down feature even with fewer components. In addition, the ISDC can be in CCM on the input side. In [28], the converter can have a more excellent conversion ratio when $D > 0.38$. However, its duty cycle is confined within 0.5, unsuitable for a wide input voltage range. Besides, this converter lacks expendable flexibility and is without continuous input current. Concerning [30], even though the converter can accomplish CCM operation at the input and output by utilizing fewer power components, its voltage conversion ratio is unsuitable for high step-down applications and without expandable ability.

Table 1 Comparison of the proposed topology and other converters

Refs.	Voltage gain	No. of components *S/D/C/M.C*	Maximum voltage stress on switch	Maximum voltage stress on diode	Common ground	Interleaved control	Maximum duty cycle	Continuous input current	Expandability
[26]	$\frac{D}{3}$	5/0/4/1	$\frac{2V_{in}}{3}$	N/A	No	No	1	No	No
[27]	$\frac{D}{3}$	8/0/6/3	$\frac{V_{in}}{3}$	N/A	Yes	Yes	1	No	Yes
[28]	$\frac{nD(1-D)}{n+1}$	4/0/2/2	V_{in}	N/A	Yes	Yes	0.5	No	No
[29]	$\frac{D(1-D)}{n+D(1-D)}$	2/2/2/2	$\frac{nV_{in}}{D-D^2+n}$	$\frac{(1-D)V_{in}}{n+D(1-D)}$	Yes	No	1	No	Yes
[30]	$\frac{D}{2-D}$	2/3/3/2	$\frac{V_{in}}{2-D}$	$\frac{V_{in}}{2-D}$	Yes	No	1	Yes	No
[31]	D^2	2/2/2/2	V_{in}	V_{in}	Yes	Yes	1	No	No
Pro	$\frac{D}{4-2D}$, $D \leq 0.5$	2/5/3/3	$\frac{3V_{in}}{4-2D}$	$\frac{V_{in}}{2-D}$	Yes	Yes	1	Yes	Yes

*S Switch, *D* Diode, *C* Capacitor, *M.C.* Magnetic core

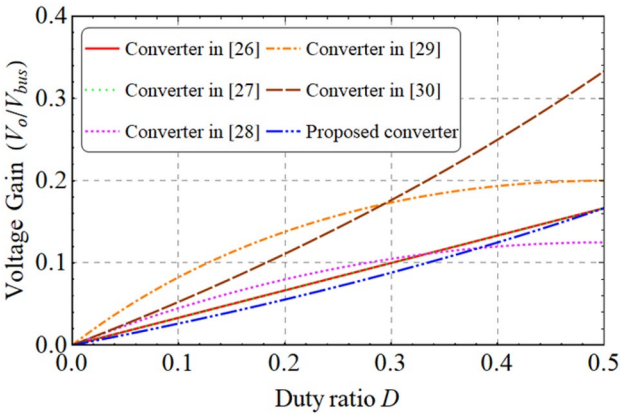

Fig. 9 Voltage gain comparison between ISDC and other similar converters

7 Experimental results

A prototype with a 500-W power rating to process 400-V bus voltage and 24-V output is developed to validate the feasibility of the proposed converter. The photo of the prototype is presented in Fig. 10. The switching frequency is 100 kHz. Detailed specifications of the prototype, along with component parameters, are provided in Table 2.

Figure 11 shows the practical waveforms, in which the duty cycles of switches S_1 and S_2 are 22%, operating at interleaving with 180° out of phase. Figure 11a presents control signals v_{gs1} and v_{gs2} and the corresponding inductor current i_{L1}. Evidently, the inductor L_1 operates in CCM. Figure 11b shows the measurement of the interleaved currents of output inductors, which illustrates that the ISDC can effectively suppress output current ripple. Figure 11c is the practical waveforms of switch S_1, which reveals that the voltage and current stresses are about 336 V and 10.41 A, respectively, in consistency with (8) and (18). For switch S_2, its voltage and current waveforms are shown in Fig. 11d,

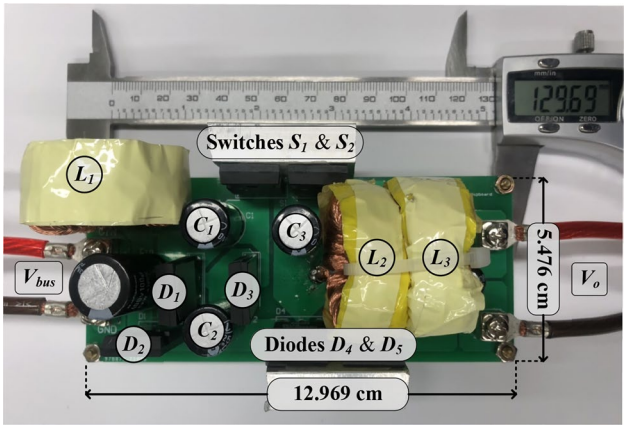

Fig. 10 The photo of the experimental prototype

Table 2 Experiment parameters and components

Parameters	Values & types
V_{bus} (DC-bus voltage)	400 V
V_o (Output voltage)	24 V
P_o (Output power)	500 W
f_s (Switching frequency)	100 kHz
L_1 (Inductor)	605 µH
L_2 and L_3 (Inductor)	36 µH
S_1 and S_2 (Power MOSFET)	IXFH36N50P
$D_1 - D_3$ (Diode)	DPG60C300HB
D_4 and D_5 (Diode)	DSSK60-02A
$C_1 - C_3$ (Electrolytic capacitor)	47 µF
C_o (Electrolytic capacitor)	200 µF

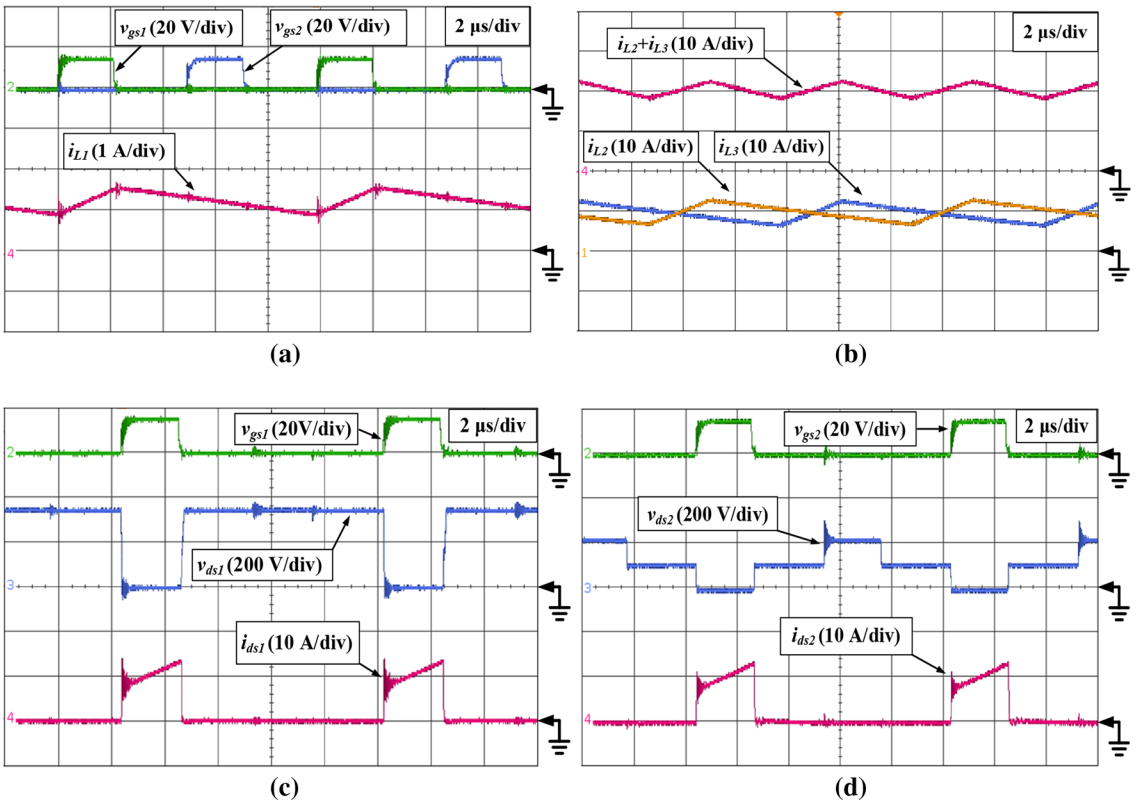

Fig. 11 Measured waveforms of the proposed converter. **a** Control signals of S_1 and S_2 and the corresponding inductor current i_{L1}. **b** The currents of L_2, L_3, and the output current. **c** Voltage and current of S_1. **d** Voltage and current of S_2

in which the voltage stress of S_2 is around 224 V, and the current stress is 10.41 A, in accordance with (9) and (19), respectively.

Figure 12 displays the measured waveform of the step-load-change response, in which the load changes from full load to half load and then returns to full load. The measured waveform reveals that the ISDC can keep its output voltage constant even under step load change. In addition, from the zoomed-in waveforms, it can be observed that the output voltage fluctuation is within 1.5 V (that is, below 6%), and the transient time is less than 0.6 ms during the loading and unloading phases of 10 A.

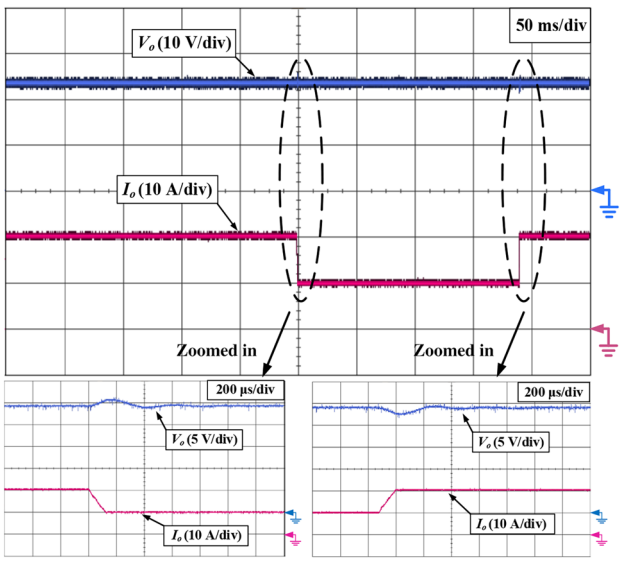

Fig. 12 Experimental result: step change of load between 10 and 20 A

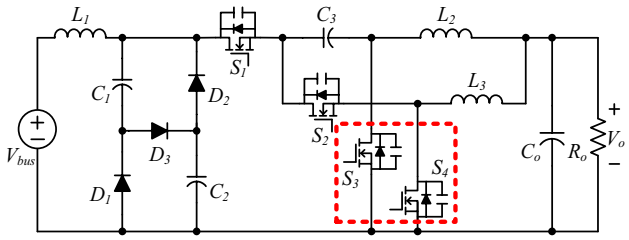

Fig. 13 The proposed converter utilizing synchronous rectifiers

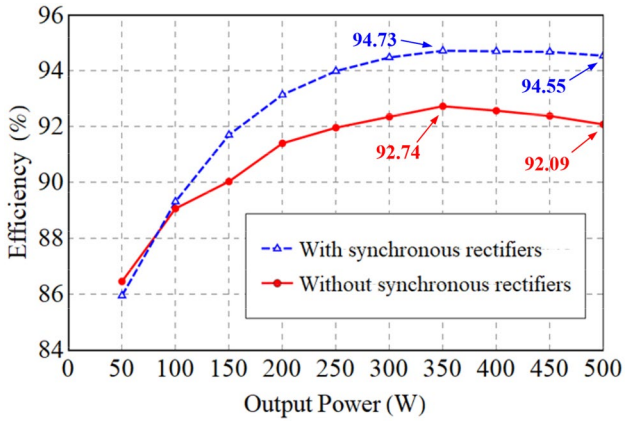

Fig. 14 Efficiency of the proposed converter with and without synchronous rectifiers

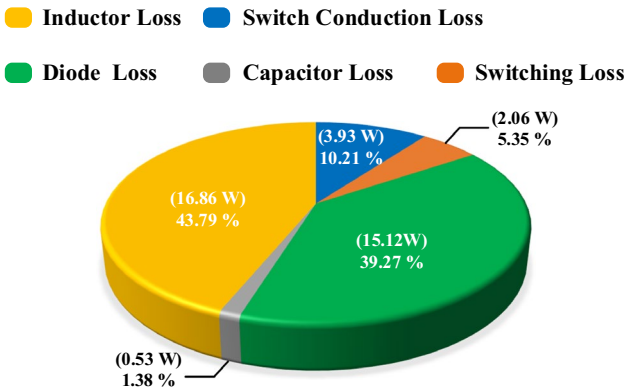

Fig. 15 The power budget of the converter at full load without the utilization of synchronous rectifiers

The diodes D_4 and D_5 can be replaced with switches S_3 and S_4 as synchronous rectifiers, as illustrated in Fig. 13, to enhance efficiency further. Figure 14 depicts the efficiency curves from light load to full load, with and without synchronous rectifiers. The maximum measured efficiency is 92.74% without synchronous rectifiers at 350 W and 94.73% with synchronous rectifiers also at 350 W load. While the ISDC is in a situation without the use of synchronous rectifiers, the power budget is estimated in Fig. 15 at full load. Diodes cause a significant part of power loss. That is, utilizing the synchronous rectifiers can accomplish a much better efficiency.

8 Conclusion

An interleaved high step-down converter, ISDC, is proposed in this paper, which is developed by embedding a capacitor-diode voltage splitter and a buck-derived interleaved circuit. The ISDC can intrinsically possess the advantages: high step-down conversion ratio, continuous current on both sides of input and output, EMI interference reduction, expandability for a much higher conversion ratio, interleaving operation at low voltage side, current ripple reduction, low voltage stress and low current stress on active switches, and high efficiency. A 500-W prototype to step down a 400-V voltage to 24 V is

carried out to validate the proposed converter. The measurements have verified the correctness of the theoretical analysis and the feasibility of the converter. The maximum efficiency is 92.74% at 350 W. While utilizing synchronous rectifiers, the maximum efficiency can increase to 94.73%. The ISDC can be easily expanded to obtain a much higher conversion ratio, only raising the number of diodes and capacitors without any additional active switch.

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Data availability The datasets generated and/or analyzed during the current study are available from the corresponding author upon reasonable request.

Declarations

Competing interests The authors declare no competing interests.

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