Research Article

An energy-efficient RAM cell based on novel majority gate in QCA technology

Ali H. Majeed[1] · Esam AlKaldy[1] · Salah Albermany[2]

Abstract
The limitations of the Complementary Metal–Oxide–Semiconductor (CMOS) technology such as the dissipated power, hard lithography, and short channel effects, led the researchers to look for an alternative technology. The unique properties of the QCA technology such as low dissipated power, speed, and the small feature size were the reason for considering it as a CMOS alternative in this work. In this paper, a new layout for five input single layer majority gate is proposed. The proposed majority gate is used in order to carry out new low power RAM cell with the ability to set the output or to reset it. Designing a cost efficient memory cell is an important issue because it is a brick unit for the whole RAM that considers the most essential component in the digital system. The proposed RAM cell shows improvement around 7% in terms of cost function and a noticeable reduction in switching energy. The QCADesigner tool is used in this work for circuit design and verification while the QCAPro tool is used for power analysis.

Keywords Quantum-dot cellular automata · RAM cell · Majority gate · QCA memory

1 Introduction

CMOS-based devices face lots of challenges including short-channel effects, hard lithography and significant increase in power dissipation [1]. QCA is one of the most important nanotechnologies presented as a possible alternative to CMOS-based devices [2, 3]. The idea of QCA was first noted in 1993 by Lent et al. [4]. QCA was implemented physically by four techniques: magnetic, metal island, molecular and semiconductor [1] and recently many papers discussed new implementation developments [5, 6]. The basic blocks in QCA are an inverter and majority voter. Many papers introduced this technique for designing a new structure of the majority gate. Design of an optimal structure of majority gate leads to improvements in the QCA circuit's performance. Other techniques were suggested to optimize QCA circuits such as [7–10]. Memory design attracted researchers' interest, especially in QCA. As in VLSI, QCA has many parameters for evaluation of the circuit performance such as delay, power dissipation, and area. The reliability of QCA circuits is also important and need to be considered carefully [11]. This research proposed a new structure of majority voter with five inputs and utilized it to design a new low power RAM cell structure. An analysis of power dissipation is also provided. The proposed design has many aspects such as lower power consumption, minimum area, single layer implementation. In addition, the inputs are placed outside the design and crosstalk is avoided which makes the gate more extendable and robust.

In this paper, QCA fundamentals are reviewed in Sect. 2, five bits majority gate are discussed in Sect. 3, QCA memory cell mechanisms have been presented in Sect. 4, the related works are provided in Sect. 5, the proposed designs

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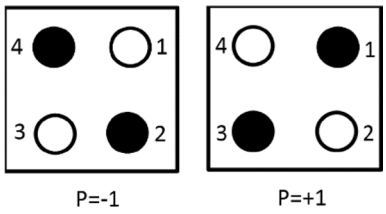

Fig. 1 The polarized QCA cell

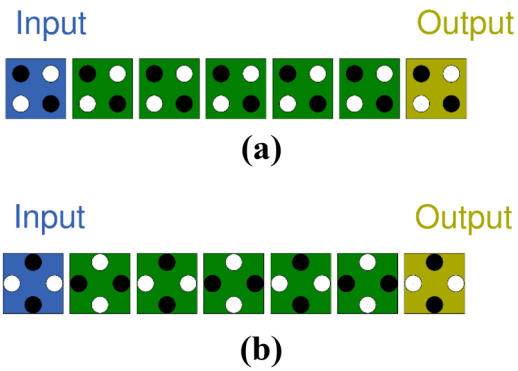

Fig. 2 QCA wire **a** normal wire, **b** rotated wire

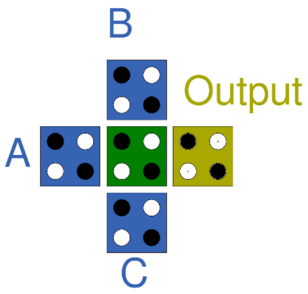

Fig. 3 Majority Gate

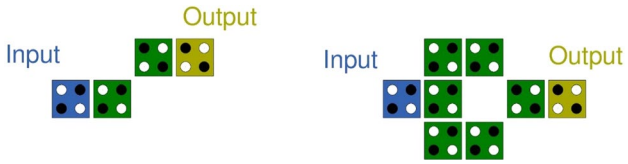

Fig. 4 QCA Inverter Forms

are introduced in Sect. 6, Sect. 7 shows the simulation results with comparison tables, finally, the conclusion will be presented in Sect. 8.

2 QCA fundamentals

The brick unit in QCA is a square cell as shown in Fig. 1. Four dots put inside each cell are regularly arranged. Two mobile electrons injected inside the cell, occupy the dots in a diagonal position due to the columbic repulsion principle. Cell polarization can be calculated using Eq. (1), and the free electrons can tunnel between the adjacent dots and cannot escape the cell due to the high intercell-potential. Because there are only two stable states, binary numbers can be represented by polarized cells. When P = + 1 is defined as logic 1 and P = – 1 as logic 0.

$$P = \frac{(p1 + p3) - (p2 + p4)}{p1 + p2 + p3 + p4}. \quad (1)$$

where pi equals 1 if the electron is present elsewhere pi = 0.

If many cells are put beside each other, QCA binary wire can be represented. Due to the coulombic interaction, the polarization of the input cell (drive cell) can transmit to the rest of the cells in the same QCA wire. The QCA binary wire is introduced in two forms normally 90° and rotated 45° as illustrated in Fig. 2 to achieve coplanar wire crossing [12]. Other approaches were suggested for coplanar wire crossing [13] since multilayer QCA circuit implementation techniques are not promising.

The main building blocks in QCA are the inverter and majority voter gate. The Majority gate for three bits can be carried out in QCA with five cells arranged as shown in Fig. 3 with a functionality as illustrated in Eq. (2). AND or OR gate can be obtained using the majority voter by connecting one of its inputs to logic 0 or logic 1 respectively.

$$\text{Maj}(A, B, C) = AB + AC + BC \quad (2)$$

The second main block in QCA is the inverter. The inverter in QCA flips the polarization and is introduced in two forms as shown in Fig. 4.

The direction of the data flow in QCA is controlled using a clock signal, which is also important to supply the power to the circuit for stimulation. The clock signal either raises or lowers the barrier between dots to prevent or allow the electrons for tunneling. The clock signal in QCA is divided into four clock phases relax, switch, hold and release to ensure adiabatic switching, each phase has a phase shift 90° from the previous and the next one. The circuit in QCA can be divided into four zones to control signal propagation, with each zone comprising four phases. The most common mechanism used in QCA as the clock signal is shown in Fig. 5 [14].

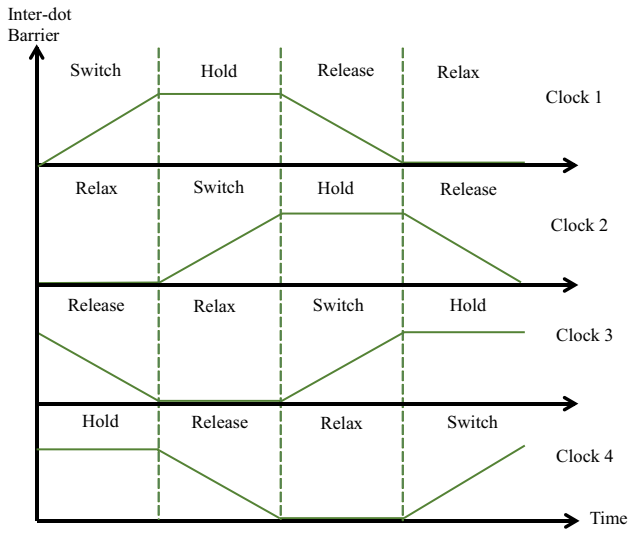

Fig. 5 QCA clock signals [14]

3 Majority-5

Majority gate with five inputs is dominant in QCA due to being used in many QCA arithmetic and memory circuits, Many structures were introduced previously [12, 15–18]. The functionality behavior of this gate illustrated in Eq. (3).

$$\text{Maj}(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE. \quad (3)$$

Figure 6 shows many previous structures proposed in the literature. Most of them have a drawback. The design shown in Fig. 6a has input cells put adjacent to each other so, it is difficult to extend. The input cells in the layout illustrated in Fig. 6b do not have the same effects. The design proposed by [17] shown in Fig. 6c cannot be implemented by a single layer because of the output cell put in the center. The above drawbacks have been overcome by the design illustrated in Fig. 6d, but this design is more complex (number of cells required) and covers a bigger area. Many fault-tolerant layouts have been introduced in [19, 20] which lead to an increase in the area and complexity of the design.

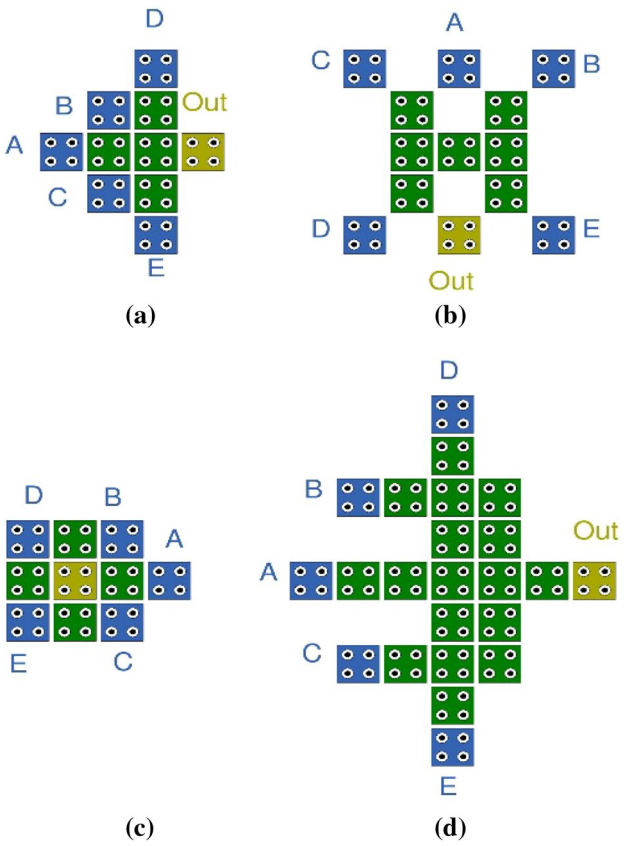

Fig. 6 Important 5 bits majority gates **a** in [15]; **b** in [16]; **c** in [17]; **d** [12]

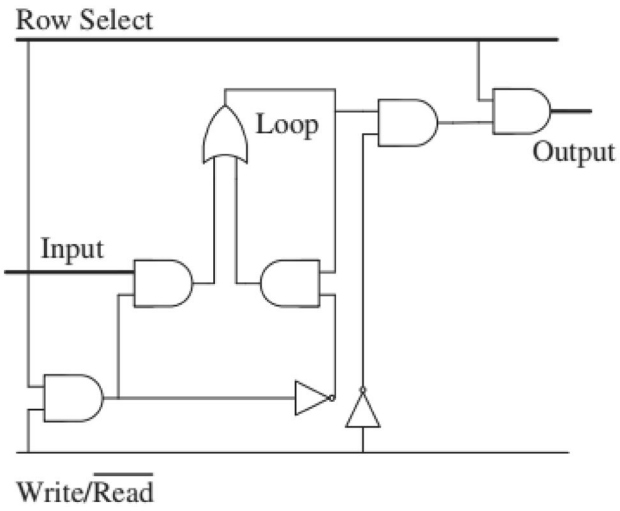

Fig. 7 Basic RAM cell schematic diagram

4 RAM cell

One of the important topics in QCA Nano-technique is designing the RAM cell. In general, there are two types of mechanism available to store the bit in QCA technology, loop-based and line-based. Feeding the bit back passing through four time zones will store the bit in a mechanism called loop-based. On the other hand, by using the QCA line architecture, the previous value was saved in a mechanism called line-based. The basic RAM cell schematic diagram is illustrated in Fig. 7 [21].

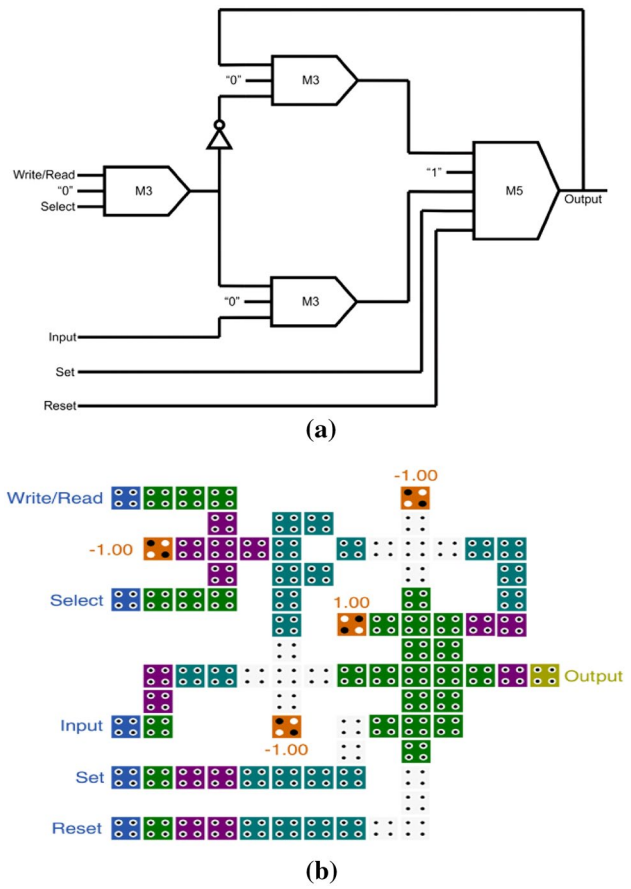

Fig. 8 RAM cell proposed in [12] **a** Schematic diagram, **b** QCA layout

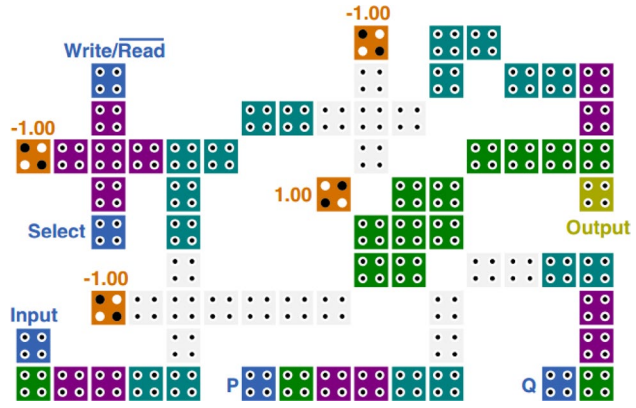

Fig. 9 The QCA layout of majority-5 based RAM cell in [1]

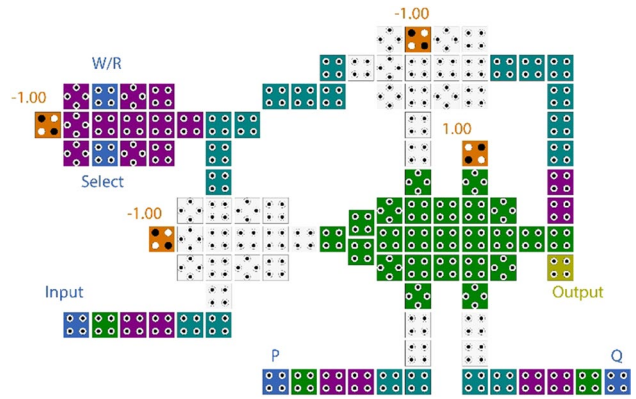

Fig. 10 Fault-tolerant memory cell presented in [22]

5 Related work

Many QCA RAM cells have been introduced in the literature. Majority-5 based efficient RAM cell schematic diagram and QCA layout were introduced earlier in [12]. This RAM cell has the ability to set and reset the output as shown in Fig. 8. In [1] they proposed a new majority gate with five inputs to implement QCA RAM cell with the ability to set output or reset it in the same manner as [12]. This RAM cell is done in a lower area and with less power than [12]. Figure 9 illustrates the structure of the majority voter-based RAM cell presented in [1].

A new design error-tolerant RAM cell is proposed by [22]. Dual fault tolerant majority voters (3-bits Maj and 5-bits Maj) are proposed based RAM cell were assessed to have many defects such as extra cell deposition, cell neglect, and cell displacement. The drawbacks of fault-tolerant designs are high complex and more cost in the function implementation. Figure 10 shows the fault-tolerant memory cell presented by [22].

6 The proposed designs

The 5-bits majority voter proposed in this paper is illustrated in Fig. 11. The proposed design has many advantages over the previous structures. The main advantages of the proposed designs are a small area, low

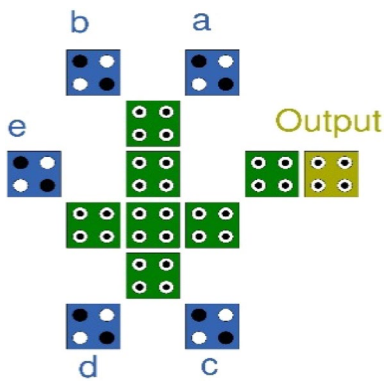

Fig. 11 Proposed majority gate (five inputs)

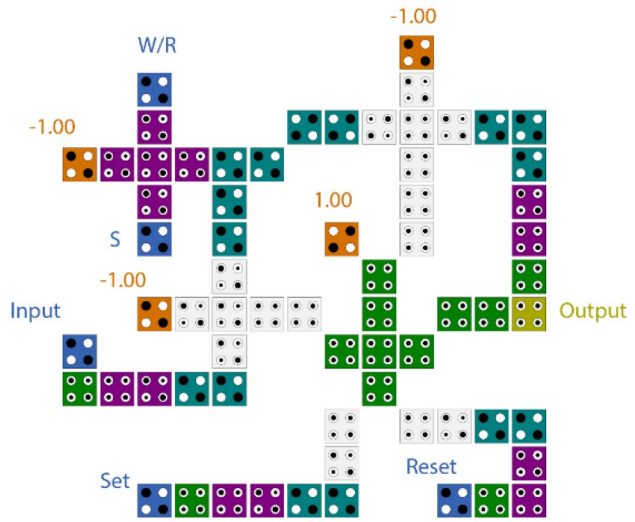

Fig. 12 The proposed structure of QCA-RAM cell

dissipated power, and low complexity. The proposed majority gate is done in a single layer which makes it more realistic for the physical implementation. The expected limitation of the proposed majority-5 is the same as the one shown in Fig. 6b but it did not cause any problems in the output as shown in the simulation results also it did not cause any error in the output when it was used in RAM cell.

Many important circuits carried out in QCA technology utilized Maj-5 as a building blocks such as an adder circuit, parity generator, and RAM cell. RAM cell was implemented in QCA following many schematic circuits, most of them utilized three-inputs majority gate (Maj-3) and five-inputs majority gate (Maj-5) in order to reduce the circuit complexity. In the proposed design, the proposed Maj-5 will be utilized as a building block in order to carry out the optimal layout QCA-RAM cell because current loop-based RAM cells are not sufficiently optimized [23].

The RAM cell which is proposed in this work is illustrated in Fig. 12. The proposed RAM cell comprises of the single gate (Maj-5), 3 gates (Maj-3), and one inverter. It is clear from Fig. 12 that the component shape selection is done to optimize the number of cells in the resulted circuit. The functionality table of the proposed RAM cell is detailed in Table 1. It is obvious from the structure

Table 1 Functionality table of the proposed RAM cell

Operation	W/R\	Select	Set	Reset	Output (t)
Read	0	1	0	1	Output (t − 1)
Write	1	1	0	1	Input
Set	X	X	1	1	1
Reset	X	X	0	0	0

that the cell consists of 4 control lines include Set, Reset, Select and Write/Read\. When the set and reset lines connected to different logical values which are '0' and '1', the selection line is enabled and if the Write/Read\ line is setting to '1', write operation will be activated, the input value will appear at the output, In addition, the read operation is done by connecting the Write/Read\ line to '0'. If Set and Reset lines are connected to the same logic value '1', set mode enabled and the output will go high (logic '1'). Similarly, reset mode enabled if the Set and Reset lines are connected to logic '0' then the output will be reset to '0'.

7 Simulation results and comparisons

QCADesigner tool was utilized with default parameters values for circuit simulation and verification. The output waveforms of the proposed Majority gate are shown in Fig. 13. The simulation results indicate the proposed design is error free. In addition, Table 2 shows the comparisons of the proposed majority-5 and their more efficient similar designs. The results prove that the proposed designs offer smaller space and fewer cells than previous designs. In addition, in order to improve the analysis and comparison of the majority gates, the energy analysis was also done utilizing the QCAPRO software and the analysis details are provided in Table 3. According to the results, the majority voter proposed in this paper leads to an average

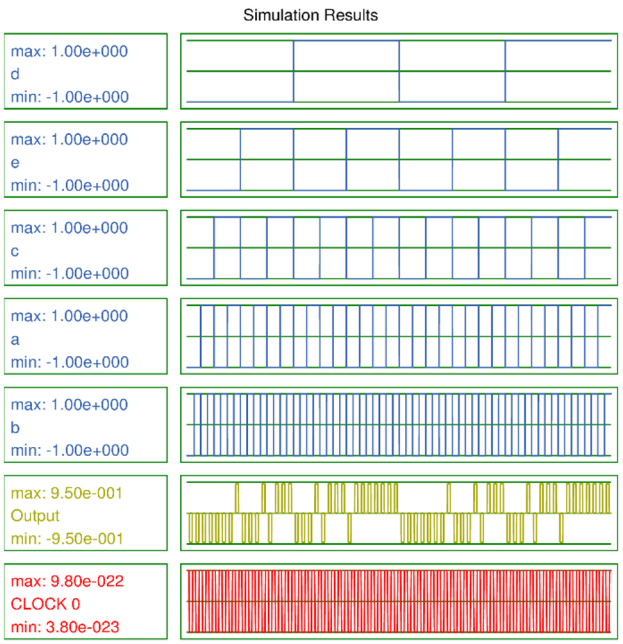

Fig. 13 The simulation output of the proposed majority-5

Table 2 Characteristics of many previous designs of 5-inputs majority gates

5-input majority gate	Area (μm^2)	Cell count	Layer
[15]	0.01	10	One
[24]	0.005	10	Multiple
[12]	0.02	23	One
[25]	0.03	42	One
[20]	0.04	51	One
[26]	0.01	17	One
[1]	0.01	14	One
[16]	0.01	13	One
[27]	0.02	18	One
Proposed	0.01	13	One

of 12% improvement in total power dissipation relative to their previous similar designs.

Figure 14 illustrates the simulation waveforms for the proposed RAM cell. The results proved that the proposed circuits are error free. In addition, Table 4 shows the performance parameters for QCA memory cells. The results show that the proposed memory cell has less complexity than its previous counterparts.

According to Table 4 results, the proposed memory cell improves the average of 6% in terms of cells counts compared to previous designs. Table 4 also provide the cost function for implementation according to [28] and using the same approach calculation as [1]. Figure 15 shows the energy dissipation analysis of many memory cells at three different tunnel power levels (0.5 E_k, 1 E_k, and 1.5 E_k) at a temperature of 2 k. According to the results taken from

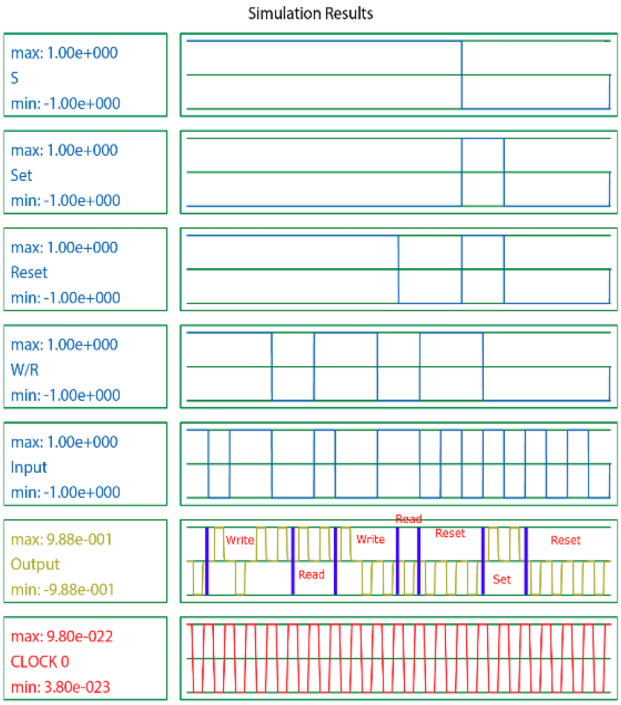

Fig. 14 The proposed RAM cell simulation result

QCAPro tool, the proposed design wastes less energy than previous similar designs. The results show that the memory cell proposed in this work leads to improvements of approximately 60%, 6% and 40% in terms of switching, leakage and total energy dissipation relative to previous similar circuits.

Table 3 The power consumption analysis for different Maj-5 gates

Maj-5 presented in	Avg. leakage energy dissipation (meV)			Avg. switching energy dissipation (meV)			Total energy consumption (meV)		
	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek
Ref. [27]	3.44	10.67	19.52	32.66	29.89	27.01	36.1	40.56	46.53
Ref. [15]	1.28	4.14	7.69	11.53	10.37	9.16	12.81	14.51	16.85
Ref. [16]	3.38	8.95	15.03	9.23	7.7	6.41	12.61	16.65	21.44
Ref. [17]	1.35	4.25	7.8	10.94	9.84	8.7	12.29	14.09	16.5
Proposed	3.67	9.42	15.57	5.77	4.71	3.86	9.43	14.13	19.42

Table 4 Comparative results of RAM cell

RAM cell	No. of cells	Area (μm^2)	Crossover	S/R ability	Clock cycle	Cost function
[21]	158	0.16	Yes	No	2	2496
[25]	109	0.13	No	yes	1.75	1862
[12]	88	0.08	No	Yes	1.5	2115
[29]	75	0.06	Yes		1.5	1368
[1]	71	0.06	No	Yes	1.25	841
Proposed	67	0.06	No	Yes	1.25	784

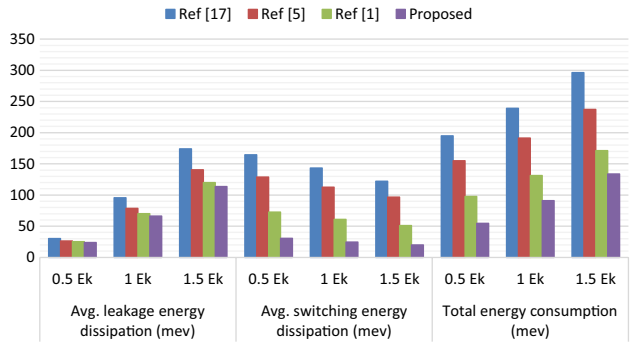

Fig. 15 Energy dissipation comparison of RAM cell

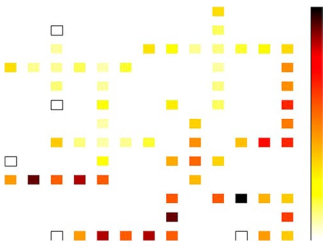

Fig. 16 The thermal energy dissipation maps for the proposed RAM cell (at 2 K) with 0.5 E_k

Figure 16 shows the map of QCA-cells dissipated power at 2 k with 0.5 E_k. In this form, dark cells represent high energy dissipation. It is clear that the proper configuration of cells in the proposed majority voter made it less energy dissipation compared to current memory cells.

Overall the results indicate that the proposed circuits have many features: lower cell counts, lower cost, lower latency, and lower power consumption as a primary circuit in digital systems.

8 Conclusions

A new layout single layer majority-5 gate is presented. The majority gate is utilized to carry out a new QCA-RAM cell with the ability to set or reset the output. QCADesigner tool is utilized in this work for circuit design and verification while QCAPro tool is used for power analysis. The advantages of the proposed designs are a small area, low dissipated power, low cost, and low complexity. The proposed circuits are done in a single layer which make them more realistic for physical implementation.

Compliance with ethical standards

Conflict of interest On behalf of all authors, the corresponding author states that there is no conflict of interest.

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