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REGULAR PAPER

Performance Analysis of the Gate All Around Nanowire FET with Group III–V Compound Channel Materials and High-k Gate Oxides

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Abstract
The increasing demand for faster and energy efficient electronics has forced the researchers to develop more power and performance efficient integrated circuits. For this purpose, the overall size of the transistor needs to be scaled down to its very limit. Transistor scaling and performance are not only limited to overall transistor design but also to the material of the channel that is being used. In order to make a performance efficient transistor, not only is a new transistor design needed but replacement of conventional channel material i.e., silicon needs to be done. In this work, a 2-D Numerical simulation model of nanowire FET with GAA technology was carried out at 22 nm gate length using an open-source nanoscale simulation tool MUGFET. Then a study of the performance parameters of this NW-GAAFET with Silicon and Group III-V compound semiconductor channel materials and High-k gate oxides has been performed. The electrical performance parameters, drain induced barrier lowering (DIBL), subthreshold swing (SS), and on/off current ratio (I_{on}/I_{off}) are extracted and validated through comparative analysis with previous high performance GAA nanowire FETs.

Keywords GAA nanowire FET · DIBL · SS · High-k oxide · Nanowire

1 Introduction

The increasing demand for more and more powerful logic devices drives the continued size and operational scaling of complementary metal oxide semiconductor (CMOS) devices. Performance benefits and greater complexity gained by scaling enable many advancements in electrical equipment. Researchers have devised a number of techniques to shrink the dimensions of a particular CMOS device without sacrificing performance. By incorporating fin field effect transistor (FinFET) [1], GAA nanowire transistors [2–4], and other possible architectures, one essential objective is to enhance the static control of the gate.

Many manufacturing firms consider the GAA nanowire transistor to be a good contender for next-generation CMOS devices due to its higher degree of efficiency and compliance with the fabrication process. But still GAA nanowire FET is not perfect to be used under 32 nm process due to short channel effects. In order to make this transistor more unsusceptible to short channel effects (SCE), a replacement of the conventional channel material silicon is needed. In this regard, Daniel Nagy et al., developed a Si-NW-GAAFET with good transistor characteristics at room temperature having a Subthreshold Swing of 70 mV/dec, DIBL of 55 mV/V, Ion of 1590 uA/um and Ioff about 9.9 uA/um [5]. In 2018, Rafael Vinicius Tayette da Nobrega et al. evaluated the modeling of nanowire GAAFET with several Group III-V [6]. The oxide material used in Rafael Vinicius' device is SiO_2, which is linked at the gate interface. But still performance was not found satisfactory, the reason being the lower relative permittivity or dielectric constant (k) [7] of SiO_2 in comparison to the other contenders for the gate oxide materials [5, 6, 8]. However, in order to improve the electrical characteristics of FETs, gate oxides based on high-k materials have significantly improved the performance of GAA nanowire FET [6, 8]. In this regard, a simulation based comparative analysis of the electrical performance of silicon (Si) and Group III-V materials in GAA nanowire FETs has been presented. Secondly, the effect of hafnium dioxide (HfO_2) and zirconium dioxide (ZrO_2) as inorganic gate insulators on the device performance has been evaluated.

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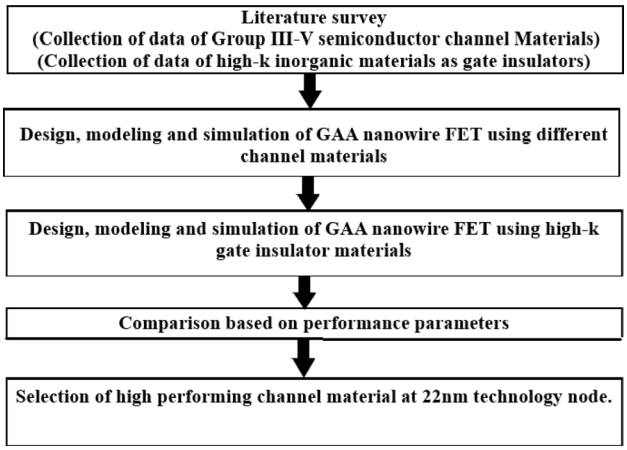


Fig. 1 Methodology followed in the simulation process

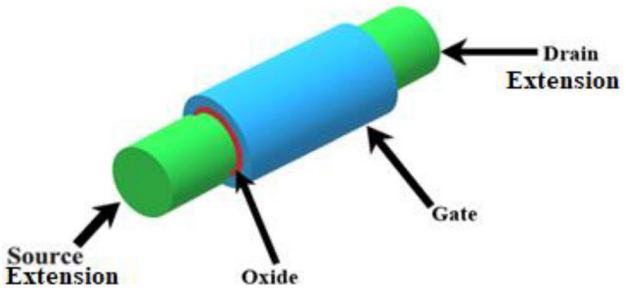


Fig. 2 3D structure of the proposed GAA nanowire FET

2 Methodology and Device Specifications

The method followed in the simulation process is shown in Fig. 1. To begin, the majority of study on the physical and electrical characteristics of channel materials, dielectric values of the gate oxides as well as the work function of the gate metal has been examined through the literature survey, which is cited as [9–21]. To develop a device with high speed and low power, a range of channel materials including Silicon (Si), Gallium Antimonide (GaSb), Gallium Nitride (GaN), Aluminum Gallium Arsenide (AlGaAs), Gallium Arsenide (GaAs), and Indium Phosphide (InP), as well as high-k gate oxides namely Hafnium Dioxide (HfO_2, k ~ 22) and Zirconium Dioxide (ZrO_2, k ~ 32) are examined. Figures 2 and 3 demonstrate the outer 3D structure of the proposed GAA nanowire FET and the cross-section device structure of a GAA n-channel nanowire FET respectively.

The proposed nanowire FET includes thickness of gate oxide (T_{ox}), diameter of channel (D_{ch}), Gate Length (L_g), length of Source and Drain terminals (L_s and L_d respectively). T_{ox}, the thickness of oxide is retained at 1.5 nm and remained constant throughout the simulations. The source & drain extension lengths were each chosen at 30.8 nm for simulation purposes, while the gate length is retained at 22 nm, and the channel diameter was kept at 12.76 nm. The doping of the drain and source is kept constant at $5E+19\ cm^{-3}$, while the channel is doped at $1E+15\ cm^{-3}$. The gate bias is set between 0 and 1 V, whereas the drain bias is set between 0.05 and 1 V for I-V characteristics while all other parameters are measured at $V_d = 1$ V. Gate overlap with the source and gate overlap with the drain have not been taken into account. Gaussian doping for source and drain is kept at 7.1 nm and penetration into oxide was kept at 0.05 nm (Table 1).

3 Results and Discussion

MUGFET (Multi-Gate Field Effect Transistor) software [22] is used to simulate the device at the nanoscale level. Before carrying out the simulations, the device is calibrated. For the calibration purpose, we compared our proposed model with the existing one in [5] at two parameters namely subthreshold swing and DIBL. A slight variation

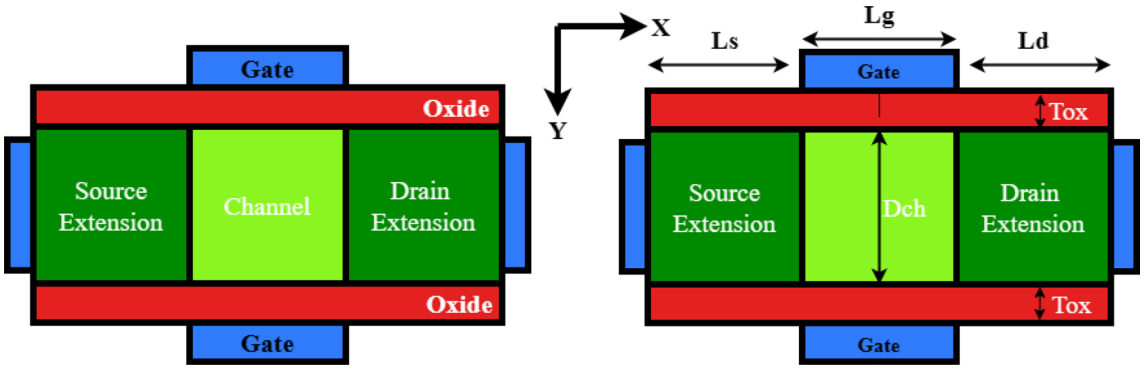


Fig. 3 Cross-section device construction in 2D for geometry x and geometry y of GAA nanowire FET

Table 1 GAA nanowire FET device dimensions and parameters

Device dimensions and parameters	
VDD, Lin [V]	0.05
VDD, Sat. [V]	1
Gate length (Lg [nm])	22
Diameter of channel (Dch [nm])	12.76
Oxide thickness (Tox [nm])	1.5
Length of source extension (Ls [nm])	30.8
Length of drain extension (Ld [nm])	30.8
Gaussian doping [nm]	7.1
Channel doping [cm^{-3}]	1.00E+15
Source/Drain doping [cm^{-3}]	5.00E+19

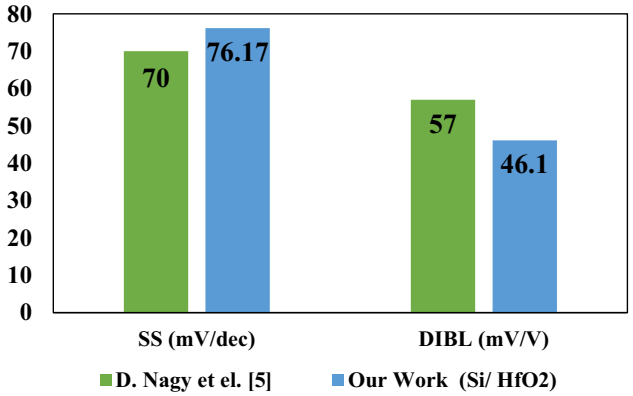
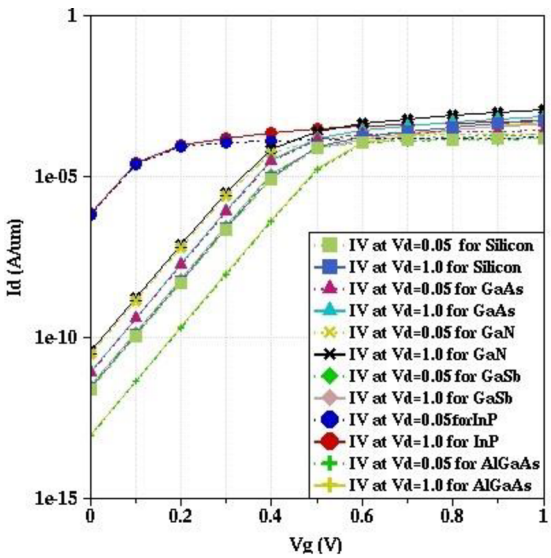


Fig. 4 Calibration of GAA nanowire transistor model parameters

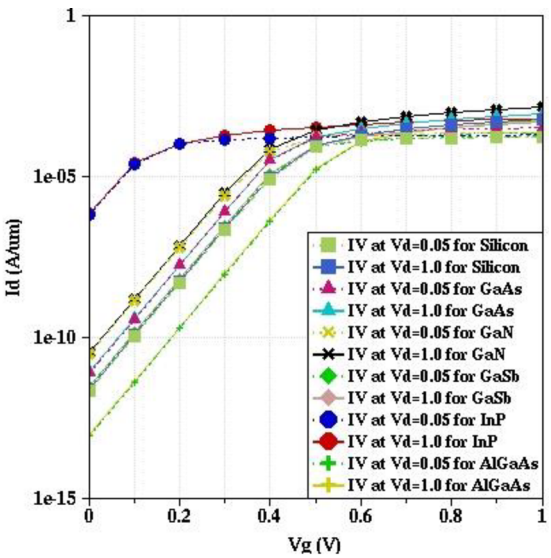
in the parameters is observed due to the simulator limitations. The respective calibration data for DIBL and SS is shown in Fig. 4 in form of bar Graphs.

We recovered the DIBL, SS, I_{on}, transconductance and ratio of I_{on}/I_{off} parameters after verifying the simulator. The study is extended to include ZrO_2 as other gate dielectric and the substitution of GaAs, GaN, GaSb, AlGaAs and InP for Si nanowire. The respective I–V Curves for different channel materials with HfO_2 as gate oxide and I-V Curves for different channel materials with ZrO_2 as gate oxide are shown in Fig. 5a and b respectively. Table 2 and 3 depict the findings of these studies and their comparison with Daniel Nagy's transistor model [5] at 22 nm of technology node and Fig. 6a, b, 7a, b, 8a, b and represent the findings of our study in the form of bar graphs. All the results have been derived at V_d and $V_g = 1.0$ V.

For the perfect transistor, a smaller subthreshold swing is always preferred because Subthreshold Swing is the gate voltage needed to shift the drain current by an order of magnitude, or one decade. Group III-V materials and AlGaAs delivers the better Subthreshold Swing than Silicon except GaN GAA-NW transistor. Lowest Subthreshold Swing was registered for InP, which is followed by AlGaAs GAA-NW transistor at second place in terms of performance. Based on the data in Tables 2 and 3, replacing the HfO_2 gate oxide with ZrO_2 resulted in a DIBL decrease for all transistors. The Subthreshold Swing of all NW-GAA-FETs also decreases when gate oxide dielectric constant increases.



(a): Comparison of I-V curves for various channel materials with HfO_2 as gate oxide



(b): Comparison of I-V curves for various channel materials with ZrO_2 as gate oxide

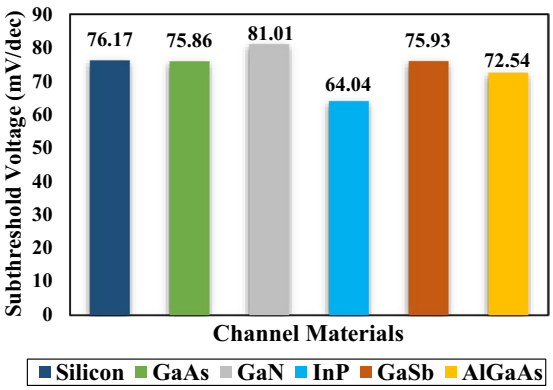
Fig. 5 **a** Comparison of I-V curves for various channel materials with HfO_2 as gate oxide. **b** Comparison of I-V curves for various channel materials with ZrO_2 as gate oxide

Table 2 Performance analysis of different channel materials using different parameters with HfO_2 as gate oxide

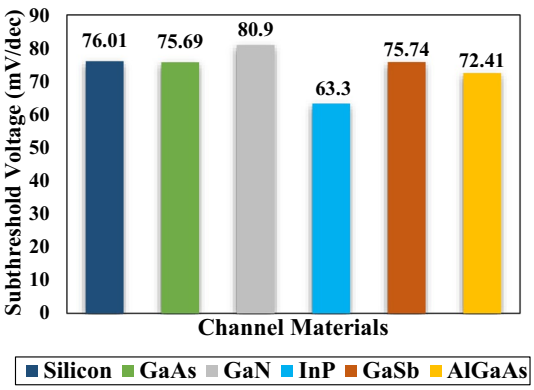
Performance parameters							
Channel material	SS	DIBL	Threshold voltage	Ion	Ioff	Ion/Ioff	Transconductance
	mV/dec	mV/V	V	A/μm	A/μm	–	S/μm
Si/HfO_2	76.17	46.10	0.53	4.99E−04	2.52E−12	1.98E+08	8.43E−04
$GaAs/HfO_2$	75.86	3.32	0.48	6.99E−04	8.24E−12	8.48E+07	1.07E−03
GaN/HfO_2	81.01	35.74	0.43	1.13E−03	3.48E−11	3.25E+07	1.81E−03
InP/HfO_2	64.04	45.70	0.22	5.02E−04	6.73E−07	7.46E+02	2.30E−04
$GaSb/HfO_2$	75.93	40.26	0.54	4.06E−04	3.10E−12	1.31E+08	6.47E−04
$AlGaAs/HfO_2$	72.54	1.84	0.60	4.50E−04	9.35E−14	4.82E+09	8.68E−04
Si/ High-k [5]	70.00	57.00	0.26	1.59E−03	9.9E−06	1.60E+04	NR

Table 3 Performance analysis of different channel materials using different parameters with ZrO_2 as gate oxide

Performance parameters							
Channel material	SS	DIBL	Threshold voltage	Ion	Ioff	Ion/Ioff	Transconductance
	mV/dec	mV/V	V	A/μm	A/μm	–	S/μm
Si/ZrO_2	76.01	36.08	0.51	5.87E−04	2.42E−12	2.42E+08	1.00E−03
$GaAs/ZrO_2$	75.69	2.73	0.47	8.24E−04	7.96E−12	1.04E+08	1.25E−03
GaN/ZrO_2	80.9	31.7	0.43	1.33E−03	3.35E−11	3.95E+07	2.16E−03
InP/ZrO_2	63.3	16.58	0.2	5.95E−04	6.61E−07	8.99E+02	2.82E−04
$GaSb/ZrO_2$	75.74	22.3	0.52	4.74E−04	2.96E−12	1.60E+08	7.56E−04
$AlGaAs/ZrO_2$	72.41	1.58	0.59	5.31E−04	8.99E−14	5.91E+09	1.04E−03
Si/ High-k [5]	70.00	57.00	0.26	1.59E−03	9.9E−06	1.60E+04	NR



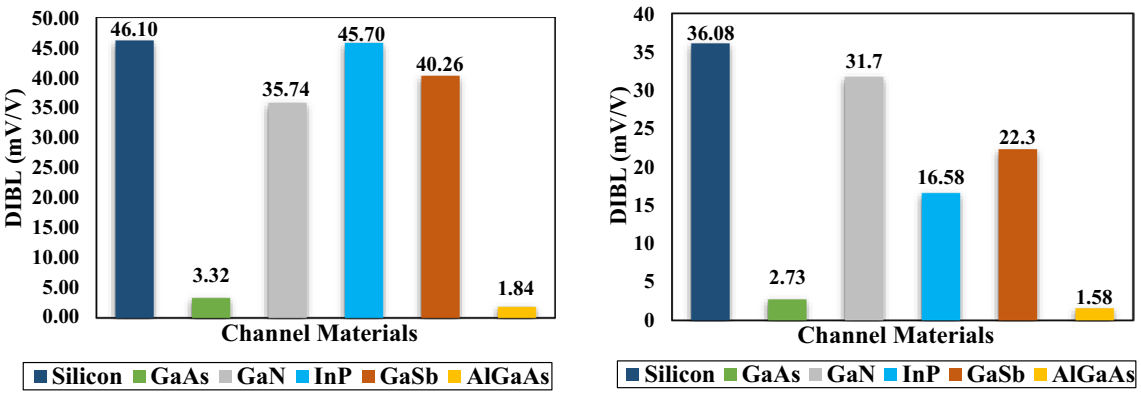
(a): Subthreshold Swing comparison for various channel materials with HfO_2 as gate oxide



(b): Subthreshold Swing comparison for various channel materials with ZrO_2 as gate oxide

Fig. 6 **a** Subthreshold Swing comparison for various channel materials with HfO_2 as gate oxide. **b** Subthreshold Swing comparison for various channel materials with ZrO_2 as gate oxide

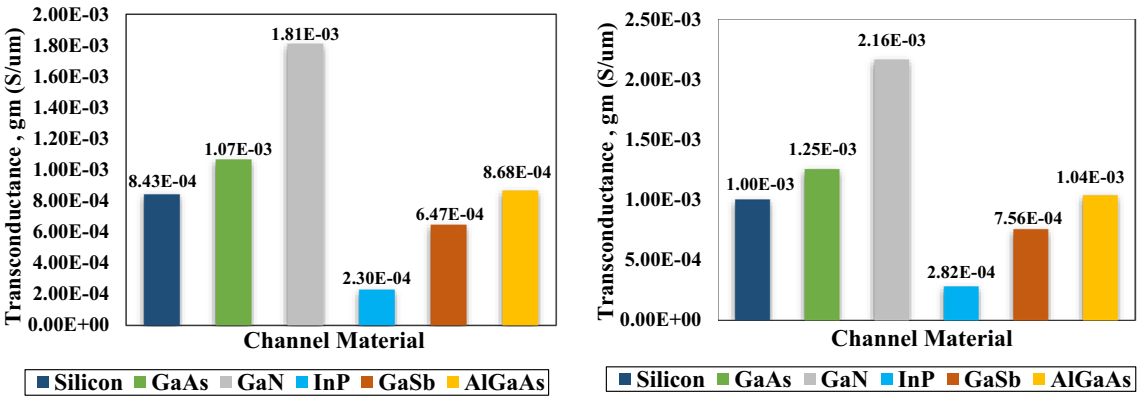
The short channel effect known as DIBL describes a transistor's threshold voltage being reduced at a greater drain voltage. Low threshold voltage leads to more leakage current. When scaling a transistor, it is usually preferable to keep it as low as possible. For Drain Induced Barrier Lowering all of the proposed materials performed better than Silicon with GaAs and AlGaAs registering the lowest of the values. In comparison to [5] our transistor model has registered a huge improvement by decreasing DIBL from 57 to 1.58 mV/V while using AlGaAs as the channel material



(a): DIBL comparison for various channel materials with HfO_2 as gate oxide

(b): DIBL comparison for various channel materials with ZrO_2 as gate oxide

Fig. 7 **a** DIBL comparison for various channel materials with HfO_2 as gate oxide. **b** DIBL comparison for various channel materials with ZrO_2 as gate oxide



(a): Transconductance comparison with various channel materials using HfO_2 gate oxide

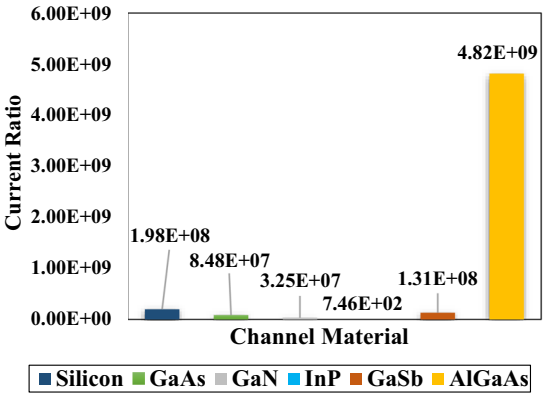
(b): Transconductance comparison with various channel materials using ZrO_2 gate oxide

Fig. 8 **a** Transconductance comparison with various channel materials using HfO_2 gate oxide. **b** Transconductance comparison with various channel materials using ZrO_2 gate oxide

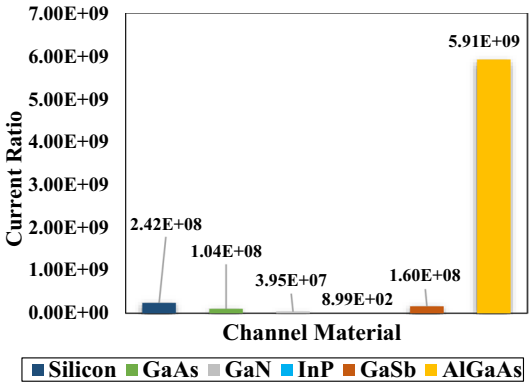
and ZrO_2 as gate oxide. This proves that a transistor using AlGaAs can maintain its threshold voltage and hence minimize the leakage current.

In the case of transconductance or the transistor gain GaN and GaAs registered the best performance numbers, followed by AlGaAs at third place which performed marginally better than Silicon. As can be seen from the comparative Tables 2 and 3, the transistor has highest gain, when the gate oxide is replaced with the dielectric of high dielectric constant (ie. ZrO_2 with k = 32.57). In this case the comparison with [5] is not possible because a proper study of transconductance parameter has not been included in the study.

Group III-V materials might have benefits in terms of some performance parameters, but they have their own disadvantages. The Group III-V materials showed a considerable drop in the electrical characteristics due to poor Leakage Current (I_{off}) performance. The comparatively lighter masses of electrons and holes of Group III-V materials result in better mobility and saturation velocity of both the carriers in the channel and hence it results in a high "On current" (I_{on}) but it also results in a high leakage current (I_{off}) therefore the ratio (I_{on}/I_{off}) is poor for Group III–V materials. Also, in comparison to AlGaAs the DIBL of Group III–V materials was high which was another factor resulting in high leakage current of Group III–V materials. However, AlGaAs is the only material which not only outperformed Silicon but every single Group III-V material by its electrical performance, due to its better DIBL performance, larger band gap and slightly heavier masses of the carriers. If we compare our AlGaAs/ ZrO_2 model with



(a): Comparison of current ratio Ion/Ioff of various channel materials using HfO_2 as gate oxide.



(b): Comparison of current ratio Ion/Ioff of various channel materials using ZrO_2 as gate oxide.

Fig. 9 **a** Comparison of current ratio Ion/Ioff of various channel materials using HfO_2 as gate oxide. **b** Comparison of current ratio Ion/Ioff of various channel materials using ZrO_2 as gate oxide

the Si/High-k model from [5] a significant improvement in the current ratio from 1.60E+04 in [5] to 5.91E+09 in our work can be seen. The comparison of I_{on}/I_{off} ratio is shown in Fig. 9a, b respectively.

4 Conclusions

In this work, results on performance analysis of Gate All Around Nanowire FET with Group III-V Compound Channel Materials and High-k Gate Oxides have been presented. A nanowire FET structure based on gate all around technology has been investigated to study the impact of replacing conventional gate dielectrics with high-k gate dielectrics and conventional channel material, silicon with group III–V materials and their compounds. The electrical performance parameters under consideration were drain induced barrier lowering (DIBL), subthreshold swing (SS), threshold voltage (V_T), current on–off ratio (I_{on}/I_{off}) and transconductance. The major findings and related conclusions are summarized and some ideas on future works are suggested.

2-D Numerical simulation model of nanowire FET with GAA technology was carried out at 22 nm gate length using an open-source nanoscale simulation tool MUGFET (multi-gate field effect transistor) available at nano-hub [22]. The nanowire FET model was simulated using high performance channel materials such as Silicon (Si), Gallium Nitride (GaN), Indium Phosphide (InP), Gallium Antimonide (GaSb), Gallium Arsenide (GaAs), and Aluminum Gallium Arsenide (AlGaAs). The effect of electric field on charge transport in the channel is investigated with high-k gate oxides; Hafnium Dioxide (HfO_2, k ~ 22) and Zirconium Dioxide (ZrO_2, k ~ 32).

The simulation results suggest that using combination of hafnium dioxide (HfO_2) with Aluminum Gallium Arsenide (AlGaAs) semiconductor channel material shows significant improvement in DIBL ~ 1.84 mV/V, subthreshold swing SS ~ 72.54 mV/dec, $I_{on}/I_{off} \sim 4.82 \times 10^9$, transconductance (gm ~ 8.68E−4) and comparable value in terms of threshold voltage $V_T \sim 0.60$ V) with respect to rest of the materials. In second investigation, combination of Zirconium Dioxide ZrO_2 with Aluminum Gallium Arsenide (AlGaAs) results in improved DIBL ~ 1.58 mV/V, $I_{on}/I_{off} \sim 5.91 \times 10^9$, transconductance (gm ~ 1.04E−03) and comparable values in terms of threshold voltage $V_T \sim 0.59$ V) and subthreshold swing SS ~ 72.41 mV/dec. The combination of Zirconium Dioxide ZrO_2 with Aluminum Gallium Arsenide (AlGaAs) clearly stands out as preferred gate oxide and semiconductor over Si/SiO_2 and $AlGaAs/HfO_2$ combination as specific and other combinations as general.

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