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REGULAR PAPER

Darlington Based 8T CNTFET SRAM Cells with Low Power and Enhanced Write Stability

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Abstract
In this paper, a novel low power and high write margin Darlington based NCNTFET Darlington 8T SRAM cell is proposed. The power consumption of the proposed Darlington SRAM cell is compared with that of conventional 6T CNTFET and conventional 8T CNTFET SRAM cells. The power consumption of the proposed Darlington SRAM cells is very less as compared to that of conventional 6T and 8T CNTFET SRAM cells for all write, hold, and read operations. The write static noise margin (WSNM) of the proposed NCNTFET Darlington 8T cell is found to increase by 70.83% than that of both conventional 6T and 8T CNTFET SRAM cell. Effect of CNTFET parameters such as chiral vectors (m,n), gate oxide thickness (Hox), dielectric constant of gate oxide material (Kox), temperature, pitch value, number of carbon nano tubes (CNTs) and supply voltage (VDD), on the power performance, drain current (I_D) and drain to source voltage (VDS) of the novel proposed Darlington SRAM cell are investigated. The write, hold, and read power consumption of proposed NCNTFET Darlington 8T SRAM cell is compared with that of some of the existing SRAM cells. The simulation is carried out using Stanford University 32 nm CNTFET model.

Keywords SRAM · CNTFET · Low power · SNM

1 Introduction

Moore's law states that in every eighteen months, the number of transistors in an integrated circuit is getting doubled. The International Technology Roadmap for Semiconductors (ITRS) has predicted that the silicon (Si) has reached its scaling limits [1]. The minimization of the size of metal oxide semiconductor field-effect transistor (MOSFET) below 10 nm has several demerits such as high leakage power, quantum effects, PVT variation, etc. Hence, electronics engineers are in need to search for the best alternative device instead of MOS transistors [2]. Carbon Nano Tube Field Effect Transistor (CNTFET) is one of the promising semiconductor devices to overcome all the limitations of Si technology at nanoscale regime. CNTFET has many favourable electrical characteristics like high ON to OFF current ratio, ballistic transport, good transconductance, low power consumption, and least PVT variation [3].

1.1 Carbon Nano Tube Field Effect Transistor

CNTFET is obtained by replacing the conducting channel of MOSFET by a carbon nano tube (CNT) (Fig. 1). CNT is a graphene sheet rolled up in cylindrical form [4]. CNTFETs are classified into two categories based on number of layers of graphene. One is single walled CNT (SWCNT) and another one is multi-walled CNTs (MWCNTs) [5]. The structure of SWCNTs and MWCNTs is shown in Fig. 2. The electrical characteristics of CNT are determined by chiral

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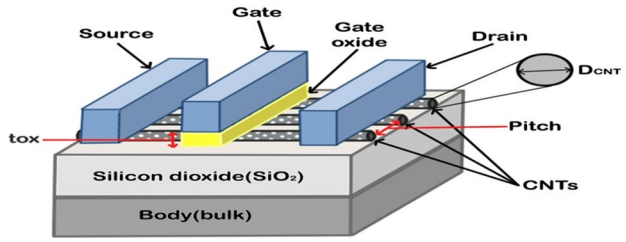


Fig. 1 Structure of CNTFET

vector or chirality of the CNT. Figure 3 shows the honeycomb structure of graphene sheet and various types of CNTs. The width of CNTFET (WCNT) is determined by [1]

$$W_{CNT} = (N-1)S + D_{CNT} \tag{1}$$

Here, N is the number of CNTs used, S is the distance between parallel CNTs also called pitch value of CNTFET, D_{CNT} -diameter of CNTs.

The chiral vectors (m, n), the threshold voltage of CNTFET (Vth), and the diameter of the CNT (D_{CNT}) are related by the following expression [1].

$$DCNT = \frac{a\sqrt{n^2 + nm + m^2}}{\pi} \tag{2}$$

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \tag{3}$$

Here a—carbon atomic distance, V_π—carbon bond energy ($V_\pi = 3.033$ eV) and e-charge of electron [1].

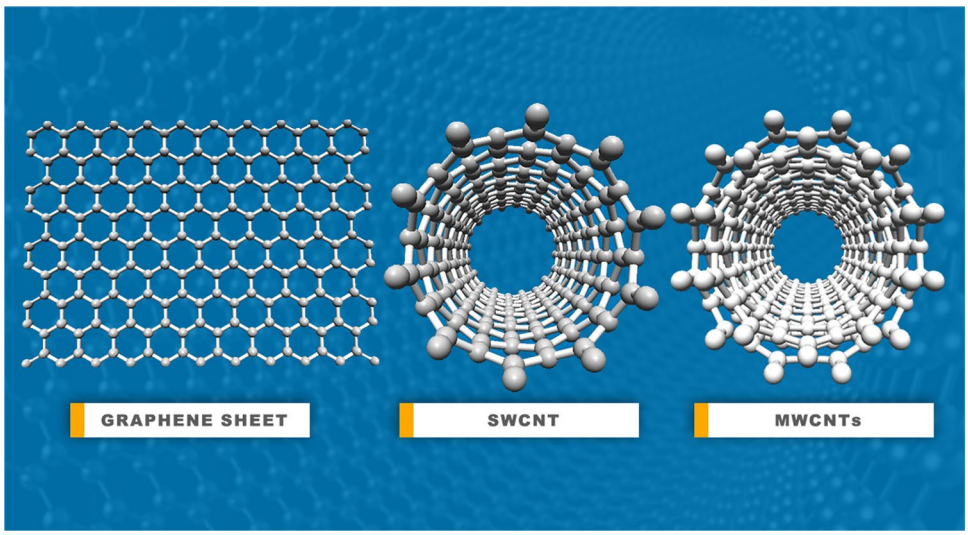


Fig. 2 Structure of graphene sheet, SWCNT and MWCNT

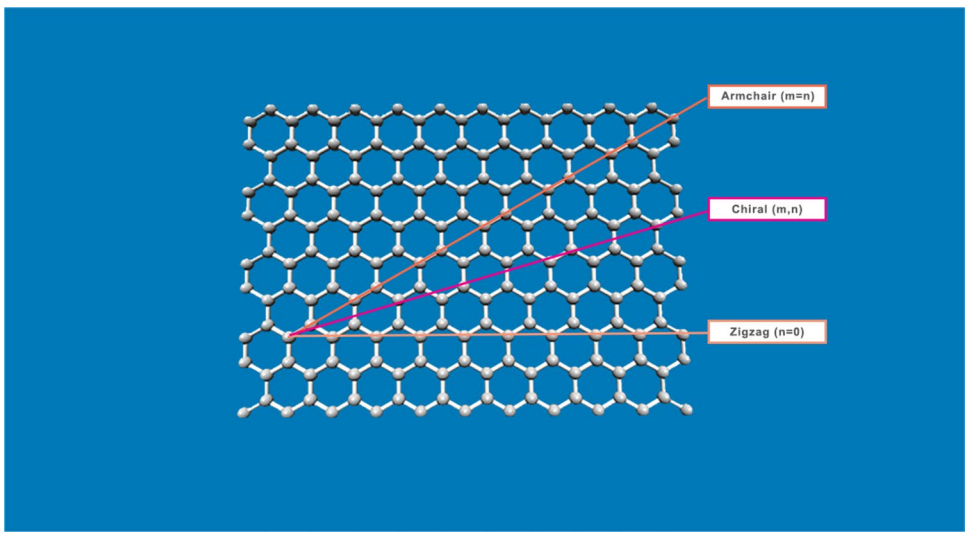


Fig. 3 Honeycomb structure of a graphene sheet, armchair, zigzag and chiral types

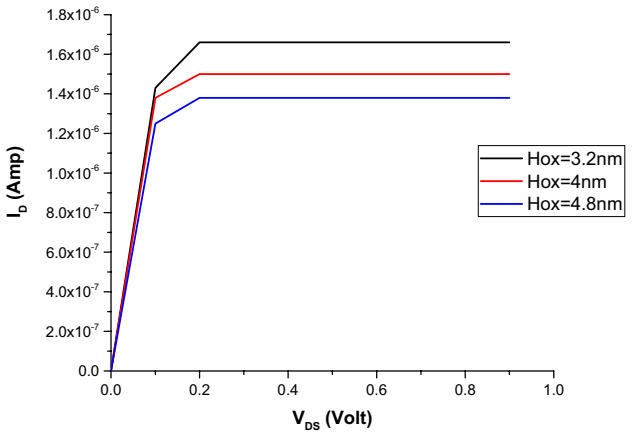


Fig. 4 I_D versus V_{DS} for various gate oxide thicknesses

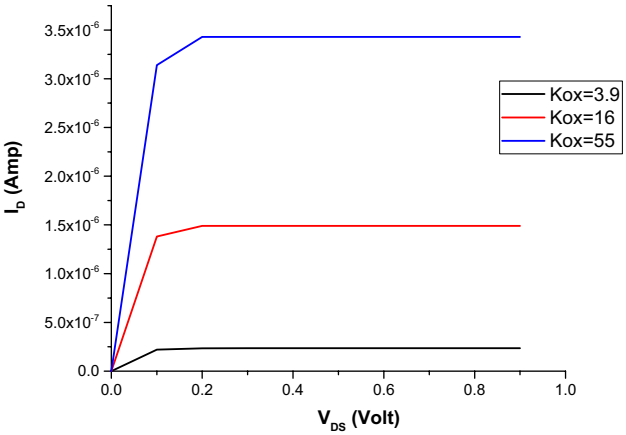


Fig. 5 I_D versus V_{DS} for various gate dielectrics constants

Leakage power and the power delay product of CNTFET based circuits are seventy-five and hundred times lower than that of MOSFET based circuits respectively. The effect of variation of process, voltage, and temperature on CNTFET is much lower as compared with that of MOSFET device [6, 7]. The chiral vectors are directly related to D_{CNT} and inversely proportional to the V_{th}. Hence, increase in m and n values increases the diameter of CNT, which in turn increases the amount of current flow in the CNTFET. Therefore, the power consumption is also increased. Increasing chiral vectors, decreases the threshold voltage of the CNTFET. At high values of chiral vectors, a minimum gate voltage is sufficient to switch ON the CNTFET [7].

Quantum capacitance determines the delay in a MOSFET and is found to increase with gate voltage but in the case of CNTFET, the quantum capacitance decreases with increasing gate voltage above 0.5 V. The threshold voltage of CNTFET is inversely proportional to the temperature. Increase of temperature from 27 °C to 227 °C decreases the threshold voltage of the CNTFET by a margin of 4.6% only [8, 9]. Variations in gate oxide thickness affects drain current capability of CNTFET. The decrease in gate insulator thickness, decreases the threshold voltage of CNTFET and increases the gate leakage current. This, in-turn increases the power consumption of the circuit [5]. Dielectric constant is directly proportional to gate capacitance, thus increase in the value of dielectric constant decreases the threshold voltage of CNTFET [10]. Hence, the power consumption of CNTFET is increased with increasing of dielectric constant value [11]. The dielectric constant (Kox) of silicon dioxide (SiO_2), hafnium oxide (HfO_2), and titanium oxide (TiO_2) are 3.9, 16, and 55 respectively.

Drain current (I_D) as a function of drain to source voltage (V_{DS}) is calculated for various oxide thickness, dielectric constant, chiral vectors, temperature, number of CNTs, and pitch value. Figures 4, 5, 6, 7, 8 and 9 are showing the

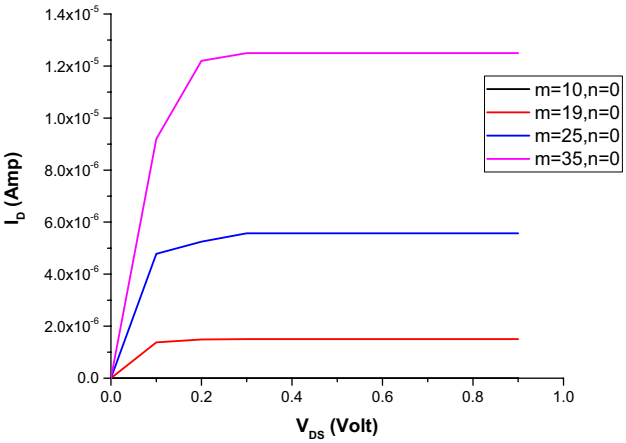


Fig. 6 I_D versus V_{DS} for various chiral vectors

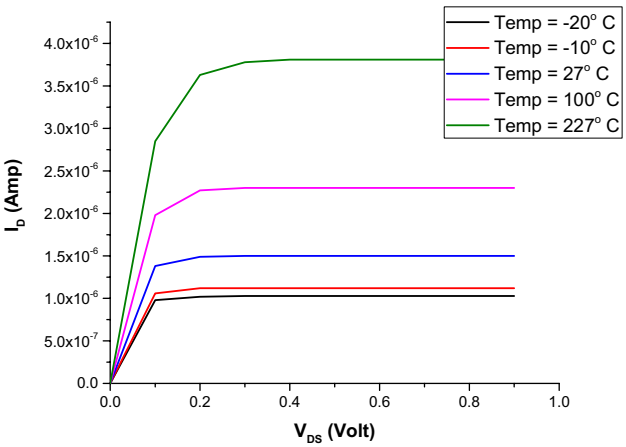


Fig. 7 I_D versus V_{DS} curve for various temperature values

variation drain current (I_D) and drain to source voltage (V_{DS}) of CNTFET.

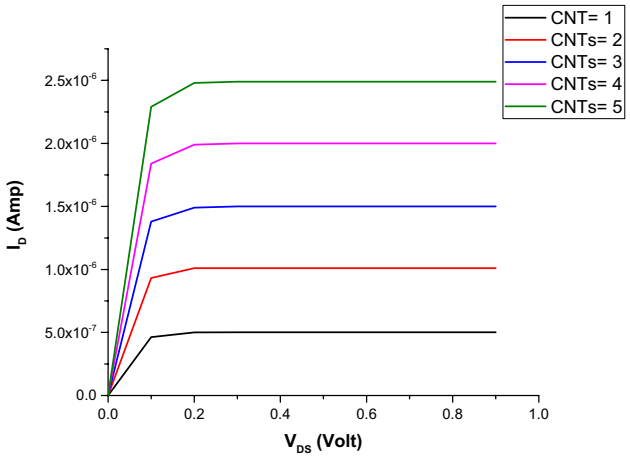


Fig. 8 I_D versus V_{DS} curve for single and multiple CNTs

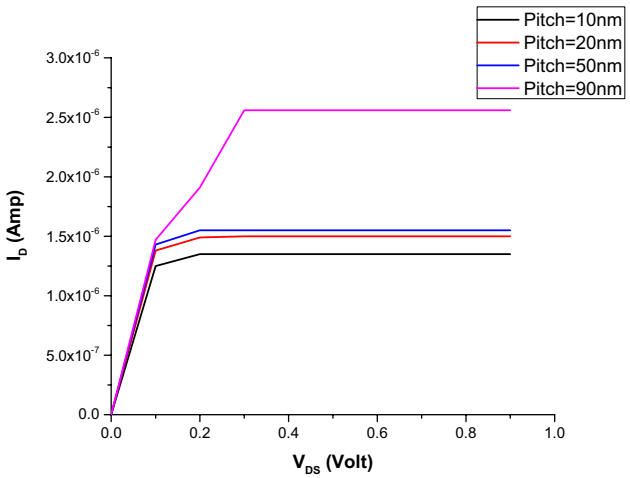


Fig. 9 I_D versus V_{DS} curve for various pitch values

1.2 Static Random-Access Memory

SRAM is one of the essential building blocks of digital very large scale integrated (VLSI) circuits and it occupies 90% of total chip area. SRAMs are the most important source of static power consumption. Hence, design of SRAM cell has to be done in consideration with low power consumption, high speed, and smaller chip area. SRAM cells designed with CNTFET are being proposed for achieving low power and high speed operations [12]. The read noise margin of conventional 6T (Fig. 10) SRAM cell is reduced by using same path for both read and write operations [13]. In conventional 8T SRAM cell (Fig. 11), a separate read path is used, which increases read stability of the memory cell as compared with that of the conventional

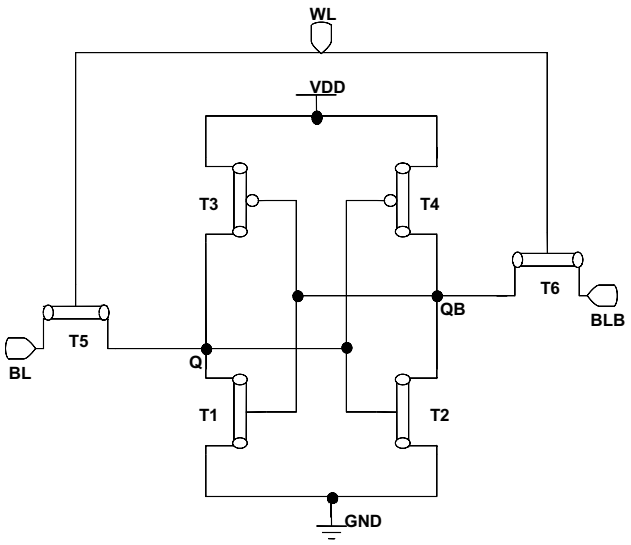


Fig. 10 6T CNTFET SRAM Cell [3]

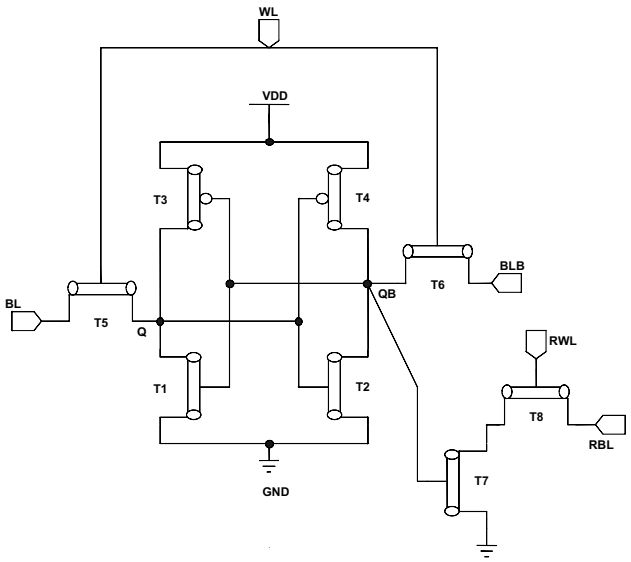


Fig. 11 Conventional 8T CNTFET SRAM cell [13]

6T SRAM cell. The conventional 8T SRAM cell consumes more power during the read operation. This is due to current leakage in the Read Bit Line (RBL) [14]. In conventional 10T SRAM cell, stacked access transistors are used to reduce the sub-threshold leakage in bit lines. The differential read method improves the Read static Noise Margin (RSNM) and decreases the radiation effect on the storage nodes [15]. Fine grained bit line stacking technique based 8T SRAM cell reduces read port leakage current of 8T bit-cell. The read and write power consumption of

fine-grained bit line stacking technique based 8T SRAM cell has significantly minimized by adopting the Bank-level Word Line (WL) driver power-gating method. The leakage power of an SRAM cell is reduced by using the floating write drive technique. Hence, Fine grained bit line stacking technique based 8T SRAM cell achieves 75% leakage power reduction as compared to that of conventional 8T SRAM cell [16]. The 8T SRAM cell proposed in [17] has virtual ground. This virtual ground weakens the positive feedback of the circuit which in turn increases the WSNM of the SRAM cell. This proposed cell does not require any precharging circuit for the read operation. In the proposed cell, the storage node is separated from the read path. Hence, RSNM of the circuit is also improved. The write, hold and read currents of the proposed SRAM cell are reduced and speed is increased as compared with that of conventional 6T SRAM cell[17]. The 8T SRAM cell with vertical read word line (RWL) and selective dual split power line offers better power performance than the conventional 6T SRAM cell. The dynamic power consumption of the proposed cell is drastically reduced due to vertical read word line. The vertical read word line selects only particular read bit lines during the read operation. This, in turn controls the charging and discharging of selected bit lines. Hence, the dynamic power consumption of the proposed cell is reduced during the read operation. The proposed memory cell noise margin is also improved by the dual split power line technique [18]. The 6T and transmission gate based 8T SRAM cells are constructed using Heterojunction Tunnel Field Effect Transistor (HETT) which dissipates less power compared to that of MOS transistors. HETT based SRAM cells also offer high speed operations [19]. The Schmitt trigger based 8T SRAM proposed is a modified version of conventional 6T SRAM cell. A high threshold voltage (V_{th}) NMOS transistor is added in the pull-down network of the conventional 6T SRAM cell which gives the structure of the Schmitt trigger based 8T SRAM cell [18]. The presence of high V_{th} NMOS transistor reduces the leakage power consumption of the proposed SRAM cell [18]. A single ended TG based 8-transistor (8T) SRAM cell has feedback cutting facilities, which reduces the disturbances during the reading condition. Hence the SNM of the circuit is increased. The power and delay performances of the circuit are very good as compared with that of conventional SRAM cells [20]. The 2-read/write 8T dual-port SRAM cell consumes less dynamic power. It has an additional circuit named as world line pulse adjusting circuit which adjusts the pulse width of the word line for both read and writes operations. The bit line discharging power is reduced by shortening the width of the word line during different row access. The 2-read/write 8T dual-port SRAM cell reduces the read power by 7% and write power by 18% [21].

2 Structure and Operation of Proposed NCNTFET Darlington 8T SRAM Cell

The circuit diagram of the proposed NCNTFET Darlington 8T SRAM cell is shown in Fig. 12. It is a modified structure of the conventional 6T CNTFET SRAM cell. Two NCNTFETs (N5 and N6) are connected in Darlington fashion in the pull-down network of the conventional 6T CNTFET SRAM cell gives the structure of the proposed NCNTFET Darlington 8T SRAM cell. The CNTFETs N1, N2, P1, P2, N5, and N6 form the storage cell of the proposed structure. The CNTFETs N3 and N4 act as access transistors. These access transistors are controlled by the word line. It has storage nodes Q and QB. The bit lines BL and BLB are used as a path for write and read operations. The presence of Darlington NCNTFETs in the pull-down network of the conventional 6T CNTFET SRAM cell improves the power performance of the memory cell during the write, hold, and read conditions. The power consumption of the proposed NCNTFET Darlington 8T SRAM cell is very less as compared with that of conventional 6T and 8T CNTFET SRAM cells.

2.1 Write Operation

For write a bit in the storage cell, the corresponding bit and its complement values are placed on BL and BLB respectively. WL is raised high; the access transistors are enabled. Hence BL value is stored in Q and BLB value stored in QB. Figure 13 illustrates the write operation of '1′ in the proposed cell. The conditions for write are BL = 1, BLB = 0, and WL = 1. The WL

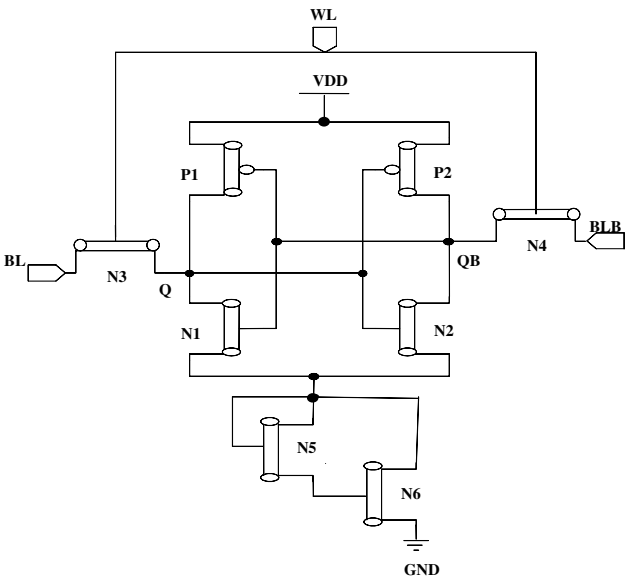


Fig. 12 Proposed NCNTFET Darlington 8T SRAM Cell

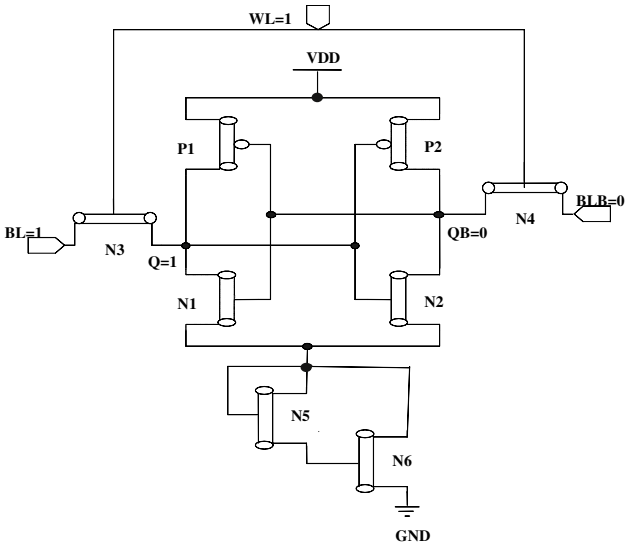


Fig. 13 Proposed NCNTFET Darlington 8T SRAM Cell during write '1'

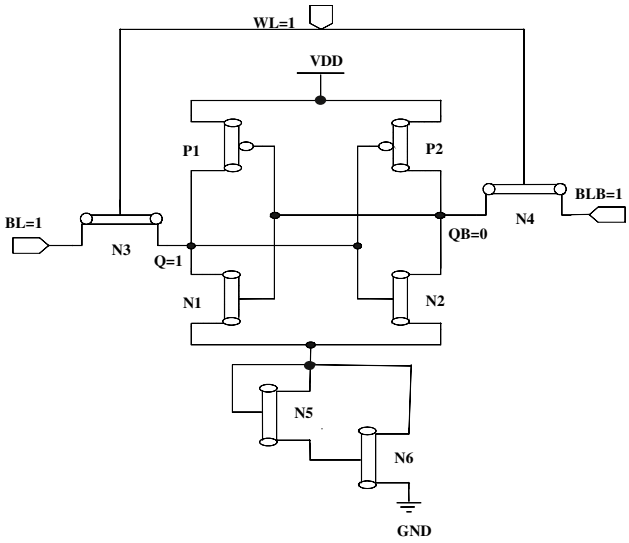


Fig.14 Proposed NCNTFET Darlington 8T SRAM cell during read '1'

is raised; this in turn enables the access transistors. Hence the BL and BLB values are transferred to Q and QB respectively. The storage node Q is raised high. Hence N2 is enabled and P2 is disabled. Due to that QB gets discharged to ground potential. Hence P1 is enabled and N1 is disabled. The 'ON' condition of P1 connects the storage node Q with supply voltage (VDD). This shows the bit '1' store in Q and bit '0' in QB.

2.2 Read Operation

The structure of the proposed NCNTFET Darlington 8T SRAM cell for the read operation is shown in Fig. 14. Before read operation, the WL has to be kept low for some time, simultaneously the bit lines are pre-charged up to VDD. After pre-charging, the WL is raised high. Hence, the access transistors N3 and N4 are turned 'ON'. As shown in Fig. 12, during the conditions Q = 1 and QB = 0, N1 is 'OFF' and N2, N4, N5 and N6 are in 'ON' condition. Hence, the BLB gets a discharging path through all these 'ON' transistors. Meanwhile, the BL maintains its potential as that of VDD. The potential difference between the BL and BLB is sensed by the sense amplifier and the resultant stored value is produced at the output of the sense amplifier.

2.3 Hold Operation

The hold mode of the SRAM cell is also called standby mode. During hold operation WL = 0. Hence the access transistors N3 and N4 are switched off. Therefore, neither writing nor reading is possible. The storage nodes hold the bit values stored in the previous clock cycle. In Fig. 15, the hold operation is shown.

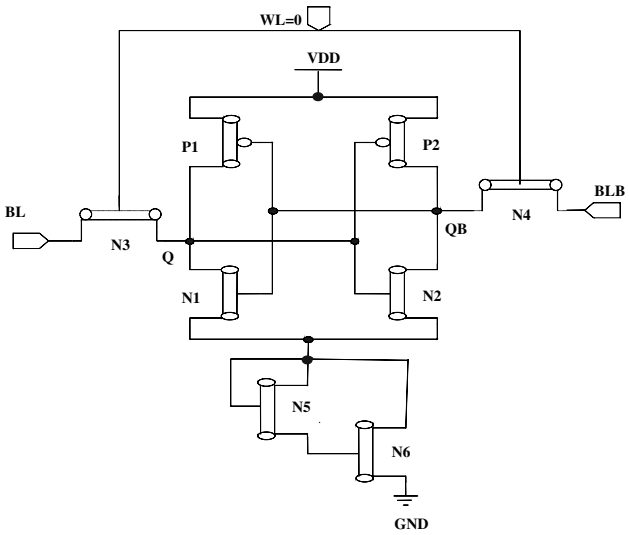


Fig. 15 Proposed NCNTFET Darlington 8T SRAM cell during hold operation

3 Results and Power Analysis

A Darlington pair of NCNTFETs are connected in the pull-down network of the conventional 6T SRAM cell gives the structure of proposed NCNTFET Darlington 8T SRAM cell. The Darlington pair is offering high input impedance. The presence of high impedance Darlington pair in series with the pull-down network reduces the leakage current flow through it. Hence the power performance of the proposed NCNTFET Darlington 8T SRAM Cell is improved as compared to that of conventional 6T and 8T SRAM cells. The power comparison of SRAM cells is summarised in Table 2.

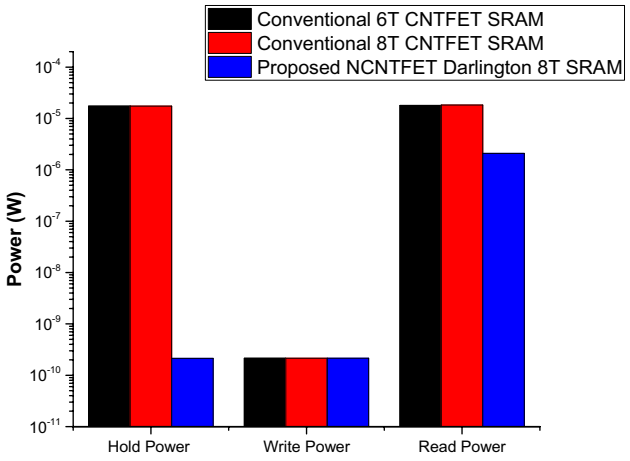


Fig. 16 Power comparison of SRAMs cells

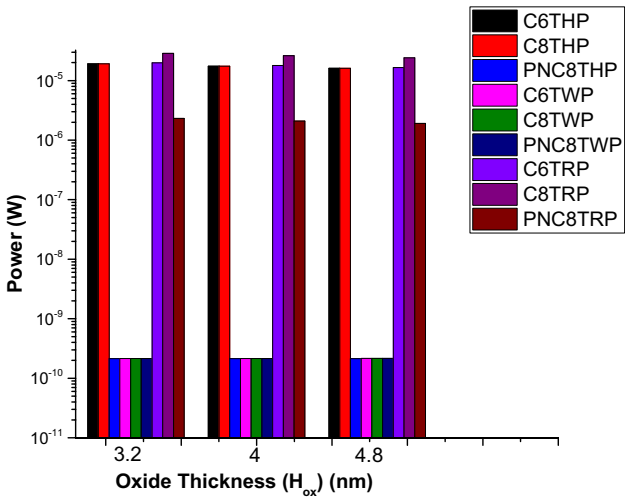


Fig. 17 Power comparisons of SRAMs under oxide thicknesses variation

The hold condition power consumption of conventional 6T and 8T CNTFET SRAM cells are 1.7469×10^{-5} W but it is found to be 2.1366×10^{-10} W for the proposed NCNTFET Darlington 8T SRAM Cell. The hold condition power performance of the proposed NCNTFET Darlington 8T SRAM Cell is nearly 100% improved as Compared to that of Conventional 6T and 8T CNTFET SRAM cells. During the read operation, the power consumption of conventional 6T CNTFET SRAM and 8T CNTFET SRAM cells is 1.7985×10^{-05} W and 1.8279×10^{-5} W respectively. The read power performance of the proposed NCNTFET Darlington 8T SRAM Cell is improved by 87.18% and 88.57% than conventional 6T CNTFET SRAM and 8T CNTFET SRAM cells respectively. Figure 16 shows the power comparison of conventional 6T, 8T, and proposed SRAM cell. The device

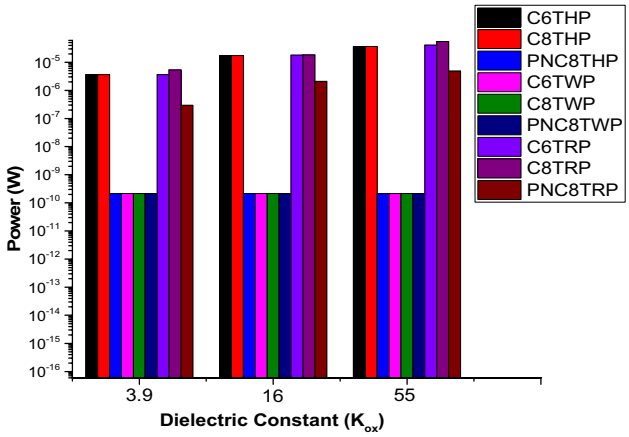


Fig. 18 Power comparisons of SRAMs under dielectric constant variation

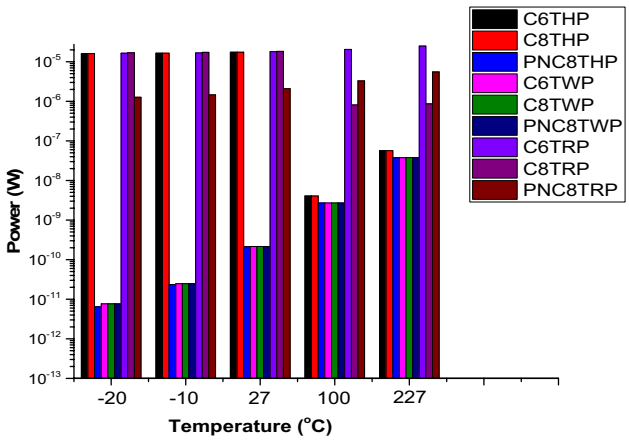


Fig. 19 Power comparisons of SRAMs under temperature variation

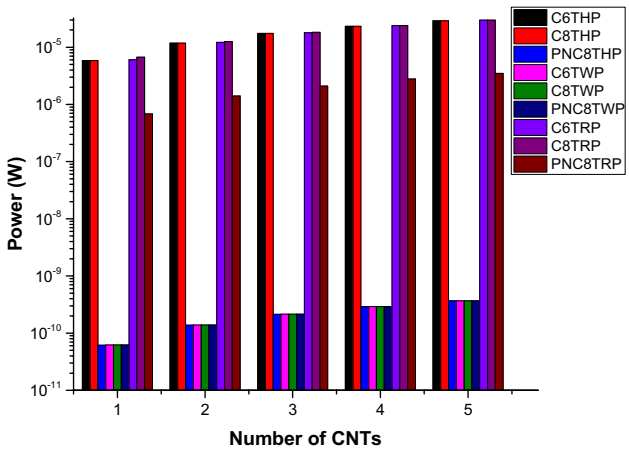


Fig. 20 Power comparisons of SRAMs for single and multiple CNTs

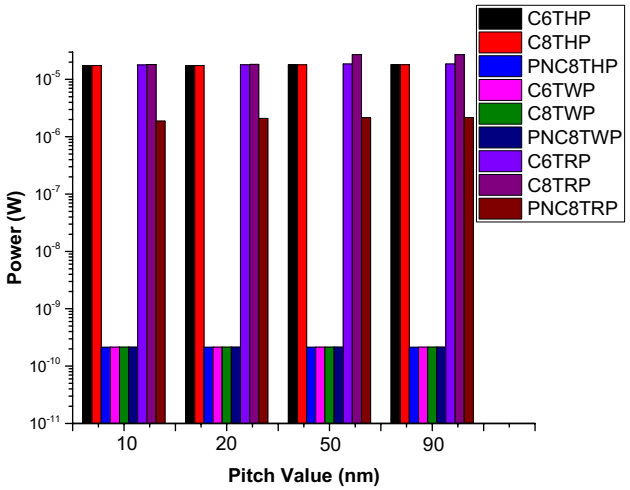


Fig. 21 Power comparisons of SRAMs under pitch value variation

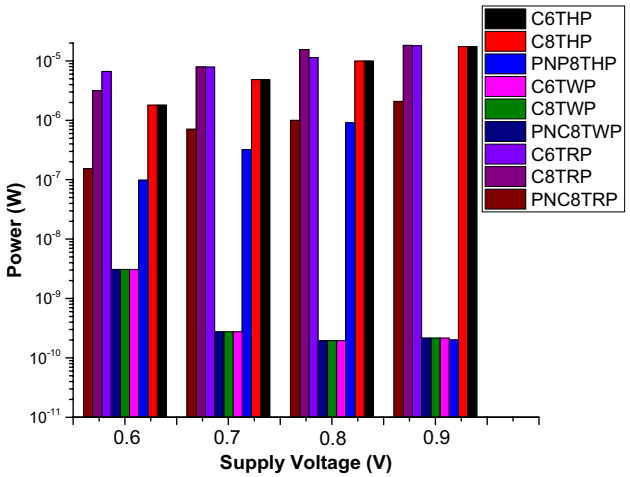


Fig. 22 Power comparisons of SRAMs under supply voltage variation

Table 1 Device parameters and process assumptions for simulations

Sl. no.	Parameters	Value
1	Oxide thickness (Tox)	4 nm
2	Gate constant dielectric (Kox)	HfO2 (16)
3	CNT pitch	20 nm
4	Power supply	0.9 V
5	Temperature	27 °C
6	Gate/source/drain length (CNT)	32 nm
7	Number of CNTs	3

parameters for nominal values and process assumptions for simulations are listed in Table 1

The nominal values of chiral vectors are m = 19 and n = 0. Rather than choosing the same chiral values for all the CNTFETs, the dual chiral value concept is applied. Dual chiral values can be applied in two ways. Case 1: NCNTFET with m = 19, n = 0 and PCNTFET with m = 16, n = 0 and Case 2: PCNTFET with m = 19, n = 0 and NCNTFET with m = 16, n = 0. The simulation result shows that the power consumption of all the memory cells during dual chiral values is lesser as compared with that of nominal value power consumption [2]. The Table 3 gives the complete power report for single and multiple chiral vectors.

The gate oxide thickness (Hox) of CNTFET is varied by ± 20% from the nominal value (4 nm). The power performance of the SRAM cells is investigated for the variation of gate oxide thickness during the write, hold, and read conditions. It is noted that the power consumption of the memory cell is inversely proportional to gate oxide thickness. Increasing gate oxide thickness increases the threshold voltage of the CNTFET and reduces the charge leakage from the channel to the gate. Hence, the power consumption of conventional 6T, 8T, and proposed Darlington SRAM cell are decreased while increasing the gate oxide thickness. The Power comparisons of various SRAMs under oxide thickness variation are provided in Table 4.

Gate oxide dielectric constant of CNTFET is varied from 3.9 to 55 and the power performances of the SRAM cells are observed. The dielectric constant of SiO_2 is 3.9, HfO_2 is 16, and TiO_2 is 55. The write, hold, and read power consumption of conventional 6T, 8T, and proposed Darlington SRAM cells are calculated for these materials. The gate oxide dielectric constant of CNTFET is directly proportional to the channel current conduction of CNTFET. Hence, increasing dielectric constant increases the power consumption of the memory cell. The Power comparisons of various SRAMs under dielectric constant variation are summarised in Table 5.

Temperature of CNTFET is varied from room temperature (27 °C) to − 20 °C, − 10 °C, 100 °C, and 227 °C. The corresponding power consumption variation of conventional 6T, 8T, and proposed Darlington SRAM cell are noted. Increase in temperature of CNTFET generates thermal charges in the CNTFET channel. Hence, the increase in temperature increases the current conduction of CNTFET. This increases the power consumption of the SRAM cells. The power consumption of SRAM cells is positively proportional to the temperature. The Power comparisons of various SRAMs under temperature variation are tabulated in Table 6.

Table 2 Power comparisons of SRAM cells

Power (W)	Conventional 6T CNTFET SRAM [3]	Conventional 8T CNTFET SRAM [13]	Proposed NCNTFET Darlington 8T SRAM cell	% of improvement (compared to conventional 6T CNTFET SRAM [3])	% of improvement (compared to conventional 8T CNTFET SRAM [13])
Hold static power	1.7469×10^{-5}	1.7469×10^{-5}	2.1366×10^{-10}	100.00	100.00
Write static power	2.1503×10^{-10}	2.1493×10^{-10}	2.1493×10^{-10}	0.00	0.00
Read static power	1.7985×10^{-5}	1.8279×10^{-5}	2.0891×10^{-6}	87.18	88.57

The power consumption of conventional 6T, 8T, and proposed Darlington SRAM cell are calculated for single and multiple (2, 3, 4, and 5) CNTs during the write, hold and read modes of operations. Increase in number of CNTs increases the amount of current flow in the CNTFET channel. This, in turn increases the power consumption of memory cell. Hence, the power consumption of conventional 6T, 8T, and proposed Darlington SRAM cell is directly proportional to the number of CNTs present in the CNTFET. The Power comparisons of various SRAMs during single and multiple nano tubes are provided in Table 7.

Table 3 Power comparison of SRAMs for nominal and dual chiral values

Chiral vector	Conventional 6T CNTFET SRAM [3]	Conventional 8T CNTFET SRAM [13]	Proposed NCNTFET Darlington 8T SRAM Cell
Hold power (W)			
Nominal chiral value	1.7469×10^{-5}	1.7469×10^{-5}	2.1366×10^{-10}
Dual chiral value			
Case1	2.2931×10^{-10}	2.2931×10^{-10}	1.1352×10^{-10}
Case2	1.2916×10^{-10}	1.2918×10^{-10}	1.1330×10^{-10}
Write power (W)			
Nominal chiral value	2.1493×10^{-10}	2.1493×10^{-10}	2.1493×10^{-10}
Dual chiral value			
Case1	1.1478×10^{-10}	1.1442×10^{-10}	1.1477×10^{-10}
Case2	1.1474×10^{-10}	1.1437×10^{-10}	1.1475×10^{-10}
Read power (W)			
Nominal chiral value	1.7985×10^{-5}	1.8279×10^{-5}	2.0891×10^{-6}
Dual chiral value			
Case1	1.3294×10^{-5}	8.1023×10^{-7}	1.3562×10^{-6}
Case2	1.2048×10^{-5}	8.1013×10^{-7}	6.7637×10^{-7}

The axial distance between two adjacent CNTs is called the pitch value of CNTFET. The nominal pitch value is found to be 20 nm. Here, the power consumption of CNTFET is calculated for pitch values such as 10 nm, 50 nm, and 90 nm. The power consumption of conventional 6T, 8T, and proposed Darlington SRAM cell are calculated for those corresponding pitch values. Increasing pitch value increases the power consumption of the SRAM cells. The Power comparisons of various SRAMs under pitch value variation are tabulated in Table 8.

The nominal supply voltage for 32 nm technology is 0.9 V. The proposed Darlington SRAM cells have not achieved the required functionality when the supply voltage is less than 0.6 V. Hence the supply voltage is varied from 0.9 to 0.6 V. The power consumption of conventional 6T, 8T, and proposed Darlington SRAM cell are noted for write, hold, and read conditions. From the simulation results, it can be seen that the power consumption of the SRAM cell is directly proportional to the supply voltage. Thus, decreasing the supply voltage decreases the power consumption of SRAM cells. The Power consumption comparisons of various SRAMs under supply voltage variation are provided in Table 9. Figures 17, 18, 19, 20, 21, 22 show the power comparison of 6T, 8T and proposed SRAM cells for the varation of CNTFET parameters

4 Static Noise Margin Analysis

The static noise margin (SNM) is one of the important performance metrics of a memory cell. The stability of a memory cell is measured based on SNM of the cell. Maximum tolerance of SRAM cells against DC noise voltage is defined as the static noise margin of the SRAM cell. For evaluating SNM, the voltage transfer characteristics (VTCs) of memory cell storage nodes Q and QB are noted. A butterfly diagram is drawn from VTCs. SNM of a memory cell is equal to the largest diameter of the square that can be fixed in the

Table 4 Power comparisons of SRAMs under oxide thicknesses variation

Oxide thickness (m) Hox	Conventional 6T CNTFET SRAM [3]	Conventional 8T CNTFET SRAM [13]	Proposed NCNTFET Darlington 8T SRAM cell
Hold power (W)			
3.2×10^{-9}	1.9142×10^{-5}	1.9142×10^{-5}	2.1359×10^{-10}
4×10^{-9}	1.7469×10^{-5}	1.7469×10^{-5}	2.1366×10^{-10}
4.8×10^{-9}	1.6147×10^{-5}	1.6147×10^{-5}	2.1370×10^{-10}
Write power (W)			
3.2×10^{-9}	2.1484×10^{-10}	2.1484×10^{-10}	2.1484×10^{-10}
4×10^{-9}	2.1493×10^{-10}	2.1493×10^{-10}	2.1493×10^{-10}
4.8×10^{-9}	2.1500×10^{-10}	2.1500×10^{-10}	2.1500×10^{-10}
Read power (W)			
3.2×10^{-9}	1.9834×10^{-5}	2.8684×10^{-5}	2.3144×10^{-6}
4×10^{-9}	1.7985×10^{-5}	1.8279×10^{-5}	2.0891×10^{-6}
4.8×10^{-9}	1.6543×10^{-5}	2.4190×10^{-5}	1.9121×10^{-6}

Here C6THP-Hold power of conventional 6T CNTFET SRAM cell, C8THP-Hold power of conventional 8T CNTFET SRAM cell, PNC8THP-Hold power of proposed NCNTFET 8T SRAM cell, C6TWP-Write power of conventional 6T CNTFET SRAM cell, C8TWP-Write power of conventional 8T CNTFET SRAM cell, PNC8TWP-Write power of proposed NCNTFET 8T SRAM cell, C6TRP-Read power of conventional 6T CNTFET SRAM cell, C8TRP-Read power of conventional 8T CNTFET SRAM cell and PNC8TRP-Read power of proposed NCNTFET 8T SRAM cell

Table 5 Power comparisons of SRAMs under dielectric constant variation

Dielectric constant (Kox)	Conventional 6T CNTFET SRAM [3]	Conventional 8T CNTFET SRAM [13]	Proposed NCNTFET Darlington 8T SRAM cell
Hold power (W)			
3.9	3.6414×10^{-6}	3.6414×10^{-6}	2.1396×10^{-10}
16	1.7469×10^{-5}	1.7469×10^{-5}	2.1366×10^{-10}
55	3.6645×10^{-5}	3.6645×10^{-5}	2.1293×10^{-10}
Write power (W)			
3.9	2.1560×10^{-10}	2.1530×10^{-10}	2.1529×10^{-10}
16	2.1493×10^{-10}	2.1493×10^{-10}	2.1493×10^{-10}
55	2.1387×10^{-10}	2.1387×10^{-10}	2.1387×10^{-10}
Read power (W)			
3.9	3.6421×10^{-6}	5.3705×10^{-6}	2.9435×10^{-7}
16	1.7985×10^{-5}	1.8279×10^{-5}	2.0891×10^{-6}
55	4.0784×10^{-5}	5.4946×10^{-5}	4.8864×10^{-6}

Table 6 Power comparisons of SRAMs under temperature variation

Temperature (°C)	Conventional 6T CNTFET SRAM [3]	Conventional 8T CNTFET SRAM [13]	Proposed NCNTFET Darlington 8T SRAM cell
Hold power (W)			
− 20	1.6088×10^{-5}	1.6088×10^{-5}	6.4467×10^{-12}
− 10	1.6385×10^{-5}	1.6385×10^{-5}	2.3459×10^{-11}
27	1.7469×10^{-5}	1.7469×10^{-5}	2.1366×10^{-10}
100	4.0653×10^{-5}	4.0653×10^{-5}	2.7029×10^{-9}
227	5.6884×10^{-5}	5.6884×10^{-5}	3.7795×10^{-8}
Write power (W)			
− 20	7.6870×10^{-12}	7.6870×10^{-12}	7.6960×10^{-12}
− 10	2.4715×10^{-11}	2.4715×10^{-11}	2.4723×10^{-11}
27	2.1493×10^{-10}	2.1493×10^{-10}	2.1493×10^{-10}
100	2.7042×10^{-9}	2.7042×10^{-9}	2.7036×10^{-9}
227	3.7804×10^{-8}	3.7804×10^{-8}	3.7713×10^{-8}
Read power (W)			
− 20	1.6370×10^{-5}	1.6898×10^{-5}	1.2682×10^{-6}
− 10	1.6713×10^{-5}	1.7195×10^{-5}	1.4596×10^{-6}
27	1.7985×10^{-5}	1.8279×10^{-5}	2.0891×10^{-6}
100	2.0530×10^{-5}	2.1406×10^{-5}	3.2752×10^{-6}
227	2.4977×10^{-5}	2.6688×10^{-5}	5.5134×10^{-6}

Table 7 Power comparisons of SRAMs for single and multiple CNTs

Number of CNTs	Conventional 6T CNTFET SRAM [3]	Conventional 8T CNTFET SRAM [13]	Proposed NCNTFET Darlington 8T SRAM cell
Hold power (W)			
1	5.8615×10^{-6}	5.8615×10^{-6}	6.1509×10^{-11}
2	1.1773×10^{-5}	1.1773×10^{-5}	1.3815×10^{-10}
3	1.7469×10^{-5}	1.7469×10^{-5}	2.1366×10^{-10}
4	2.3215×10^{-5}	2.3215×10^{-5}	2.9035×10^{-10}
5	2.8962×10^{-5}	2.8962×10^{-5}	3.6694×10^{-10}
Write power (W)			
1	6.2216×10^{-11}	6.2216×10^{-11}	6.2214×10^{-11}
2	1.3885×10^{-10}	1.3885×10^{-10}	1.3884×10^{-10}
3	2.1493×10^{-10}	2.1493×10^{-10}	2.1493×10^{-10}
4	2.9157×10^{-10}	2.9157×10^{-10}	2.9156×10^{-10}
5	3.6820×10^{-10}	3.6820×10^{-10}	3.6819×10^{-10}
Read power (W)			
1	6.0396×10^{-6}	6.6715×10^{-6}	6.8327×10^{-7}
2	1.2127×10^{-5}	1.2583×10^{-5}	1.4027×10^{-6}
3	1.7985×10^{-5}	1.8279×10^{-5}	2.0891×10^{-6}
4	2.3892×10^{-5}	2.4025×10^{-5}	2.7879×10^{-6}
5	2.9798×10^{-5}	2.9772×10^{-5}	3.4868×10^{-6}

Table 8 Power comparisons of SRAMs under pitch value variation

Pitch value (nm)	Conventional 6T CNTFET SRAM [3]	Conventional 8T CNTFET SRAM [13]	Proposed NCNTFET Darlington 8T SRAM cell
Hold power (W)			
10	1.7419×10^{-5}	1.7419×10^{-5}	2.1372×10^{-10}
20	1.7469×10^{-5}	1.7469×10^{-5}	2.1366×10^{-10}
50	1.8012×10^{-5}	1.8012×10^{-5}	2.1363×10^{-10}
90	1.8087×10^{-5}	1.8087×10^{-5}	2.1363×10^{-10}
Write power (W)			
10	2.1463×10^{-10}	2.1463×10^{-10}	2.1501×10^{-10}
20	2.1493×10^{-10}	2.1493×10^{-10}	2.1493×10^{-10}
50	2.1490×10^{-10}	2.1490×10^{-10}	2.1490×10^{-10}
90	2.1490×10^{-10}	2.1490×10^{-10}	2.1490×10^{-10}
Read power (W)			
10	1.7915×10^{-5}	1.8259×10^{-5}	1.8807×10^{-6}
20	1.7985×10^{-5}	1.8279×10^{-5}	2.0891×10^{-6}
50	1.8582×10^{-5}	2.6989×10^{-5}	2.1620×10^{-6}
90	1.8665×10^{-5}	2.710×10^{-5}	2.1682×10^{-6}

Table 9 Power comparisons of SRAMs under supply voltage variation

Supply voltage (V) VDD	Conventional 6T CNTFET SRAM [3]	Conventional 8T CNTFET SRAM [13]	Proposed NCNTFET Darlington 8T SRAM cell
Hold power (W)			
0.9	1.7469×10^{-5}	1.7469×10^{-5}	2.1366×10^{-10}
0.8	9.9607×10^{-6}	9.9606×10^{-6}	1.9102×10^{-10}
0.7	4.8276×10^{-6}	4.8275×10^{-6}	1.6804×10^{-10}
0.6	1.8010×10^{-6}	1.8009×10^{-6}	1.4474×10^{-10}
Write power (W)			
0.9	2.1493×10^{-10}	2.1493×10^{-10}	2.1493×10^{-10}
0.8	1.9495×10^{-10}	1.9495×10^{-10}	1.9495×10^{-10}
0.7	2.7430×10^{-10}	$2.743\times10–^{10}$	2.7431×10^{-10}
0.6	3.0873×10^{-9}	3.0873×10^{-9}	3.0874×10^{-9}
Read power (W)			
0.9	1.7985×10^{-5}	1.8279×10^{-5}	2.0891×10^{-6}
0.8	1.1419×10^{-5}	1.5561×10^{-5}	9.9777×10^{-7}
0.7	7.8489×10^{-6}	7.9309×10^{-6}	7.0998×10^{-7}
0.6	6.6664×10^{-6}	3.1519×10^{-6}	1.5399×10^{-7}

butterfly diagram [7]. The proposed NCNTFET Darlington 8T SRAM cell is offering high write SNM than the conventional 6T and 8T CNTFET SRAM cells. The WSNM of conventional 6T and 8T CNTFET SRAM cells is 240 mV. The proposed NCNTFET Darlington 8T SRAM offers 410 mV WSNM. Hence the WSNM of proposed NCNTFET Darlington 8T cell is increased by 70.83% than both conventional 6T and 8T CNTFET SRAM cells. Due to the presence of Darlington pair CNTFETs the hold and read modes noise

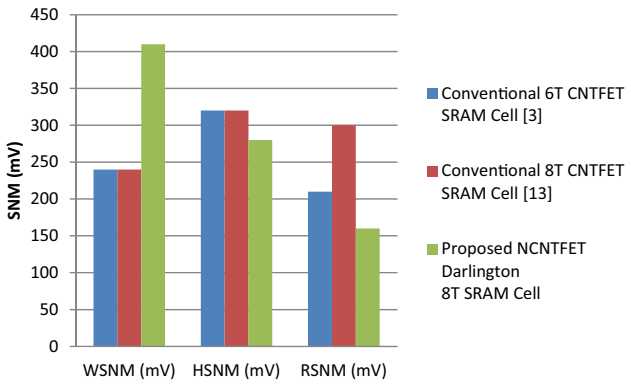


Fig. 23 SNM comparison of various SRAM cells

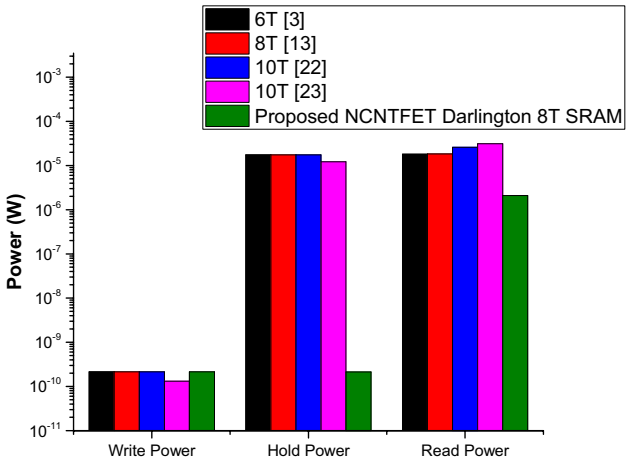
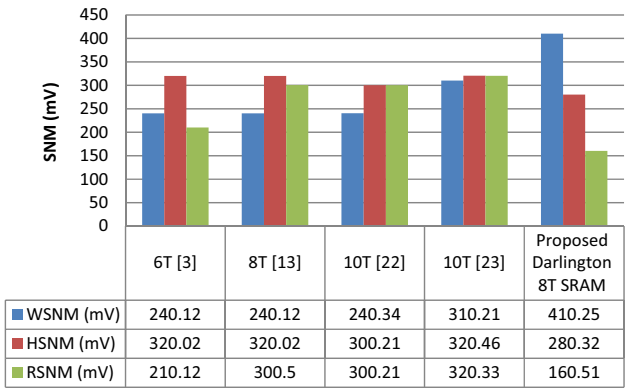


Fig. 24 Power comparison among various CNTFET SRAM cells



	6T [3]	8T [13]	10T [22]	10T [23]	Proposed Darlington 8T SRAM
WSNM (mV)	240.12	240.12	240.34	310.21	410.25
HSNM (mV)	320.02	320.02	300.21	320.46	280.32
RSNM (mV)	210.12	300.5	300.21	320.33	160.51

Fig. 25 SNM comparison among various CNTFET SRAM cells

margins of the proposed cell reduced lesser than conventional 6T and 8T cells. Figure 23 shows the SNM comparison of conventional 6T, 8T, and proposed SRAM cell.

5 Comparison of Various CNTFET SRAM Cells

The simulation results shows that the hold power consumption of proposed 8T cell is 99.99% lower when compared with that of conventional 6T [3], 8T [13], 10T [22] and 10T [23] cells. The read power consumption of proposed 8T cell is 88.38%, 88.57%, 91.96% and 93.29% lower when compared with that of conventional 6T [3], 8T [13], 10T [22] and 10T [23] cells, respectively. The proposed 8T cell also achieves write SNM of 1.7, 1.7, 1.7, and 1.32 times higher compared to 6T [3], 8T [13], 10T [22] and 10T [23] cells, respectively. Figures 24 and 25 shows the power and SNM comparison of various CNTFET SRAM cells, respectively.

6 Conclusion

The effect of CNTFET parameters on drain current and drain to source voltage is observed. The simulation results show that the CNTFET drain current and power consumption are directly proportional to dielectric constant, chiral vectors, temperature, number of CNTs in the CNTFET channel, pitch value, and supply voltage. The CNTFET drain current and power consumption are inversely proportional to gate oxide thickness. The hold condition power performance of the proposed NCNTFET Darlington 8T SRAM Cell is nearly 100% improved as Compared to Conventional 6T and 8T CNTFET SRAM cells. The read power performance of the proposed NCNTFET Darlington 8T SRAM Cell is improved by 87.18% and 88.57% than conventional 6T CNTFET SRAM and 8T CNTFET SRAM cells respectively. The WSNM proposed NCNTFET Darlington 8T cell are increased by 70.83% than both conventional 6T and 8T CNTFET SRAM cells.

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