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REGULAR PAPER

Lanthanum Doped Zirconium Oxide ($LaZrO_2$) High-k Gate Dielectric FinFET SRAM Cell Optimization

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Abstract
Inherent variations and the challenge of leakage current control in today's silicon-on-insulator metal–oxide–semiconductor field-effect transistor limits the scaling of static random-access memory. The fin-shaped field-effect transistor has been considered an attractive device for designing low power SRAM cells. In this work, a 14 nm gate length FinFET device has been designed with lanthanum doped zirconium oxide as a compound gate dielectric material. The diminished subthreshold swing (60 mV/dec), reduced leakage current (10^{-14}), lowered drain induced barrier lowering (10.6 mV/V), enhanced drive current (3.74×10^{-5}), and increased g_m (2.27×10^{-4}) were observed after simulating this optimized device. Further, two SRAM cells based on the improved device were implemented with different fin configurations. The stability parameters were investigated with the butterfly curve method. The SRAM Cell-I has presented better read static noise margin and write static noise margin in comparison to the SRAM Cell-II. The impact of supply voltage variations on stability metrics and leakage power has also been presented.

Keywords SRAM · FinFET · RSNM · Dielectric · Drain induced barrier lowering · Subthreshold swing

1 Introduction

The occurrence of short channel effects (SCE), leakage current, band to band tunneling (BTBT) and static power dissipation is due to the downscaling of planar Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) into the nanometer regime. The SOI FinFET devices are the best solution to this problem [1]. International Technology Roadmap for Semiconductors (ITRS) suggests various new materials for scaling the gate dielectric below 2 nm for preventing the high leakage current caused by the generation of direct tunneling gate leakage current [2]. Recently, several novel materials like Al_2O_3 (6 eV), HfO_2 (6 eV), La_2O_3 (5.18 eV) and ZrO_2 (5.8 eV) have come into existence in place of SiO_2 (9 eV) which have high band gap value [3–9]. It has been noticed that a gate dielectric with k over 40 is preferred, and $LaZrO_2$ has been recognized as an appropriate high-k gate dielectric material for sub-22 nm node FinFET devices [10–12].

SRAM comprises of many cell areas in the system on chip designs due to the massive requirement of transistors for a single SRAM cell array. The circuit designed with a scaled device and high-k gate dielectric material results in improved storage capacity, fast switching speed, increased efficiency of footprint and less power consumption. The use of high-k dielectrics in manufacturing has paved the way for their use in applications beyond traditional logic and memory devices. The studies of SNM for SRAM with SOI FinFETs have been contributing to technological advancement [13–19]. In this paper, performance analysis of FinFET device created with Lanthanum doped zirconium oxide ($LaZrO_2$) as a compound gate dielectric was done in Technology Computer-Aided Design (TCAD) environment.

Further, SRAM cells were made with matched size n-FinFET and p-FinFET devices. The functionality of the SRAM

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cells for reading and writing operation was investigated using timing diagrams. The SRAM cell's voltage transfer characteristic (VTC) has been demonstrated by analyzing the SRAM read and write operations. The static noise margin (SNM) SRAM read mode and SRAM write mode were evaluated with the butterfly curve method. The impact of supply voltage fluctuations on circuit performance has also been analyzed.

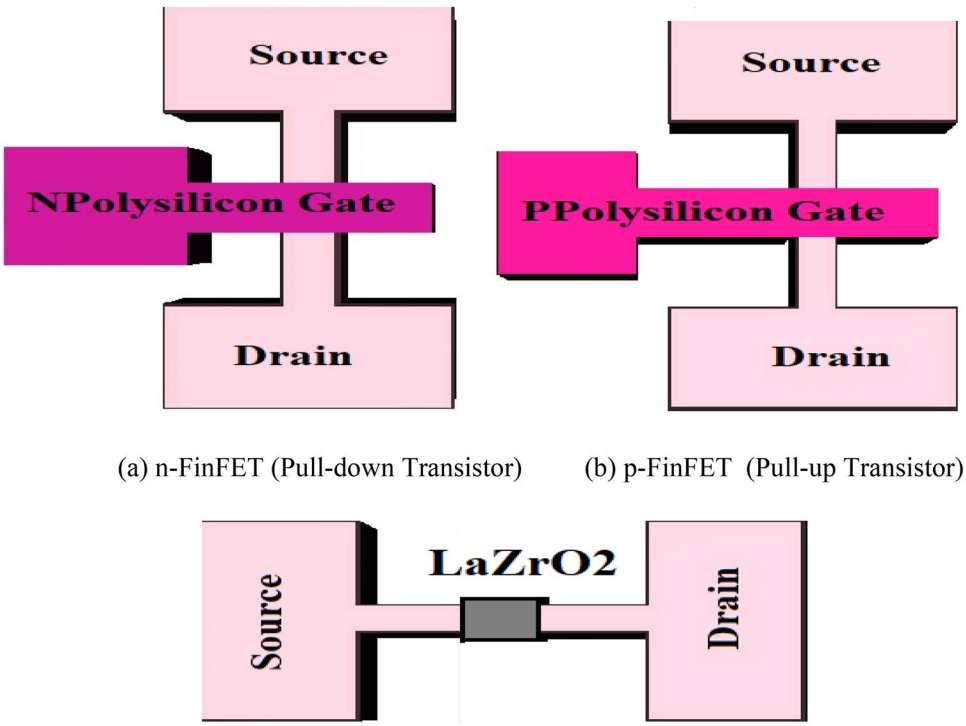
This work has been organized into multiple sections, Sect. 2 discusses the FinFET device and SRAM cell design and simulation methodology. Section 3 illustrates the results of the device, discussions and their circuit using different operating modes and stability parameters. The impact of supply voltage variations on Stability parameters and leakage power is also discussed in this section. The last section summarizes the conclusion of the research work.

2 Design and Simulation Methodology

Nanoscale FinFET device simulations are accomplished in the TCAD simulator. It was noticed that a gate dielectric with k over 40 is preferred and $LaZrO_2$ has been recognized as an appropriate high-k gate dielectric materials for sub-22 nm node FinFET devices [12, 20–22]. The novel high-k gate dielectric material is chemically stable in contact with Silicon and has high crystallization temperature, high dielectric constant (k=40) and wide energy band gaps (~ 6 eV) as compared to SiO_2. The high-k gate dielectric material has been deposited on an active silicon channel by Atomic Layer Deposition and Chemical Vapor Deposition method at high temperature [11, 12, 23, 24]. The 3D structure of n-FinFET and p-FinFET devices with matched size, as outlined in Fig. 1, was used for devising the 6T SRAM cells. The device specifications for FinFET devices according to ITRS have been summarized in Table 1 [25]. Table 2 describes important TCAD device parameters of the 14 nm processes for 6T SRAM cell circuits [21, 22, 26–29].

Table 1 FinFET parameters used in simulation (as per ITRS [25])

Device parameters	Simulation work (n-FinFET& p-FinFET)
Gate length, L_g (nm)	14
Transistor fin height, H_{Fin} (nm)	24
Transistor fin width, W_{Fin} (nm)	8
Transistor fin pitch (nm)	40
Source/drain doping concentration (donor) for nMOS (cm^{-3})	3×10^{20}
p-type substrate doping concentration (cm^{-3})	1×10^{16}
Body doping concentration (cm^{-3})	1×10^{17}
Dielectric permittivity, k	40
Physical oxide thickness (nm)	1.1
Supply voltage (Volts)	0.7



(a) n-FinFET (Pull-down Transistor) (b) p-FinFET (Pull-up Transistor)

Fig. 1 Bird's-eye view of FinFET structures

Table 2 Important TCAD designing parameters for FinFET based 6 T SRAM Cell

Process parameters	Value
Design rule unit lambda (μm)	0.007
Thickness of substrate region (μm)	0.03
Height of fin (μm)	0.024
Thickness of gate oxide (μm)	0.0011
S/D doping concentration (donor) for nMOS (cm^{-3})	3×10^{20}
S/D doping concentration (acceptor) for pMOS (cm^{-3})	3×10^{20}
Supply voltage, Vdd (V)	0.7 V
Thickness of buried oxide (μm)	0.02
Thickness of poly-silicon gate (μm)	0.002
Thickness of ILD dielectric (μm)	0.008
Thickness of ILD Metal 1(μm)	0.008
Lateral characteristic length of S/D doping of nMOS (μm)	0.004
Vertical characteristic length of S/D doping of nMOS (μm)	0.003
Doping concentration in p-type substrate (cm^{-3})	1×10^{16}
Doping concentration in body (cm^{-3})	1×10^{17}

The simulated devices are designed at 300K using models such as Drift diffusion model (DDM), Lombardi Surface mobility model, Shockley Read Hall Model and Kane's Model [28]. Figure 2 illustrates the simulation procedure in Visual TCAD for devising FinFET. The simulator's validity was examined by matching its results with the published experimental data in the TCAD environment at 300 K as shown in Fig. 3 [30]. It proves that this paper's models and parameters are valid [28]. The proposed device was simulated using the following models:

1. DDM, which solves a certain set of Poisson equations as mentioned in Eq. (1).

$$\nabla \cdot \varepsilon \nabla \psi = -q\left(p - n + N_D^+ - N_A^-\right) \tag{1}$$

where ψ is the electrostatic potential of the vacuum level, n and p represent the electron and hole concentration, N_D^+ and N_A^- represent the ionized doping concentration and q is an electron charge. The lattice temperature is kept uniform throughout the Drift Diffusion model.

2. Lombardi Surface mobility model has been introduced to address carrier mobility in the inversion layer of designed device. A cumulative carrier mobility is calculated from doping based bulk mobility (μ_B), mobility degradation, scattering due to acoustic phonon (μ_{ac}) and scattering because of surface roughness (μ_{SR}) as follows:

$$\mu_S^{-1} = \mu_B^{-1} + \mu_{ac}^{-1} + \mu_{SR}^{-1} \tag{2}$$

3. Kane's Model can explain the generation of carriers through Band to band tunneling (G^{BB}) which is expressed as:

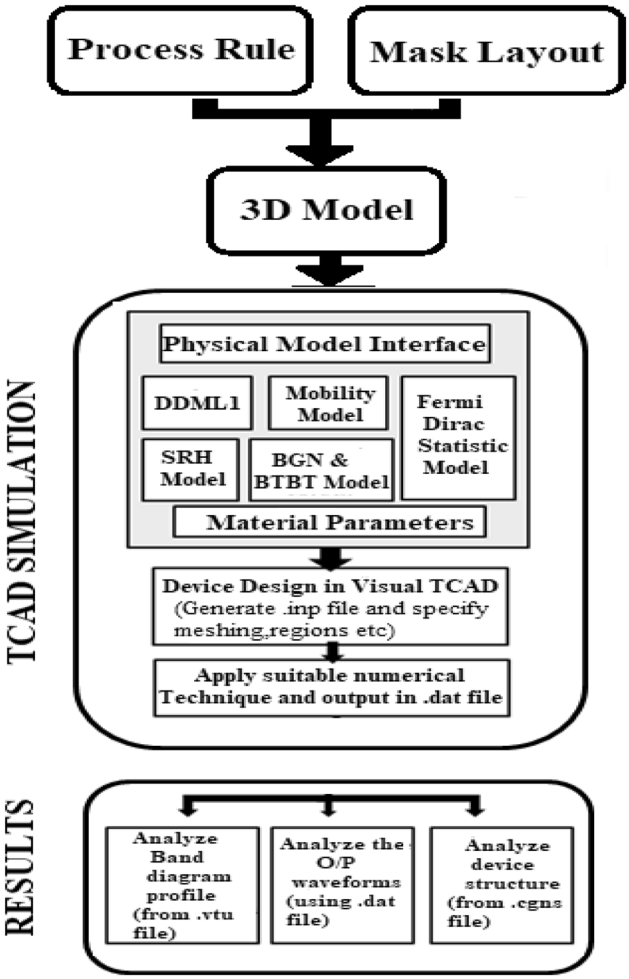


Fig. 2 Flowchart of the simulation procedure involved in Visual TCAD

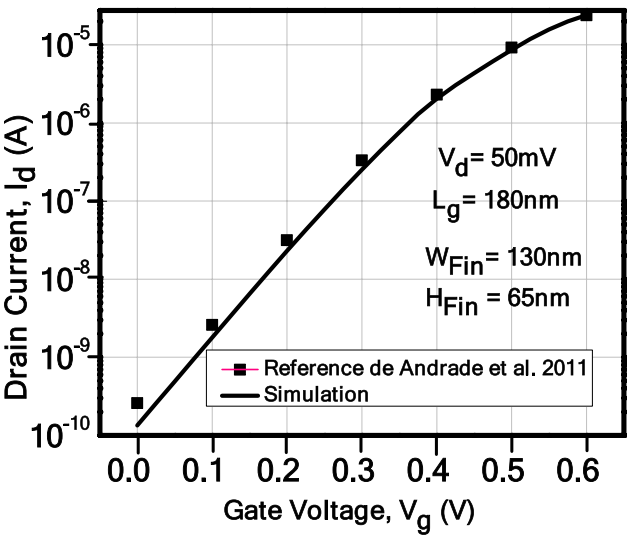


Fig. 3 I_d–V_g characteristics of FINFET with reference [30] and simulation

where E denotes electrical field magnitude, E_G represents the band-gap, A.BBT and B.BBT are experimental fitting parameters.

$$G^{BB} = A.BBT.\frac{E^2}{\sqrt{E_g}}\exp\left(-B.BBT.\frac{E_G^{\frac{3}{2}}}{E}\right) \quad (3)$$

4. The carrier recombination process is elaborated by SRH Model which is defined in Eq. (4)

$$U_{SRH} = \frac{pn - n_{ie}^2}{\tau_p\left[n + n_i e^{\frac{E_T}{KT_L}}\right] + \tau_n\left[p + n_i e^{\frac{E_T}{KT_L}}\right]} \quad (4)$$

where τ_n and τ_p are carrier lifetime which are reliant on doping concentration, n_i denotes the intrinsic carrier concentration, E_T is energy trap level, T_L is lattice temperature [22, 28].

The VI characteristics of FinFETs for input and output voltages are demonstrated in Fig. 4. It was found that both n- and p-channel FinFET devices exhibit identical characteristics for both input and output transfer characteristic curves.

3 Results and Discussions

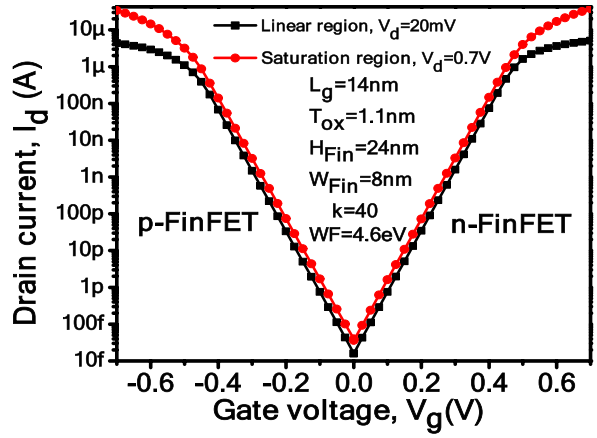
3.1 Optimized FinFET Performance

Table 3 presents the performance of matched Pull Down (PD) and Pull Up (PU) FinFET devices adopted for devising Cell-I. The performance parameters such as on-current (I_{ON}), leakage current (I_{OFF}), Subthreshold Swing (SS), Drain induced barrier lowering (DIBL) and Transconductance (g_m) are extracted from VI characteristic curves, as illustrated in Fig. 4a. These metrics have been measured for two operating regions, such as the linear and the saturation region. Both devices showed almost similar characteristics for the two operating regions.

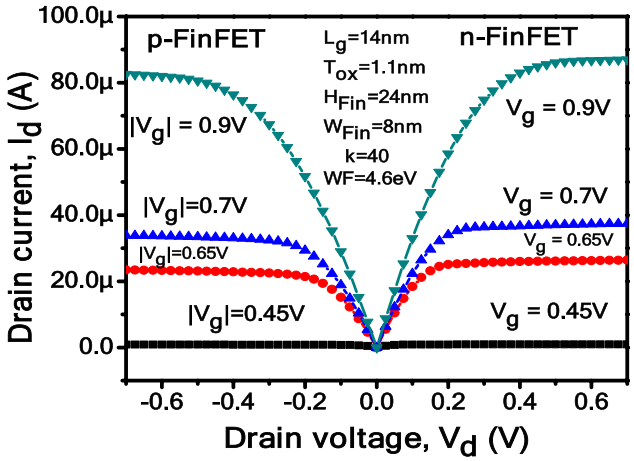
3.2 Basic Operations in 6 T SRAM Cell

6T SRAM cell can cache one-bit data using two cross-coupled inverters, and it can keep its saved data as long as power is supplied. FinFET based 6T SRAM cells containing different fin configurations in TCAD implementation are shown in Fig. 5 and Table 4. It is observed from Table 4 that Cell-II consumes more area than Cell-I.

The basic operations involved in 6T SRAM are elaborated below:



(a) Input characteristic curve



(b) Output characteristic curve

Fig. 4 VI characteristics of n-FinFET and p-FinFET devices

- *Hold operation* During this operation, the wordline (WL) is connected to the ground (Gnd). The access devices T5 and T6 are switched off and the devices T1, T2, T3, and T4 are disconnected from bitlines, as shown in Fig. 6a. The stored data bit is retained as long as the devices are cut off from the bit-lines.
- *Read Operation* WL is connected to Vdd for reading operations, and bitlines are pre-charged to Vdd. In this operation, access n-FinFET devices T5 and T6 are turned ON. Let us assume one condition: M = "1" and Mbar = "0" which causes the devices T1 and T4 to turn off and T3 and T2 are turned on. The bit-line current will flow through Bitbar-line, then passes to the ground through T6 and T2 as outlined in Fig. 6a. Therefore, the voltage at bitbar-line discharges while the energy at bit-line is maintained at Vdd, as indicated in Fig. 6b. Figure 6c outlines the read operation simulated in TCAD for FinFET based 6 T SRAM cell. The timing diagram for reading current is presented in Fig. 6d [16, 18, 31, 32].

Table 3 FinFET I–V Targets

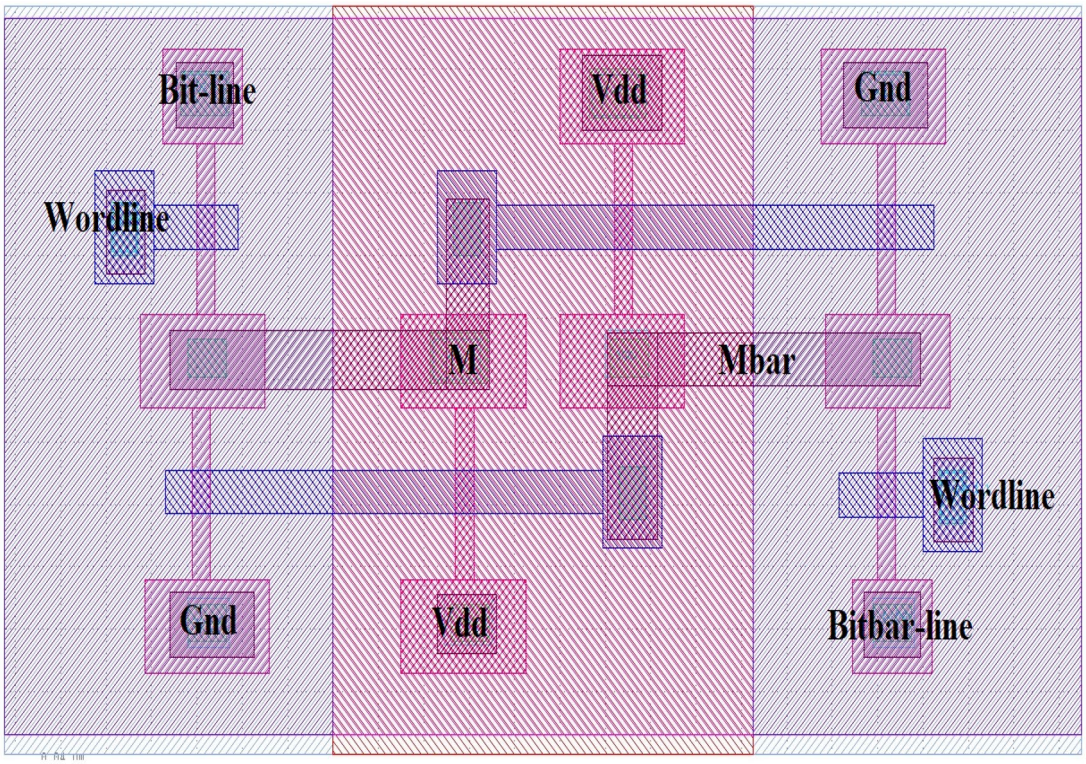
Device	Device dimensions			LIN (V_d = 50 mV, V_g = 0.7 V)				SAT (V_d = 0.7 V, V_g = 0.7 V)			
	W (nm)	L (nm)	I_{ON} (A)	I_{OFF} (A)	SS (mV/dec)	g_m (S)	I_{ON} (A)	I_{OFF} (A)	SS (mV/dec)	g_m (S)	DIBL (mV/V)
PD (N = 1)	8	14	1.22×10^{-5}	2.64×10^{-14}	59.9	5.87×10^{-5}	3.74×10^{-5}	3.59×10^{-14}	60.35	2.27×10^{-4}	10.6
PU (N = 1)	8	14	1.038×10^{-5}	2.68×10^{-14}	59.9	4.70×10^{-5}	3.38×10^{-5}	3.96×10^{-14}	61.01	2.14×10^{-4}	12.8

N = Number of fins, W = Fin width, L = Gate length, PD = Pull Down, PU = Pull Up, LIN = Linear region, SAT = Saturation region, V_g = Gate voltage, V_d = Drain voltage, SS = subthreshold swing, DIBL = Drain induced barrier lowering, g_m = Transconductance

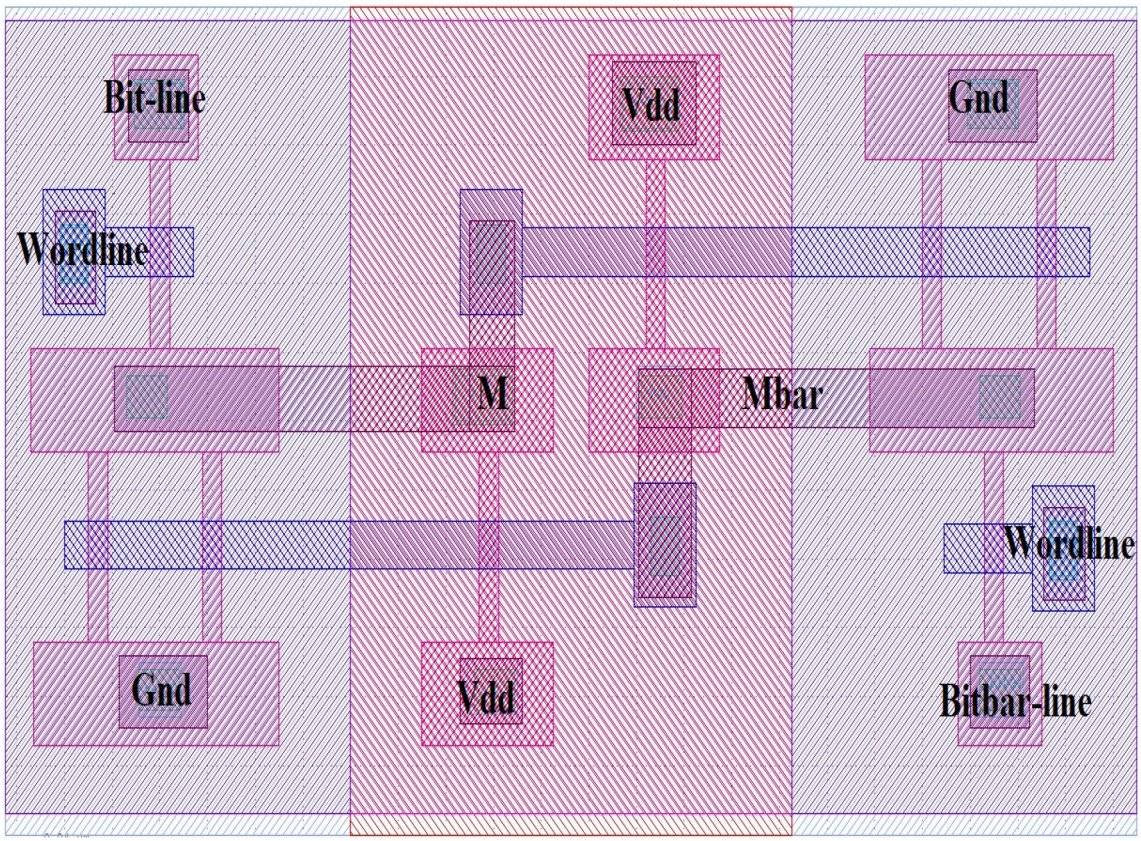
- *Write operation* The voltage levels of bitlines are opposite to each other as delineated in Fig. 7a, and the WL is connected to Vdd as outlined in Fig. 7b. This condition will turn on the transistors T5 and T6. In this situation, the voltage level of node M drops and the voltage level of node Mbar rises until the voltage level of M is enough to turn on T4 and turn off T2, or the voltage level at node Mbar is sufficient to turn on T3 and turn off T1. Subsequently, the voltage level of Mbar and M nodes will be turned over to "1" and "0" respectively, as displayed in Fig. 7c. Figure 7 outlines the write operation simulated in TCAD for FinFET based 6 T SRAM cell. The timing diagrams for bit-line, output M and write current are depicted in Fig. 7d, Fig. 7e, f, respectively [16, 18, 31, 32].

3.3 Stability Analysis of SRAM Cell-I and SRAM Cell-II

- *Read Static Noise Margin (RSNM):* RSNM is the least amount of noise voltage level needed at the storage nodes of SRAM to flip the cell data [16, 31, 33]. The set-up utilized for measuring the RSNM parameter of SRAM Cell-I is outlined in Fig. 8. WL and bit-line are connected to Vdd in this set-up, and the feedback is disconnected from the cross-coupled inverters. The voltage transfer curve (VTC) of the inverter in the half circuit has been plotted with its inverse to form a butterfly curve. The largest side of the square fitted in the butterfly curve signifies as Read SNM. The extracted value of RSNM for 6 T SRAM Cell-I at Vdd = 0.8 V is 175 mV, as shown in a butterfly curve in Fig. 10.
- *Write Static Noise Margin (WSNM):* Write Margin is another crucial parameter that ensures robust write operation and is calculated using a butterfly curve, as demonstrated in Fig. 10. During the write operation, the cross-coupled inverters are disconnected from each other. The WL joins Vdd, and the data is forced onto the bitlines from the cell, as shown in Fig. 9. The inverters' VTCs in half circuits has been plotted between M and Mbar, since the bitline is connected to Gnd and bitbar-line is connected to Vdd. Therefore, the VTCs of the two halves are not the same. The larger side of the fitted square, in between the two curves, as depicted in Fig. 10, is named as WSNM. A higher WSNM implies better write stability [16, 31–34].



(a)Schematic layout of Cell-I



(b) Schematic layout of Cell-II

Fig. 5 TCAD implementation of FinFET based 6 T SRAM cells containing different fin configurations

Table 4 SRAM cells with different fin configurations

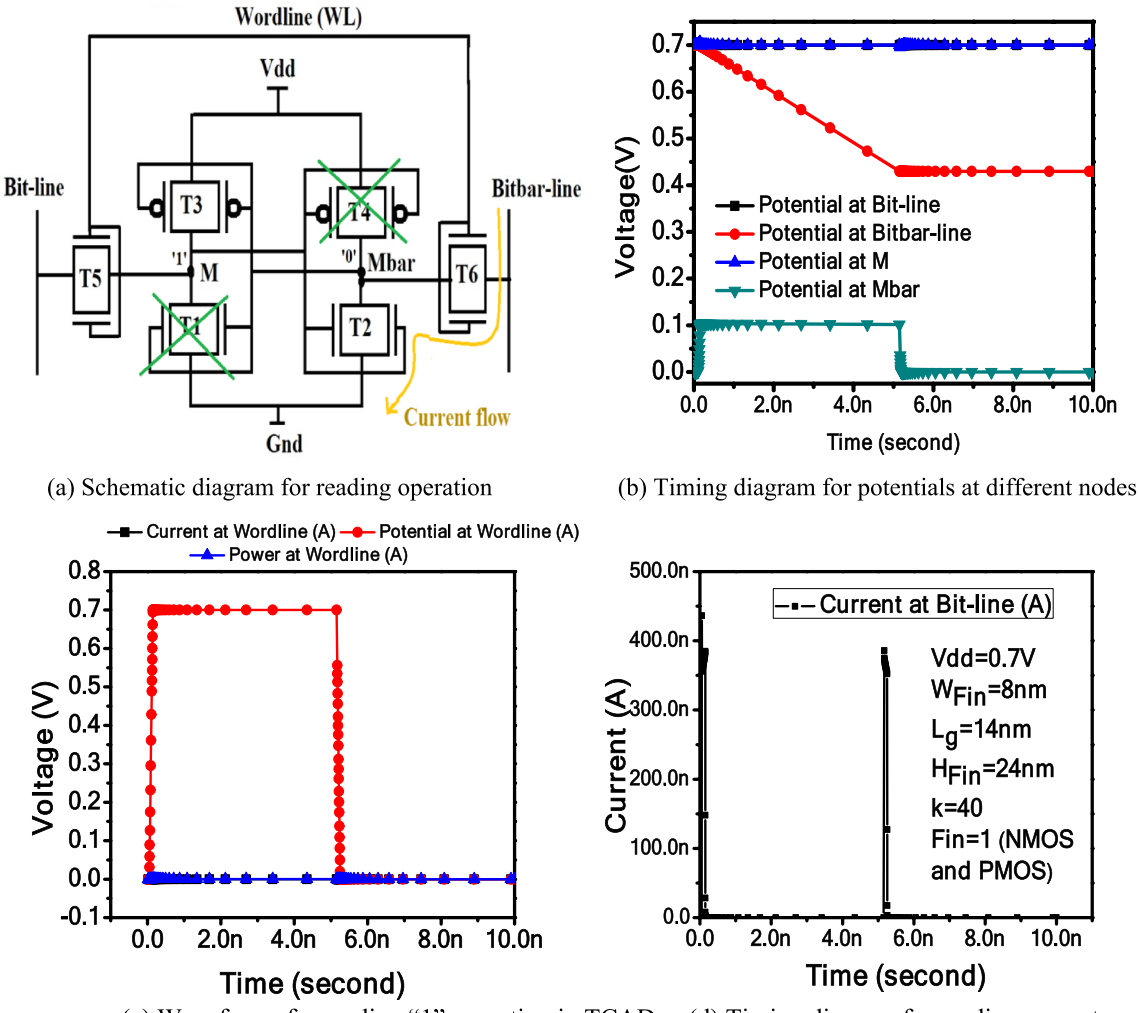
Fin configuration	Cell-I	Cell-II
Pull-up transistor	1	1
Access transistor	1	1
Pull-down transistor	1	2
Area Consumption (μm^2)	0.0775(0.3875*0.2)	0.0908 (0.454*0.2)

3.4 Impact on 6 T SRAM Cells Stabilities due to supply voltage variations

The impact of voltage variations on RSNM and WSNM was analyzed over 0.4–1.0 V for 6T SRAM Cell-I and Cell-II. Figure 11a illustrates that Cell-I shows improved results for RSNM and WSNM w.r.t Cell-II. It is also noted that RSNM enhances by 14.6× and 4.6× for Cell-I and Cell-II respectively, as the voltage varies from 0.4 to 1.0 V. The Cell-I and Cell-II demonstrated similar improvement for the lower voltage for RSNM. It is clear from Fig. 11b that the percentage change of WSNM of Cell-I over Cell-II increases from 20% at 0.4 V to 75% at 1.0 V. The area consumed by Cell-II is 14% more than Cell-I, as outlined in Table 4. Therefore, the proposed Cell-I achieves considerable improvement in the stability of FinFET based 6T SRAM cell [35, 36].

3.5 Impact on 6 T SRAM Cells Leakage Power Due to Supply Voltage Fluctuations

The leakage power is the SRAM cell's power in the absence of any switching activity or during hold mode. The multiplication of supply voltage and leakage current signifies leakage power. Subthreshold current is the main contributor to leakage current that flows from drain to the source



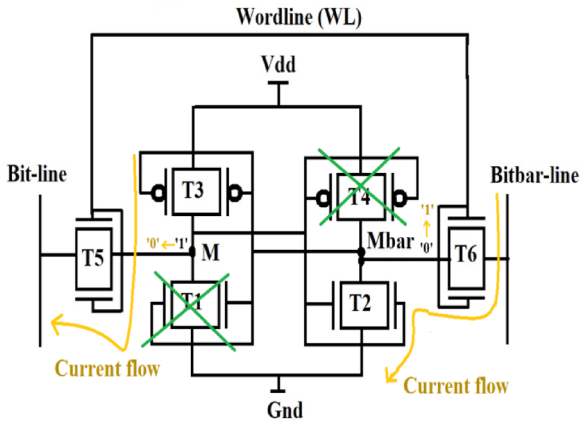
(a) Schematic diagram for reading operation

(b) Timing diagram for potentials at different nodes

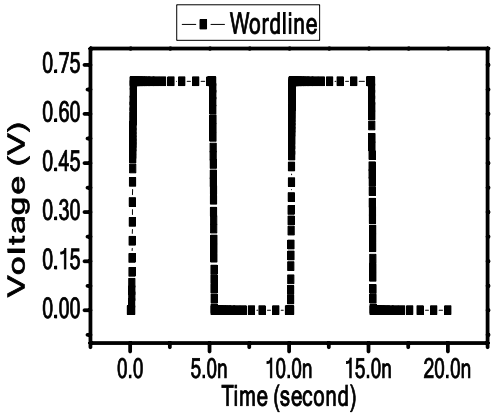
(c) Waveforms for reading "1" operation in TCAD

(d) Timing diagram for reading current

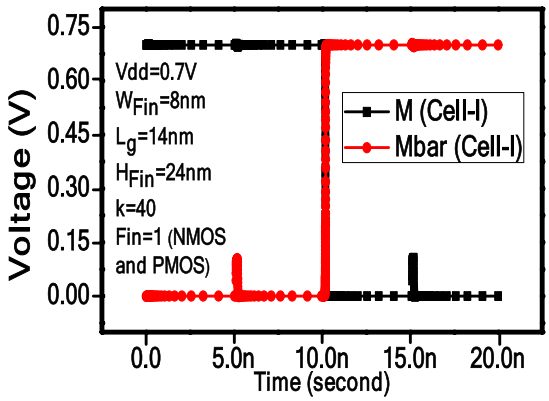
Fig. 6 Read operation for FinFET based 6 T SRAM Cell-I in TCAD



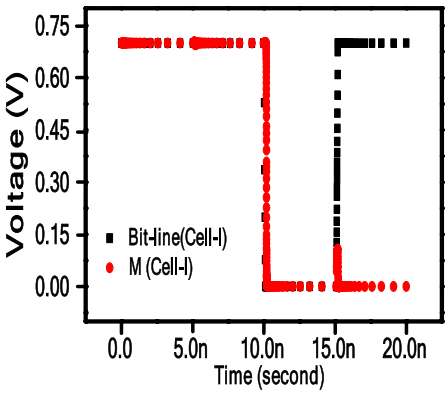
(a) Schematic diagram for writing operation



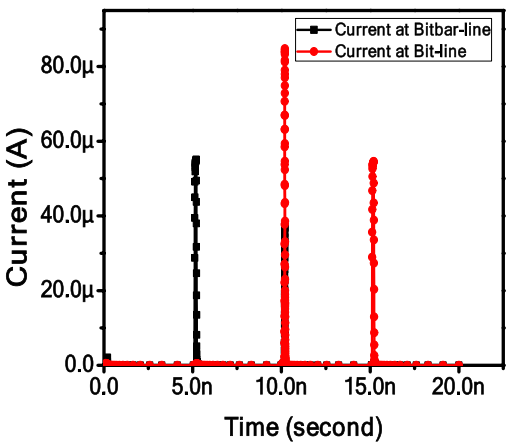
(b) Timing diagram for wordline



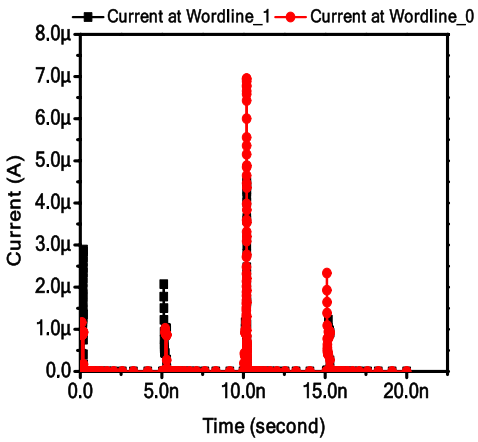
(c) Waveforms showing outputs ('M' and 'Mbar')



(d) Timing diagram for bit-line and output ('M').



(e) Timing diagrams for current at bitlines



(f) Timing diagrams for current at wordlines

Fig. 7 Write operation for FinFET based 6 T SRAM Cell-I in TCAD

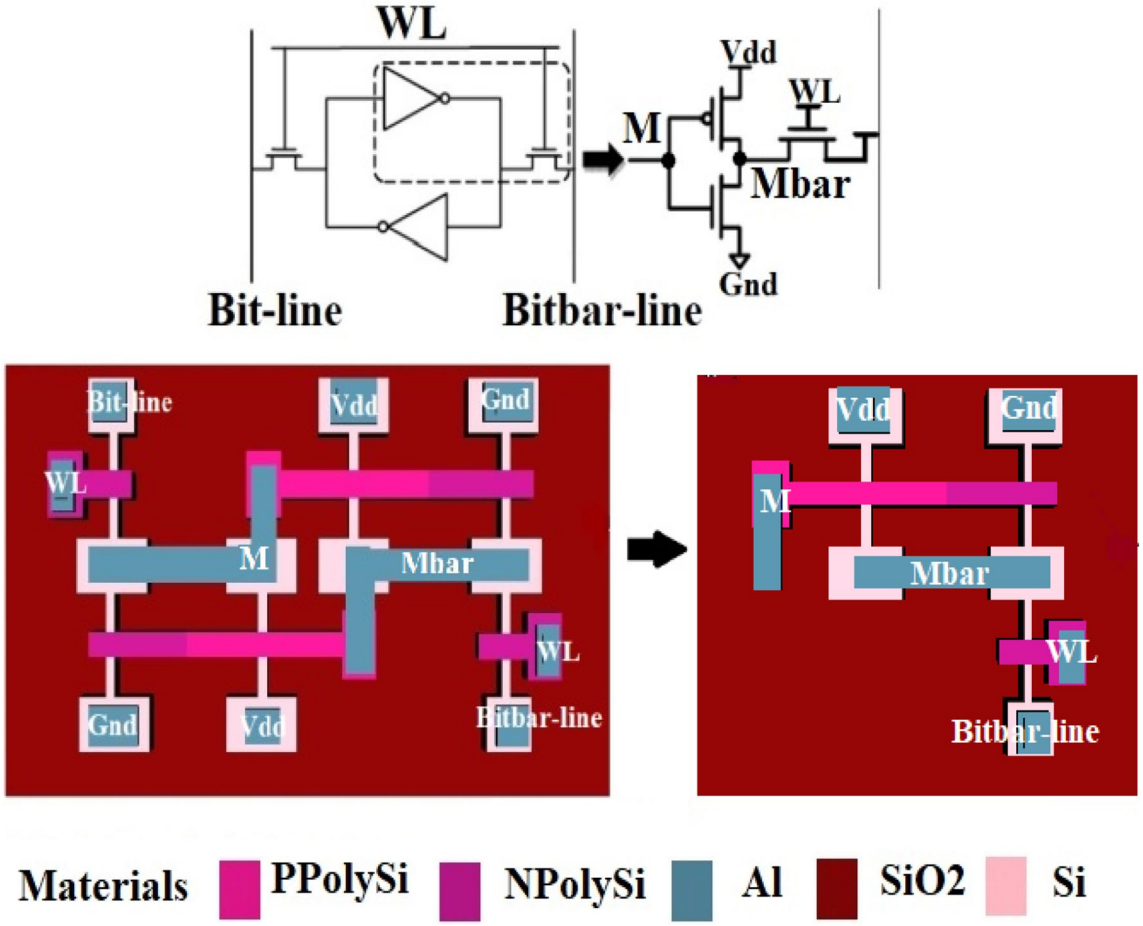


Fig. 8 Set-up for measuring RSNM of FinFET based 6 T SRAM Cell-I

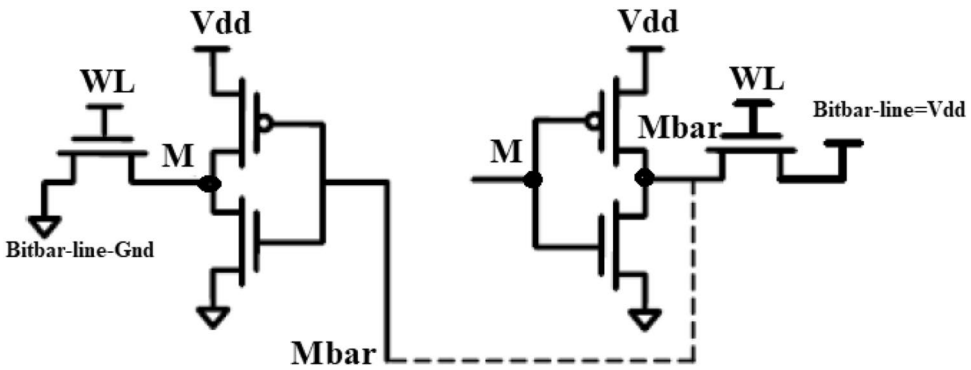


Fig. 9 Set-up for measuring WSNM of SRAM Cell-I

when the device is in the cutoff state [37, 38]. Figure 12a, b demonstrates that the leakage power of Cell-II is more (in nanowatts) as compared to Cell-I (in femtowatts) due to the large leakage current produced by the transistors of Cell-II. The leakage suppression can be done by minimizing supply voltage, as it has been observed that the supply voltage of 1 V has 2.5 times more leakage power than Vdd=0.4 V [39].

3.6 Comparison of Proposed FinFET Based 6 T SRAM Cell-I with Published Work

Carlson et al. [40] gave the values 175 mV and 0.358 μm^2 for *RSNM* and area consumption of cell, while the proposed Cell-I demonstrates improvement of 37% and 78%

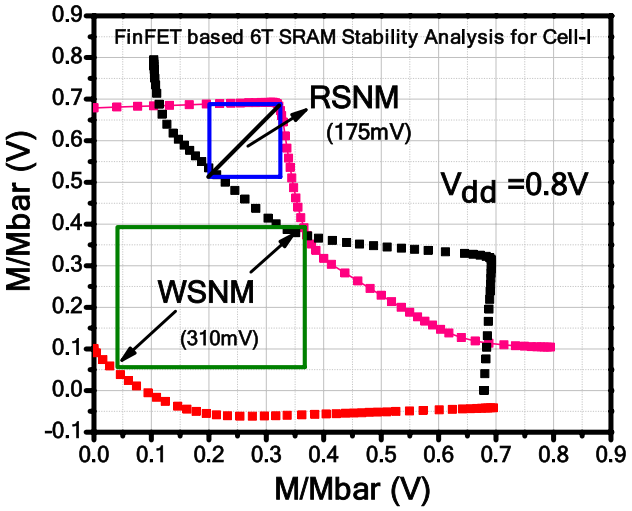
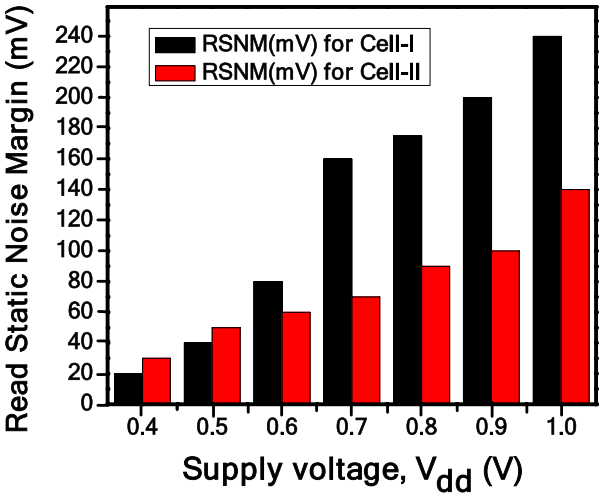
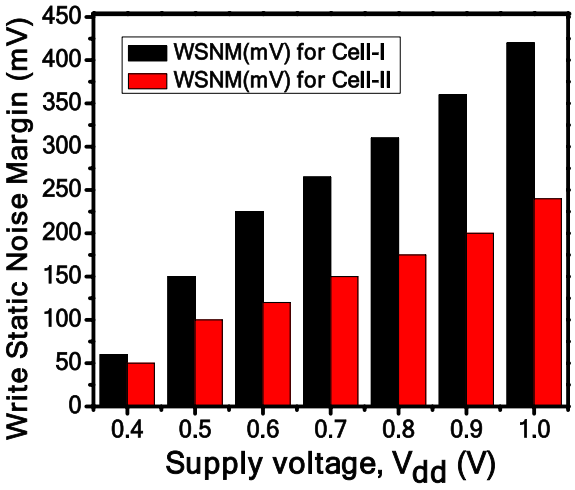


Fig. 10 VTC for indicating RSNM and WSNM for SRAM Cell-I



(a) Supply voltage fluctuation impact on RSNM for Cell-I and Cell-II



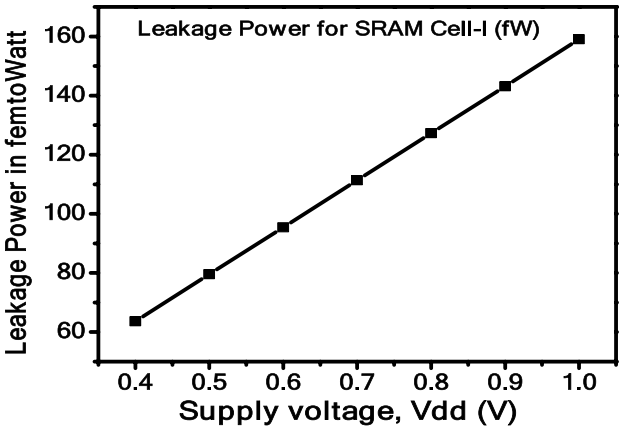
(b) Supply voltage fluctuation impact on WSNM for Cell-I and Cell-II

Fig. 11 Impact of supply voltage variation on RSNM and WSNM for Cell-I and Cell-II

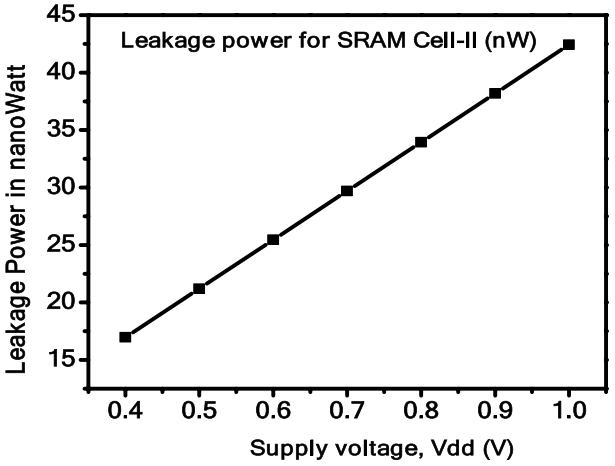
respectively, for these metrics. The proposed cell presents about 1.5 × and 2 × enhancement for RSNM compared to results extracted by Li et al. and Lim et al. respectively [16, 17]. The proposed structure utilizes a comparable area as consumed by an Intel processor at the same technology node [41–43]. The progress of 3.3% for WSNM has been presented by current research when compared with the Carlson et al.'s results at 22 nm technology [40]. It has been realized that a 6T SRAM cell designed with proposed FinFET shows reduced area and improved stability because of the amalgamation approach of work function engineering (common gate material) and high-k gate dielectric oxide in the FinFET devices.

4 Conclusion

In this paper, the 14 nm gate length FinFET device using lanthanum doped zirconium oxide as high—k gate dielectric material has been proposed to improve SCEs, the leakage performance and SNM for 6 T SRAM cells. The diminished values of SS, I_{OFF}, DIBL and enhanced values of I_{ON} & g_m are observed after simulating the proposed devices. Further, two SRAM cells based on the improved devices were implemented with different fin configurations. The cell stability metrics such as RSNM and WSNM were evaluated for two types of fin configuration cells using the butterfly method. The SRAM Cell-I has presented better read static noise margin and write static noise margin in comparison to SRAM Cell-II. The Cell-II has almost 50% reduced RSNM and WSNM values at 0.8 V, and it also consumes 14% more area as compared to Cell-I. The effects of supply voltage variation on stability parameters and leakage power were also examined for 6 T SRAM cells. It has been realized that the proposed SRAM circuit has 9% larger RSNM and 3% more WSNM than the circuit designed by Sachid et al. (2008) [44]. The previous work presented the reduced leakage power in the range of 10^{-15} for designed Cell-I as compared to the later works (10^{-9}). In the current work, the improvement of RSNM is 5x, reduction of WSNM is 2.7%, and declination of the leakage power is in the order of 10^{-3} when matched with the work done by Saun and Kumar [45].



(a) Influence of supply voltage variation on leakage power for Cell-I



(b) Influence of supply voltage variation on leakage power for Cell-II

Fig. 12 Leakage power estimation for SRAM Cell-I and SRAM Cell-II

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