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REVIEW PAPER

Comprehensive Review on Amorphous Oxide Semiconductor Thin Film Transistor

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Abstract
Oxide materials are one of the most advanced key technology in the thin film transistors (TFTs) for the high-end of device applications. Amorphous oxide semiconductors (AOSs) have leading technique for flat panel display, active matrix organic light emitting display, active matrix liquid crystal display as well as thin film electronic devices due to their excellent electrical characteristics, such as field effect mobility (μ_{FE}), subthreshold swing (*SS*) and threshold voltage (V_{th}). Researchers from various fields have studied and considered ways to improve μ_{FE} of AOS TFT, which has been studied for 16 years since 2004. Since 2004, mobility has been increased by using various methods, such as designing novel amorphous oxide materials, changing device structures, or adopting new post-treatment. The development of field effect mobility as well as the stability enhancement has been comprehensively reviewed in this report.

Keywords Amorphous oxide semiconductor · Thin film transistor · Mobility · Stability · Comprehensive review

1 Introduction

According to the Moore's law, the number of transistors doubles approximately every 2 years as shown in Fig. 1a [1, 2]. However, the Moore's law has been broken because of fast speed of developing integrity. Nowdays, the Kim's law has been applied to the memory stack as shown in Fig. 1b. As various displays and applications have evolved, the demand for high performance on devices has increased. In particular, high end product displays and integrated circuits which required high performance [3–5]. Among many candidate materials to be the next generation electronic applications, amorphous oxide semiconductor (AOS) materials are promising candidate materials due to the excellent characteristics. At the 2004, the development of AOS thin film transistor (TFT), a-IGZO TFT by Hosono et al. [5] has been remarkable. In the early period, it showed characteristics not well developed, such as low field effect mobility (μ_{FE}), bad on–off current ratio ($I_{on/off}$), and large subthreshold swing (*SS*). It is important to note that the researches on the method to increase the mobility of the AOS TFT for the next generation display and various applications. Mobility changes were strongly depending on the composition ratio of a-IGZO material to clearly define mobility. Figure 2a and b show each characteristic of composition materials [6]. It is clearly shown the In_2O_3 increases the mobility. By the steady and continuous research, the stabilization and the mass production of materials has been achieved even in industrial field. Nowdays, the research have been carried out in new fields, such as integrated circuit, memory devices, synapse, neuromorphic and artificial intelligence (AI) using some of the characteristics of AOS materials [7–9]. The μ_{FE} was calculated by the following Eq. (1) [10]:

$$\mu_{FE} = \frac{L\, g_m}{W\, V_{ds} C_{OX}} \tag{1}$$

where the *W/L* is the width/length of the channel layer, g_m is the trans-conductance, C_{ox} is the oxide capacitance of the gate dielectric and V_{ds} is the drain to source voltage.

In this paper, we reviewed and summarized the ways to improve AOS TFT mobility and stability by three category of designing new channel materials of AOS, fabricating new structure of the AOS TFTs, and adopting new post processing treatment on the channel materials.

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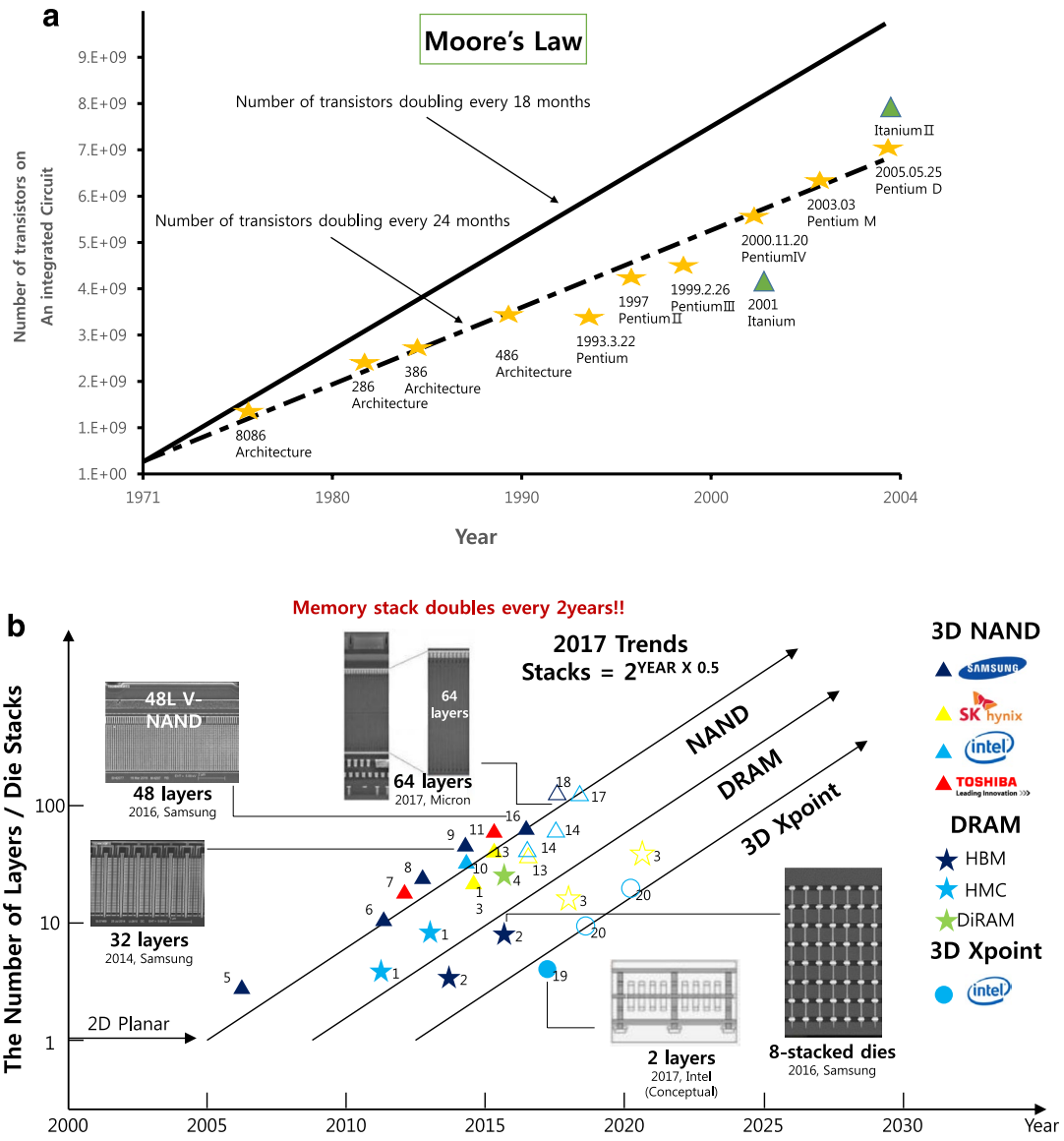


Fig. 1 **a** The Moore's law, the number of transistors doubling every 24 months. **b** The Kim's law, the memory stack doubles every 2 years

2 Materials Based AOS TFTs

Figure 3 shows the total μ_{FE} depending on the year. There are several approaches in material modifications increase the μ_{FE}. At the 2004, H. Hosono et al. [5] reported the amorphous InGaZnO (a-IGZO) with 5.5 cm^2/Vs. Figure 4 shows (a) covalent semiconductors, for examples, silicon crystalline and amorphous. The post-transition-metal oxide semiconductors with crystalline and amorphous phase were shown in Fig. 4b. After this, lots of researchers tried to apply these materials to device applications. After developed the a-IGZO, indium is the key element of the AOS TFTs. Because In^{3+} plays a significant role in achieving high mobility, which is attributed to configuration of $4d^{10}5s^0$ [5, 11–13]. So, most materials are developed with In-based materials. Tsukagoshi et al. [14] reported the InO_x-based doped with TiO_2, WO_3, or SiO_2. Their mobility exhibit 32, 30 and 17 cm^2/Vs with In-Ti–O, In-W–O and In-Si–O, respectively.

Among the lots of materials, indium (In) has the problems, such as high fabrication cost because of the rare atom in the earth and toxicity. So, AOS needs the new materials, *i.e.*, In-free materials. In a previous study, we reported the In-free material AOS TFTs called amorphous Zn–Sn–O

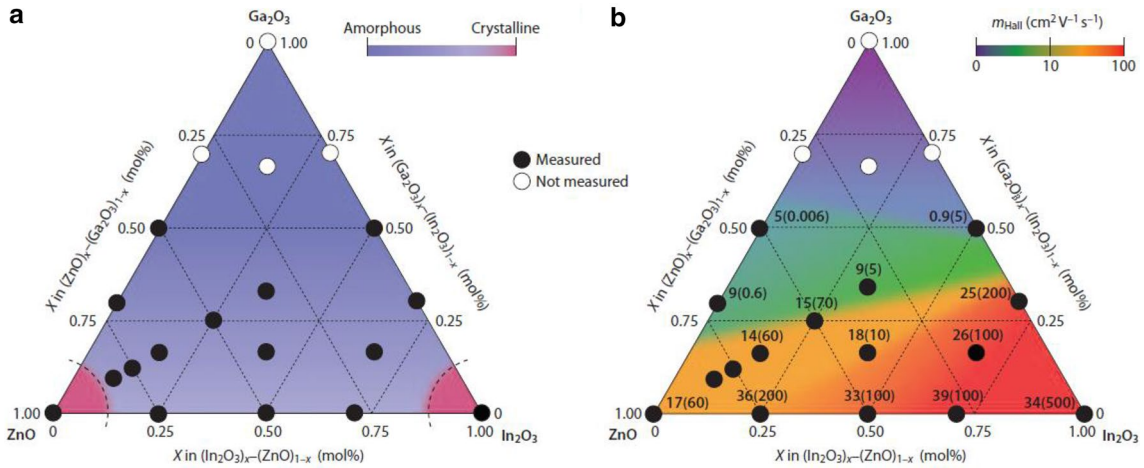


Fig. 2 **a** Amorphous formation and **b** electron transport properties of In_2O_3–Ga_2O_3–ZnO thin films. The values in **b** denote the electron Hall mobility (cm^2/V s) with density (10^{18} cm^{-3}) in parentheses [6]

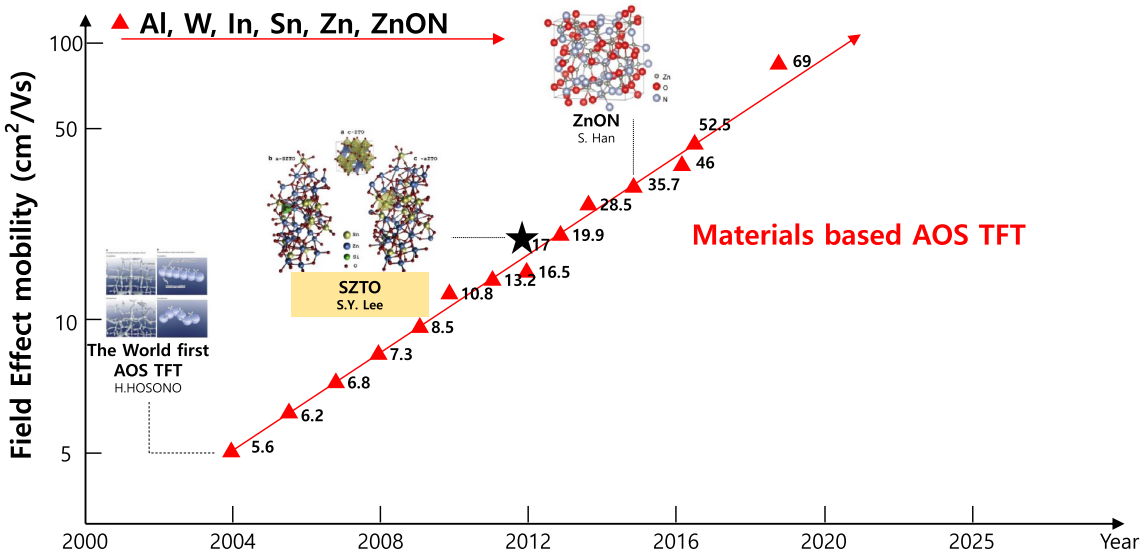


Fig. 3 The μ_{FE} depending on various amorphous oxide materials

(a-ZTO) and amorphous Si doped Zn–Sn–O (a-SZTO) [15]. Figure 5 shows (a) the crystal structure of c-Zn_2SnO_4, the amorphous structure of (b) a-SZTO and (c) a-ZTO. Also, E. M. C. Fortunato et al. [16] reported the In free AOS TFTs with high mobility using the amorphous GaSnZnO (a-GSZO). The a-GSZO TFT have the different mobility from 7.9 to 24.6 cm^2/Vs depending on the annealing temperature.

Nitrogen doped to AOS materials have been reported to show the increase of μ_{FE} because the bandgap has been reduced compared with the conventional AOS channel materials [17]. Figure 6 shows the band diagram of Zn_3N_2, ZnON, and ZnO. Ryu et al. [17] reported the ZnON with high mobility value about 99 cm^2/Vs TFT. Figure 7 shows the atomic structure of ZnON formed by melt-and-quench simulations. Also, Kim et al. [18] and Ok et al. [19] reported the ZnON TFTs with 42.6 and 50 cm^2/Vs. Park et al. [20] reported the high μ_{FE} of 52.5 cm^2/Vs of ZnON TFTs with UV-assisted ozone (UVO) annealing at 150 °C.

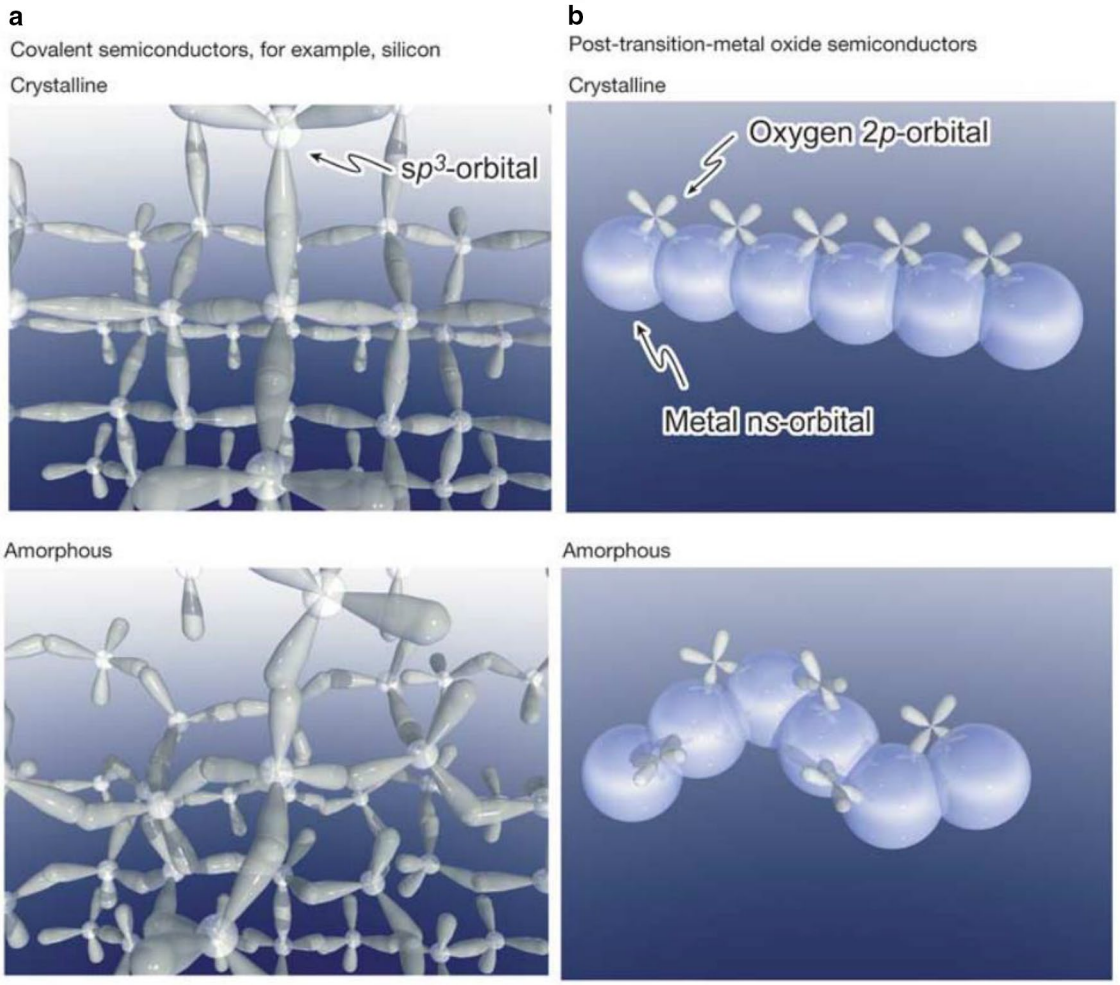


Fig. 4 Schematic orbital drawings for the carrier transport paths (that is, conduction band bottoms) in crystalline and amorphous semiconductors. **a** Covalent semiconductors have carrier transport paths composed of strongly directive sp^3 orbitals, so structural randomness greatly degrades the magnitude of bond overlap, that is, carrier mobility. Note that the orbitals shown are illustrative, and do not show exact wavefunctions. **b** Amorphous oxide semiconductors composed of post-transition-metal cations. Spheres denote metal s orbitals. The contribution of oxygen 2*p* orbitals is small. Direct overlap between neighbouring metal sorbitals is rather large, and is not significantly affected even in an amorphous structure [5]

3 Structure Based AOS TFTs

Figure 8 shows the total μ_{FE} depending on the year. There are several methods to increase the μ_{FE} including TFT structure.

The configuration of AOS TFTs are primarily related to the μ_{FE}. There are 4 types of TFT structures, such as staggered, inverted staggered, coplanar and inverted coplanar. In general, bottom-gate structure has been widely used due to the convenience in fabrication [21]. However, this structure has critical disadvantage of the large parasitic capacitance due to the overlap between the gate and the S/D [22]. The large parasitic capacitance occurs the degradation of electrical characteristic of TFTs. Therefore, the AOS TFT needs the self-aligned structure to achieve the high performance, necessary. Kim et al. reported the μ_{FE} of 5.5 cm^2/Vs with a-GIZO TFT at self-aligned top gate structure [23]. To increase the μ_{FE}, many research groups tried to stack the channel, such as bi-layer, double layer and buried layer, etc. The μ_{FE} is mainly affected by the current path at the bottom. In the general, most of channel layer consist of 2 parts,

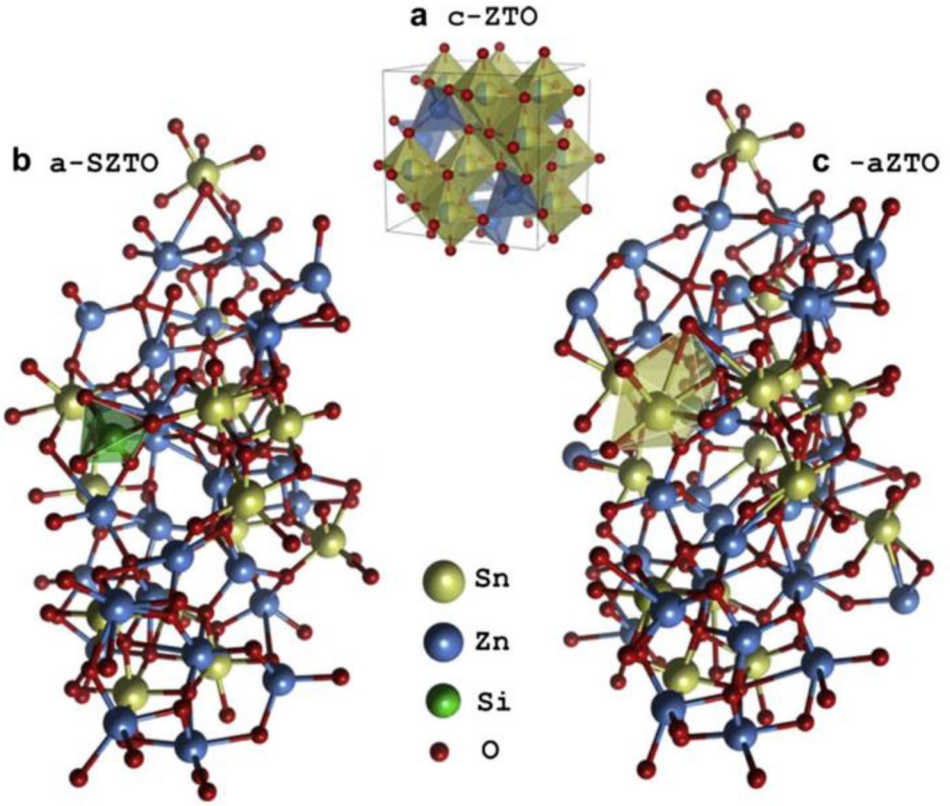


Fig. 5 **a** The crystal structure of c-Zn_2SnO_4. The amorphous structure of **b** a-SZTO and **c** a-ZTO. The oxygen coordination number of Sn is 7 and the oxygen coordination number of replaced Si atom changed to 4, keeping the local tetrahedron structure [15]

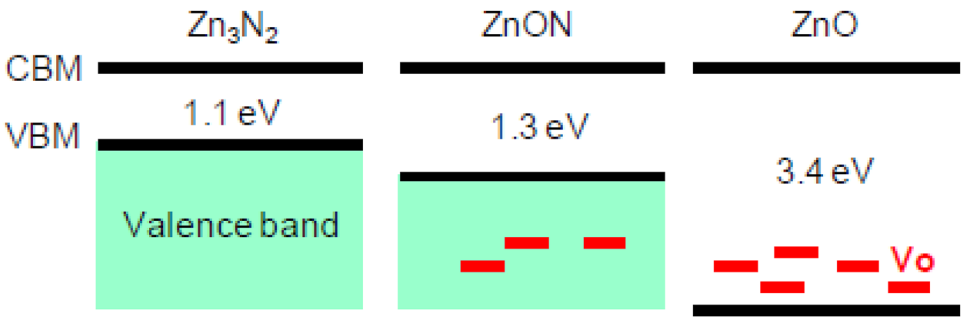


Fig. 6 Schematic band diagram of Zn_3N_2, ZnON, and ZnO [17]

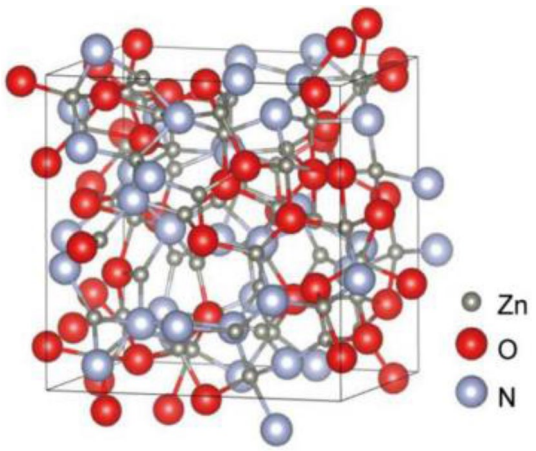


Fig. 7 An atomic structure of a-$Zn_{60}O_{24}N_{24}$ formed by melt-and-quench simulation [17]

bottom channel and top channel layer. The top channel layer was consisting of the semiconducting materials and the bottom channel layer was consisting of highly conducting materials, such as In_2O_3, InZnO and IWO [24–27]. Zhang et al. [24] reported the IGZO/In_2O_3 dual-channel structure AOS TFTs. The μ_{FE} increased significantly from 10.2 to 34.3 cm^2/Vs as a result of the change from single layer to dual channel TFT. Similarly, Yoo et al. [25] reported the AlInZnSnO and InZnO AOS TFTs. Figure 9 shows (a) Schematic cross section of AIZTO/IZO double-layer TFT and (b) the TEM image of the fabricated double-layer TFT and AIZTO/IZO channels. It is clearly shown the channel materials are separated. Figure 10 shows the μ_{FE} depending on the thickness of IZO channel layer consist of 0, 2, 4, 6, 8 and 10 nm, respectively. The μ_{FE} increased from 27.6 to 53.2 cm^2/Vs as increasing the IZO channel thickness.

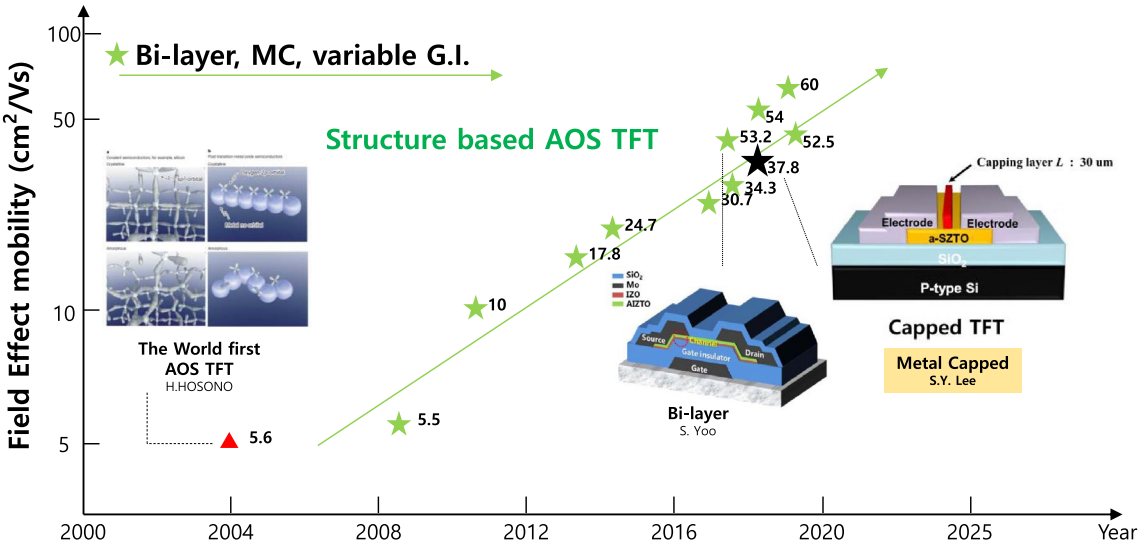


Fig. 8 The μ_{FE} depending on TFT structure

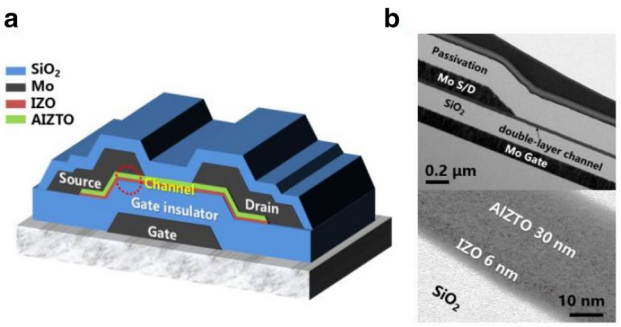


Fig. 9 **a** Schematic cross section of AIZTO/IZO double-layer channel BCE TFT. **b** Cross-sectional TEM image of the fabricated double-layer BCE TFT and AIZTO/IZO channels [25]

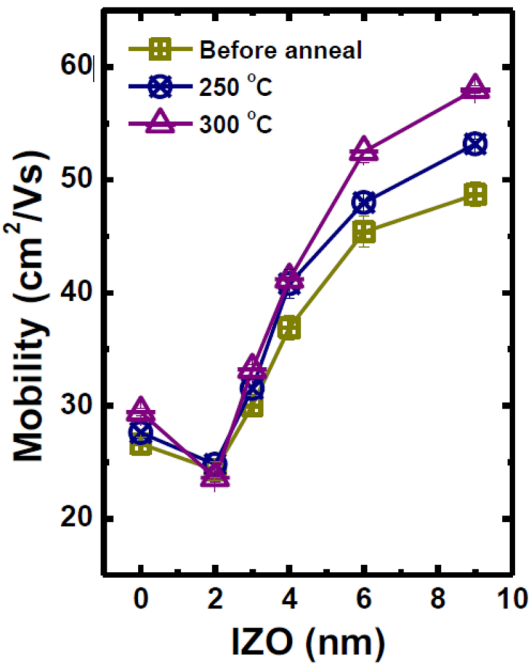


Fig. 10 Transfer curves of 30-nm-thick AIZTO single-layer TFT (control) and AIZTO/IZO (30 nm/9 nm) double-layer TFT (W/L = 40/20, annealed at 250 °C) [25]

As described above, the top and bottom layers may be manufactured differently. However, some researcher tried to another method, the top and bottom materials may be the same, but may be manufactured by changing the composition ratio of the materials, or may be manufactured by changing the partial pressure ratio of oxygen. Liu et al. [28] reported the a-IGZO TFT by double layers with no oxygen flow (NOF) and oxygen flow (OF) channel. Figure 11 shows the schematic diagrams of (a) single layer-TFT and (b) double layer TFT. The single layer TFT of NOF and OF exhibit the 12 cm^2/Vs of μ_{FE}. However, the double layer shows 19 cm^2/Vs of μ_{FE}. Also, Lee et al. [29] reported the TFT using the Hf doped IZO (HIZO) channel materials with different Hf ratios. As a result, device stability as well as the mobility of dual (or bi, double, burried) layer devices can also be significantly improved compared with a single channel layer.

The metal capping (MC) layer is easier way to increase the mobility compared with the previous method. This is a method of improving mobility by depositing metal on

Fig. 11 Schematics of the cross-sectional diagrams (not scaled) of **a** SL-TFT and **b** DL-TFT [28]

top of the channel layer, which is usually achieved by two mechanisms. First, free electrons in the channel layer may increase as electrons in the metal diffuse into the channel layer due to work function differences. In a previous study, we reported the carrier controllability with variable metal capping layer [30]. Figure 12 shows (a) the schematic diagram of conventional-TFT and metal capped-TFT, (b) the transfer curve and (c) electrical characteristics of TFTs with variable metal. The μ_{FE} increased from 20.79 cm^2/Vs as conventional TFT to 37.84 cm^2/Vs as Al capped TFT. It is attributed by the work function as shown Fig. 13. The Ag metal capped degrade the electrical characteristics because of the high work function. In other hand, the Al capped layer have lowest work function compared with other materials. In the second case, the mobility is increased because of the ω-shape current-path in the channel layer [31]. Figure 14 shows simulated total current–density distribution of SZTO TFTs as function of MC-length with (a) 0 (CON-), (b) 20, (c) 30 and (d) 40 μm. The L of MC layer increased, μ_{FE} also increased because the carrier can easily pass the path.

4 Post Process Based AOS TFTs

Figure 15 shows the total μ_{FE} using the post-process depending on the year. There are several post-process treatments to increase the mobility. In general, the oxygen vacancies (V_O) are well known as the primary driving mechanism for amorphous oxide materials. Where the oxygen atom escapes in the channel material, two electrons are generated [32].

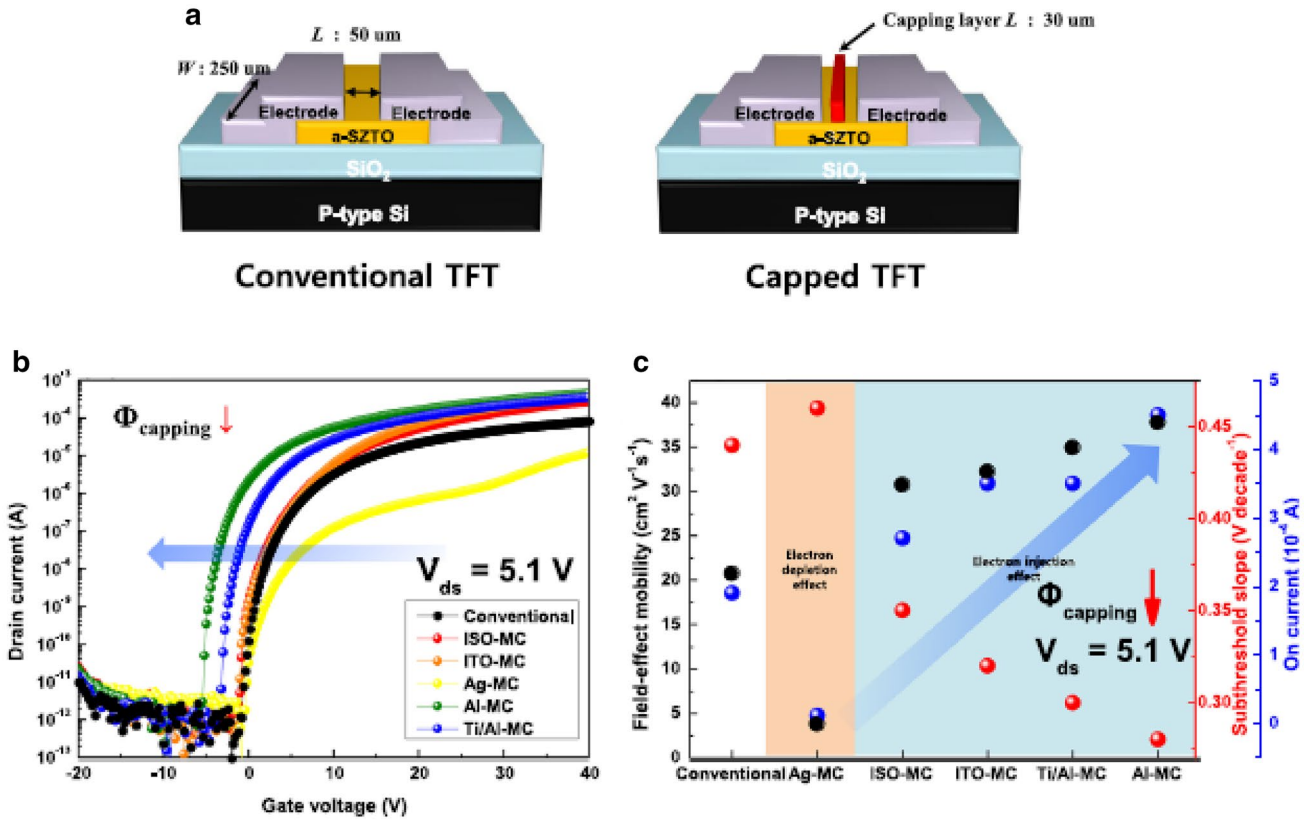


Fig. 12 **a** Schematic view of conventional-TFT and capped-TFT. **b** Transfer characteristic and **c** electrical performance of TFTs with different capping layer [30]

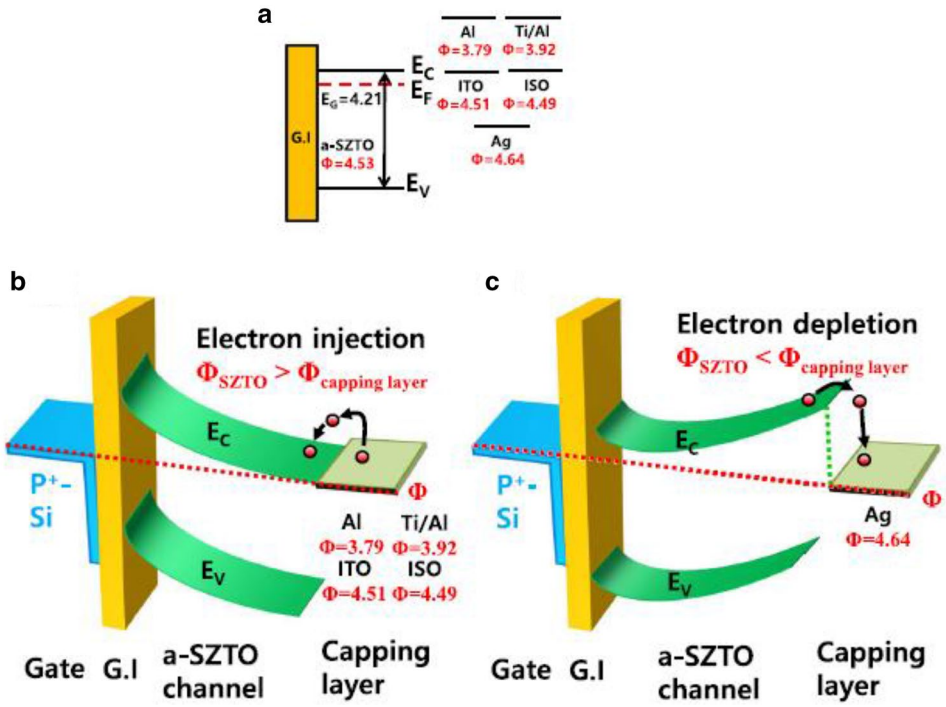


Fig. 13 Energy band diagram of SZTO-TFTs with different capping layer in thermal equilibrium. **a** noncontact, **b** electron-injection model (when $\Phi_{SZTO} > \Phi_{capping\ layer}$), and **c** electron-depletion model (when $\Phi_{SZTO} < \Phi c_{apping\ layer}$) [30]

Using this phenomenon is an effective way to obtain a large amount of electrons. The simplest method among the numerous methods is to perform plasma treatment on the channel layer. At the 2007, according to Jeong et al. [33], the mobility of the pristine a-IGZO was only 3.3 cm^2/Vs, but the Ar plasma treatment achieved 9.1 cm^2/Vs. This method has been used in many ways. In particular, it is used to form not only a channel layer but also an S/D electrode [34].

In the case of AOS TFT, still annealing process was necessary even not high temperature annealing like low temperature polycrystalline silicon (LTPS), for the activation of the thin film. So many researchers have tried to obtain high electrical characteristics and mobility while replacing this annealing. Lee et al. [35] used microwave annealing technology to fabricate an amorphous InGaZnO Thin Film Transistor (a-IGZO TFT) with 13.9 cm^2/Vs carrier mobility instead of conventional thermal annealing. Generally, the ZnO based materials can absorb the electromagnetic wave energy from 2 to 18 GHz frequency range [35–37]. Figure 16a shows the schematic of microwave annealing process. The power of microwave was set at 1P (600 W) and 2P (1200 W), the frequency used at 5.8 GHz. Figure 16b shows the transfer curve of a-IGZO TFTs depending on the microwave annealing conditions. Figure 16c shows the stability of devices depending on the microwave annealing conditions. During the gate bias stress (GBS) measurement, an electric field of 2.5 MV/cm was used. After the GBS test, the V_{th} shift of a microwave annealed a-IGZO TFT was reduced from a value of 16.2 V at a power condition of 1P for 100 s to a minimum of 1.6 V at 2P power for 100 s. In addition, W-J. Cho et al. [38], a-IGZO with microwave annealing irradiation showed a mobility of 17.4 cm^2/Vs (1000 W) higher than conventional thermal annealing of 14 cm^2/Vs. As a result of this phenomenon, the microwave annealing process can be same effect as the thermal annealing method to activate the channel layer.

As mentioned above, annealing process is required to improve electrical properties in AOS TFTs, and generally performed by furnace and ovens. On the other hand, the rapid thermal process (RTP) offers several benefits, better uniformity, including faster process times. This is the main key factors in the mass production industry. S–H. Ko. Park et al. [39] investigated the RTP with near-infrared (NIR) as a heat source, ultra-violet (UV) and deep-ultra-violet (DUV) as a light source. It is possible to activate the channel layer easier, can provides the much higher energy. Figure 17a shows the structure of back channel etched (BCE) TFTs, (b) material information used in this work, and (c) conditions of 1st annealing process using the RTP and oven. The electrical characteristics of the Al-ITZO TFTs depending on

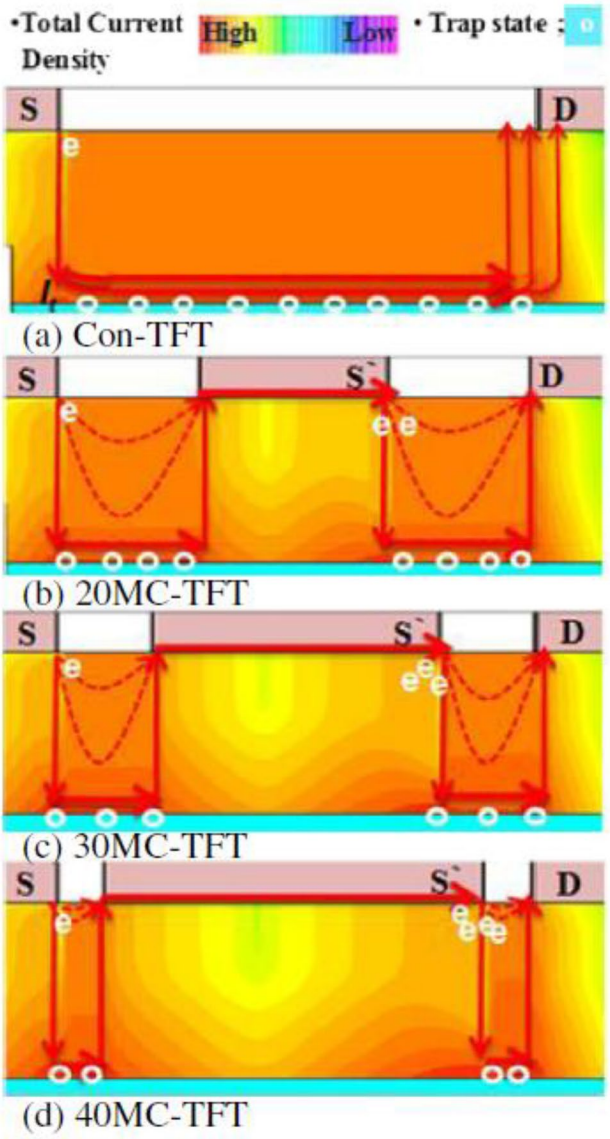


Fig. 14 Simulated total current–density distribution of SZTO TFTs as function of MC-length with **a** 0 (CON-), **b** 20, **c** 30 and **d** 40 μm. The It is trap-site in interface between channel and gate insulator [31]

the oven and variable RTP (NIR, UV/NIR, DUV/NIR) was summarized on Table 1. To confirm the uniformity, the 32 different devices were measured in 6 inch wafer. The mobility was increased from 24.1 cm^2/Vs in the oven annealing to the 29.1 cm^2/Vs in the DUV/NIR annealing. This phenomenon was related to the Fig. 18a measured X-ray reflectivity (XRR) results for the Al-IZTO film annealed at 280 °C in air using oven and RTP (NIR, UV/NIR, and DUV/NIR and (b) summary of calculated density of films after annealing. The density values of the XRR results were 6.65 and 6.64 g/cm^3, for ovens and RTP-NIR annealing. In contrast, density increased to 6.71 and 6.87 g/cm^3 after UV and DUV, respectively. In general, the density of oxidation semiconductors after heat removal can be described as structural relaxation/recovery and/or absorption of oxygen to film, and in this operation, two effects can occur simultaneously [40]. The energy of UV region is sufficient to break unstable chemical bonds, such as weakly coupled atoms and metal/oxygen interaction in the oxide layer [41]. Therefore, UV and DUV can broken the weak-bonds in the Al-ITZO film, and more effective recovery and structural relaxation occur during the step 2 (RTP annealing with NIR). In addition, under oxidation conditions, during the reduction process, oxygen can be incorporated into the active layer surface to spread to the bulk area, thereby increasing film density [40, 42]. This effect becomes stronger as when the high-energy light source, DUV is radiated even in low-temperature annealing or annealing at high temperature.

Among the various post processing methods, there is also a method using intense pulsed light (IPL) irradiation. Park et al. [43] repots the effects of IPL on the electrical characteristics of ZnON TFTs with different irradiation energies. As the irradiation energy of IPL increased 30, 40, 45, and 50 J/cm^2 and the wavelength range of the xenon lamp was from 350 to 950 nm. The illustration of the IPL process on ZnON thin films and TFTs was shown in Fig. 19. The sample was irradiated with IPL with a 20 ms pulse duration. Figure 20 shows (a) the transfer curve of ZnON TFTs depending on the IPL irradiation energy and (b) the output curve of 40 J/cm^2, respectively. Representative electrical parameters such as threshold voltage (V_{th}), saturation mobility (μ_{sat}), and subthreshold swing (SS) are also listed in Table 2. The highest μ_{FE}, 48.4 cm^2/Vs was achieved and optimized at 40 J/cm^2. This degradation contributed to the change in nitrogen-related bonding states, such as nonstoichiometric Zn_xN_y and N–N bonding, rather than that of oxygen-related bonding states and the atomic composition of ZnON thin films. These results indicate that optimizing the IPL process allows us to produce high-performance ZnON TFTs very quickly without additional heat treatment, thereby achieving high-productivity TFT manufacturing.

5 The Mobility Versus Stability of AOS TFTs

There are three main factors that affect the stability of the AOS TFTs. First, the thermal stress (TS), the bias stress (BS) and the illumination stress (IS). In the BS, there are two types of positive bias stress test (PBS) that applies positive voltage and negative bias stress test (NBS) that applies

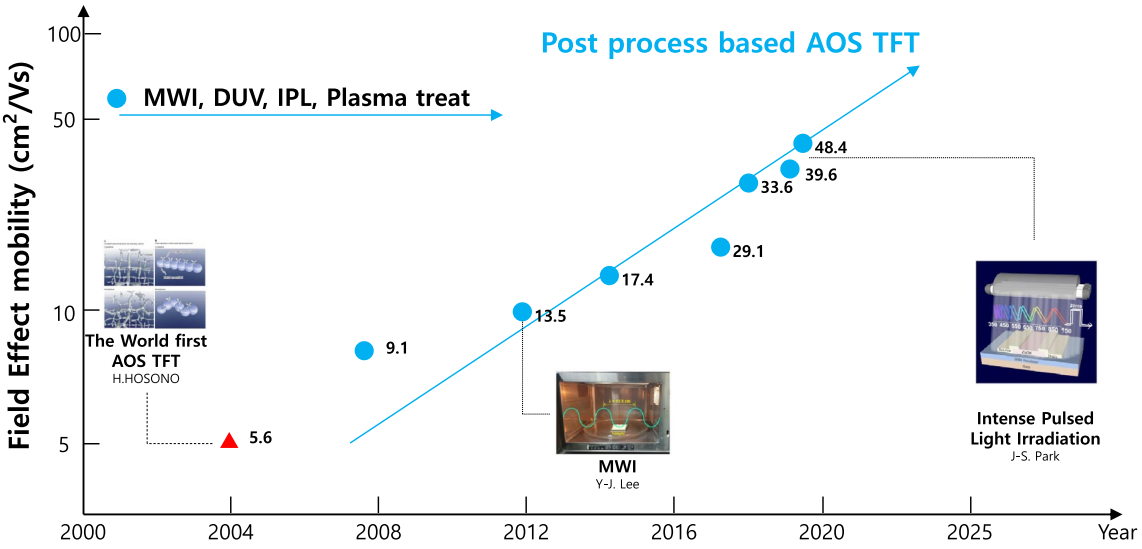


Fig. 15 The μ_{FE} depending on different post process treatment

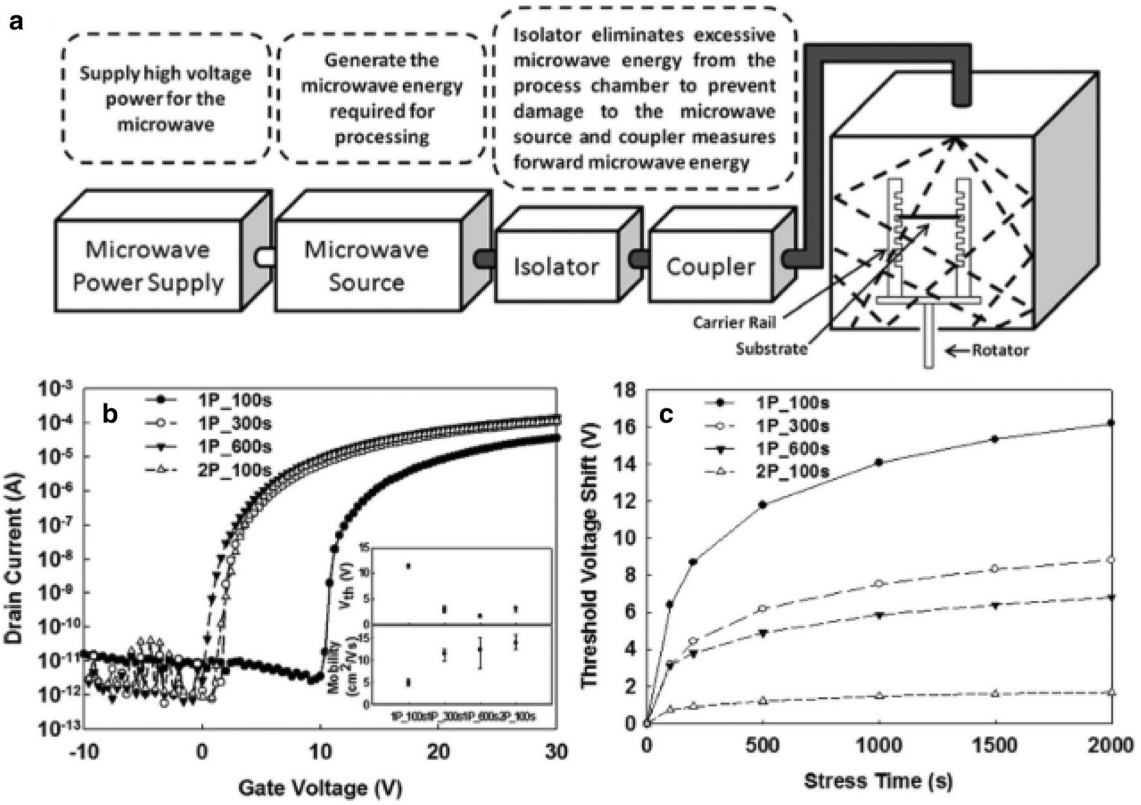
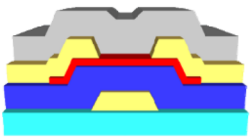


Fig. 16 **a** The schematic of microwave annealing system in this work. **b** The drain current (ID) versus gate voltage (VG) curves of a-IGZO TFTs with dif- ferent microwave annealing processes, at a drain-to-source voltage (VDS)of 11 V. The symbols of 1P_100s, 1P_300s, 1P_600s, and 2P_100s stand for the microwave annealed a-IGZO TFTs with 1P (600 W) for 100, 300, and 600 s, and 2P (1200 W) for 100 s, respec- tively. The corresponding device param- eters, such as threshold voltage (Vth) and mobility of a-IGZO TFTs are shown in the inset. **c** Threshold voltage shift of microwave-annealed a-IGZO TFTs as a function of gate bias stress durations. The electric field of gate bias stress was fixed at 2.5 MV/cm. The Vth shift was defined as the difference of the threshold voltages before and after the gate bias stress application to the a-IGZO TFT device [35]

a



b

Gate	Mo (150 nm)
Gate insulator	PE-CVD SiO_2 (200 nm)
Active	Al-IZTO (30 nm)
1st annealing @ 280°C air (oven and RTP)	
Source/Drain	Mo (150 nm)
Passivation	PE-CVD SiO_2 (200 nm)
2nd annealing @ 250°C in air (oven)	

c

Annealing method		Step 1		Step 2	
		Light source	Time (m)	Light source	Time (m)
RTP[1)]	Only NIR	-		NIR	30
	UV/NIR	UV	10	NIR	30
	DUV/NIR	DUV	10	NIR	30
Oven		-		-	120

Fig. 17 **a** Structure of BCE TFTs and **b** material information used in this work. **c** Conditions of 1st annealing process using the RTP and oven [39]

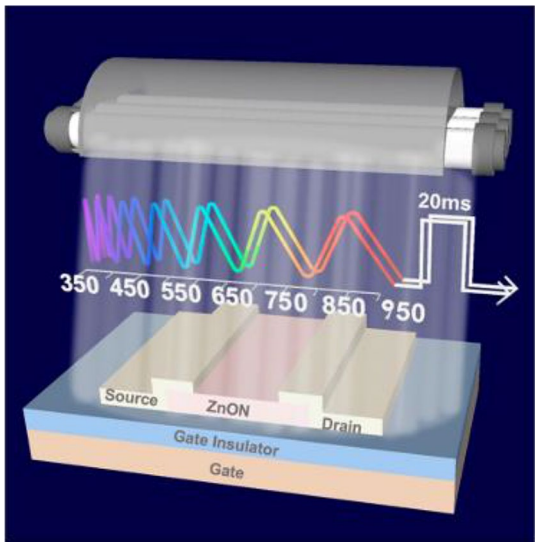
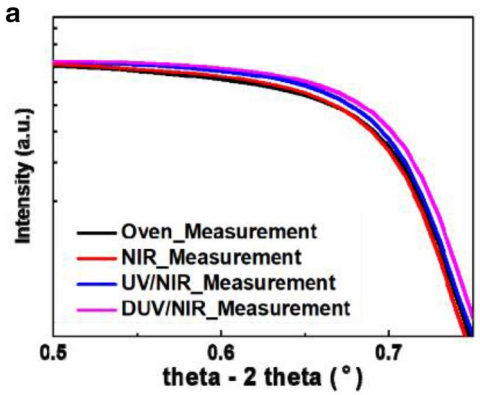


Fig. 19 Illustration of the intense pulsed-light (IPL) process on ZnON thin films and thin-film transistors (TFTs) [43]

Table 1 Summary of transfer properties of the Al-ITZO TFTs with 1st annealing using oven and RTP (NIR, UV/NIR, DUV/NIR) [39]

Annealing	Mobility (cm^2/Vs)	Hysteresis(V) @ V_{ds} = 0.1 V	V_{on} (V)	S.S (V/dec)
Oven (Ref)	24.1 ± 1.7	0.77 ± 0.2	−0.48 ± 1.02	0.11 ± 0.03
NIR only	27.4 ± 1.6	0.82 ± 0.21	−0.4 ± 0.51	0.11 ± 0.016
UV/NIR	28.2 ± 2.4	0.84 ± 0.37	−0.55 ± 0.47	0.11 ± 0.02
DUV/NIR	29.1 ± 1.7	0.62 ± 0.16	−0.41 ± 0.25	0.1 ± 0.016

a



b

Annealing	Oven	NIR	UV/NIR	DUV/NIR
Density (g/cm^3)	6.65	6.64	6.71	6.87

Fig. 18 **a** Measured XRR results for the Al-IZTO film annealed at 280 °C in air using oven and RTP (NIR, UV/NIR, and DUV/NIR. **b** Summary of calculated density of films after annealing [39]

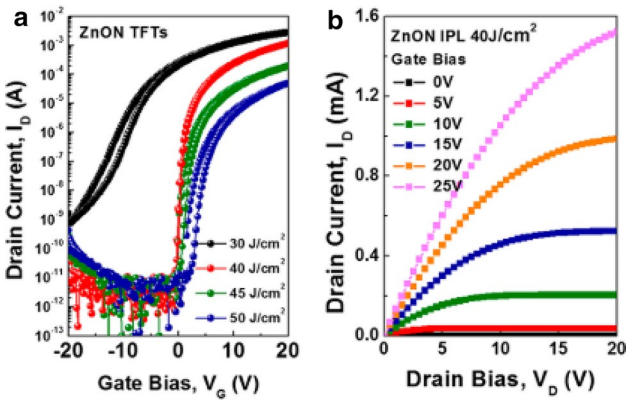


Fig. 20 **a** Transfer curves of ZnON TFTs with different IPL irradiation energies. **b** Output characteristics of ZnON TFTs with an IPL irradiation energy of 40 J/cm^2 [43]

Table 2 Device parameters (averages and standard variations) of ZnON TFTs with respect to IPL irradiation energy [43]

Energy (J/cm^2)	V_{th} (V)	μ_{sat} (cm^2/Vs)	SS (V/dec)	Hysteresis (V)
30	−14.70	45.65	1.13	0.98
40	0.98 ± 1.32	48.4 ± 1.33	0.26 ± 0.05	0.38 ± 0.03
45	1.02 ± 0.119	9.00 ± 1.25	0.52 ± 0.07	1.12 ± 0.25
50	4.20 ± 0.83	2.94 ± 0.84	0.64 ± 0.07	1.42 ± 0.12

negative voltage into the gate electrode. First of all, we could consider the thermal effect. There is a mechanism for changing V_{th} in the TS test. The lots of electrons in the valance band (E_V) are moves to the conduction band (E_C) through the trap states in the channel, when thermal energy from the temperature is affected to the channel layer [44]. Second, the PBS/NBS instability can be explained using 2 mechanisms, (1) trapping of electrons/holes in the gate dielectric or interface of channel/gate dielectric, or (2) the defects

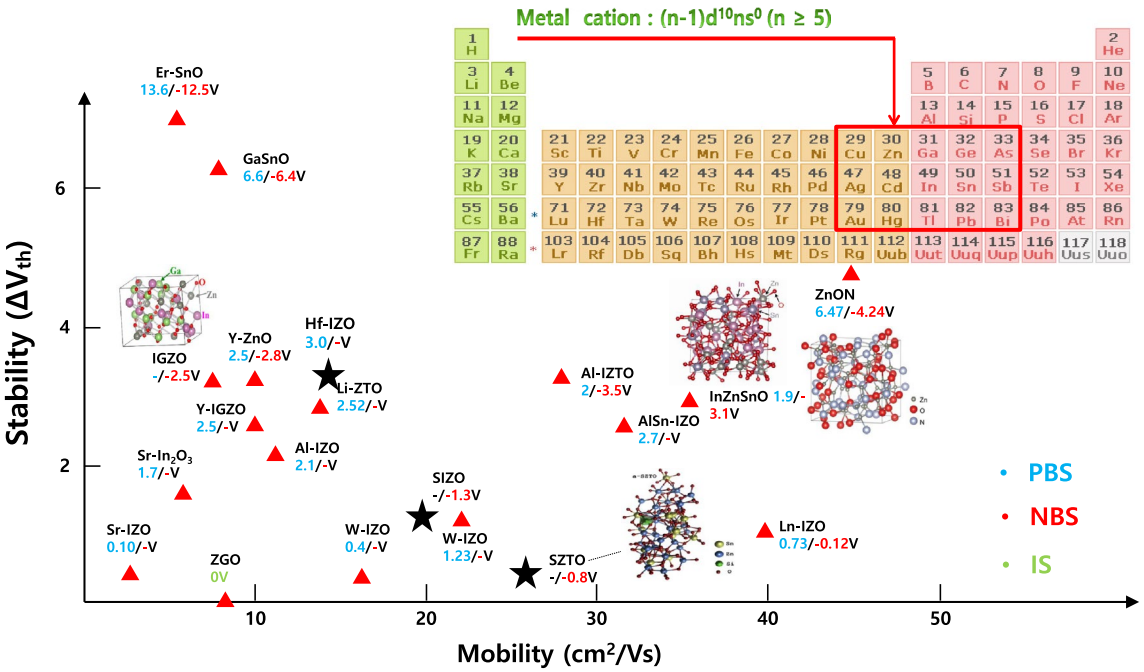


Fig. 21 The mobility versus stability with various AOS materials as of 2019

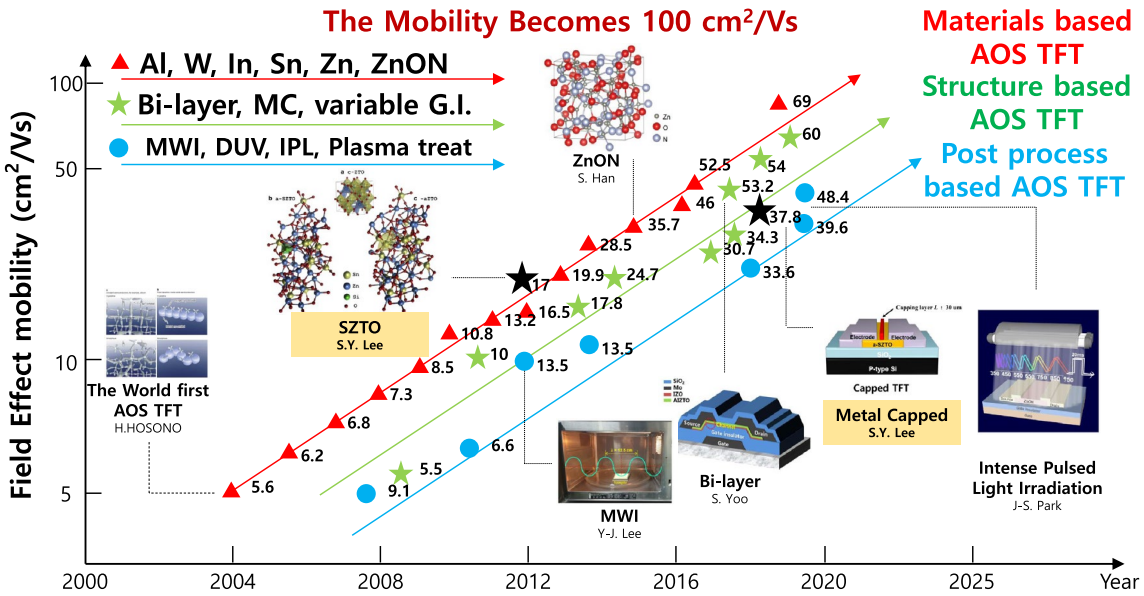


Fig. 22 Comprehensive review on the mobility development year by year with whole ways to increase the mobility

creation in the channel material [31, 45, 46]. Third, when the light illuminated to the channel material, the V_O in the deep level subgap states photo-ionized to the V_O^{2+} with 2 electrons [47, 48]. The stability is Mobility is important, but stability is also as important a parameter as mobility. In other words, two values of optimizing are continuously required. Figure 21 shows the mobility versus stability with various AOS materials as of 2019.

6 Conclusion

It is expected that AOS TFT will be the basis for next-generation industries such as displays, nanomaterials and cars of the future. In particular, high performance and design will be needed gradually as the specifications required by future applications are increasing. Thus, as discussed in this paper, the following process, which is how to achieve high mobility, should be discussed in more depth. In this paper, we investigated about various ways (materials, structures, post-processing) to achieve high mobility since 2004. Figure 22 shows comprehensive review on the development of μ_{FE} during the year by year with whole ways to increase the mobility.

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