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REGULAR PAPER

Full Adder Circuit Design with Novel Lower Complexity XOR Gate in QCA Technology

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Abstract
Quantum-dot Cellular Automata (QCA) is a new technology for designing digital circuits in Nanoscale. This technology utilizes quantum dots rather than diodes and transistors. QCA supplies a new computation platform, where binary data can be represented by polarized cells, which can define by the electron's configurations inside the cell. This paper explains QCA based combinational circuit design; such as half-adder and full-adder, by only one uniform layer of cells. The proposed design is accomplished using a novel XOR gate. The proposed XOR gate has a 50% speed improvement and 35% reduction in the number of cells needed over the best reported XOR. The results of QCADesigner software show that the proposed designs have less complexity and less power consumption than previous designs.

Keywords Nanotechnology · Quantum-dot cellular automata · XOR gate · Half adder · Full adder

1 Introduction

CMOS technology will reach the scaling limit in nanomaterial progress [1]. Consequently, alternative technology became the goal of numerous researchers. QCA is a new Nano technique that offers a new strategy for information transformation and computation. The main building units in QCA circuits are majority gate and inverter; where any QCA circuit can be constructed using only these two blocks with help of binary wire. Many digital circuits in QCA technology have been introduced in the literature, some of them focused on combinational circuits such as [2, 3] others focused on sequential and memory circuits as in [4–7]. Arithmetic circuits are considered a crucial tool in digital circuits due to their extensive used in many signal processing applications. The addition is one of the basic arithmetic operations. A full adder is the core of any arithmetic unit and is located on its critical path; therefore, its performance directly affects the entire system's performance. Many researchers have studied full adder by QCA, such as [8–15]. This implies that the performance enhancement of Adder will enhance the whole system's performance. Therefore, the design of QCA adder circuits with less complexity, shorter delays, and the lowest area, will be significantly required in the future [8, 16]. In this paper, a novel QCA-XOR gate is presented with minimum complexity. To demonstrate the operation of the proposed gate, it was used to design adder circuits, with the results compared to previous designs. Many programs introduced for QCA circuits evaluation such as [17] but QCADesigner tool is more common and it will be used for circuit simulation and evaluation in this work.

This paper will be arranged as follows: Sect. 2 preliminaries. Section 3 exclusive OR gate. The adder circuit is given in Sect. 4. Simulation results with comparisons will be detailed in Sect. 5. Finally, the conclusion is in Sect. 6.

2 Preliminaries

This section will give reviews of QCA basics.

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2.1 QCA Basics

2.1.1 QCA Cells

The fundamental QCA cell is illustrated in Fig. 1. QCA cell has a square shape consisting of four dots; where a pair of electrons is occupied within it diagonally, due to columbic repulsion. The injected electrons can transport through the tunnel between the adjacent dots. However, given the high potential between cells, it cannot tunnel between adjacent cells. Therefore, there are two arrangements of the QCA cell, depending on its polarization, as − 1 (logic "0") and + 1 (logic 1).

2.1.2 QCA Wire

QCA wire is comprised of fundamental cells that carry the input logical value to the output. The electrons interaction forces cells to take the same polarization of the neighbour cell, in other word each cell consider as a driver cell for the next one. This approach is applied in two configurations. The first is normal (or direct mode) while the second is rotated mode [18]. These two types are shown in Fig. 2.

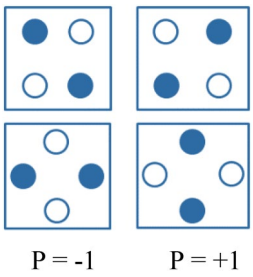

Fig. 1 Primary QCA cell

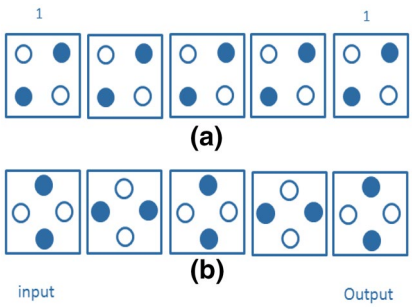

Fig. 2 QCA wire **a** direct mode, **b** rotated mode

2.1.3 QCA Gates

Three types of inverter presented in QCA are shown in Fig. 3.

Furthermore, a dominant gate in QCA circuits is majority gate; which has attracted the attention of many researchers [19–21]. Using this gate, the designer can make AND or OR gates by applying − 1 or + 1, respectively, on one of the majority inputs. Two forms of 3-input majority voters (Maj-3) are presented in Fig. 4. The Boolean equation of Maj-3 gate is given by Eq. 1 [22, 23].

$$M(A, B, C) = AB + BC + AC \tag{1}$$

The 3-inputs majority gate is expanded to many inputs majority voter with different QCA structures and layouts as in [8, 24, 25].

2.1.4 QCA Clock

Clocking is an essential part of QCA circuits due to following reasons: synchronization, power compensation, and controlling the direction of data flow. Furthermore, it gives the power to stimulate the circuit. The clock signal controls the potential barriers between dots inside the cell to achieve synchronization. The polarization of the cell is still undetermined; as long as the cell has low potential barriers, the electrons will then easily move between points. The electrons get them localized whenever the potential barriers rise to their highest value. At this point, the polarization of the cell will be determined. The clock signal contains four clock zones and every zone contains four-phases, starting

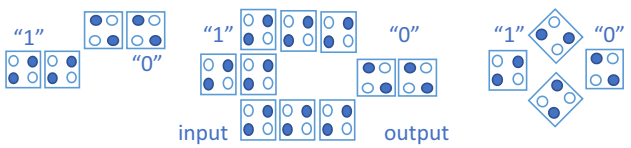

Fig. 3 QCA inverter forms

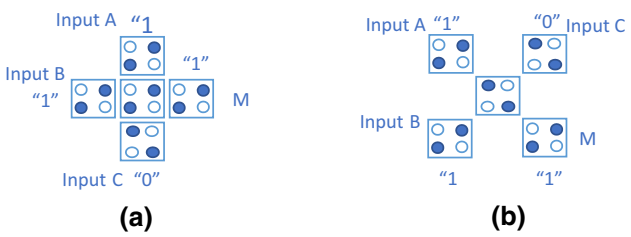

Fig. 4 Three inputs majority gate forms

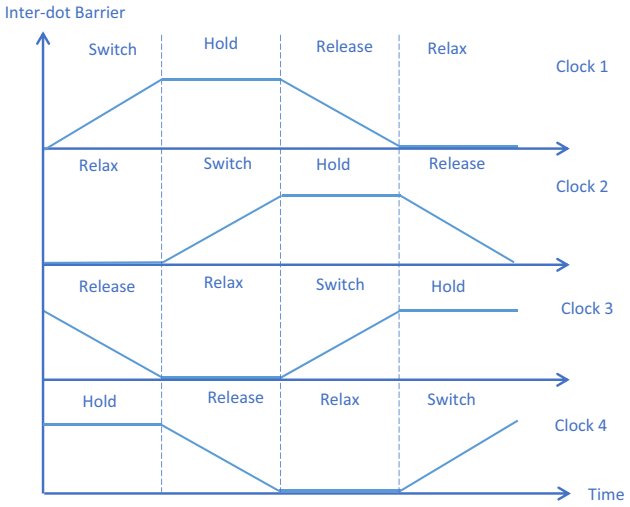

Fig. 5 Clock zones signal

from switch phase then hold, release, and relax (as illustrated in Fig. 5) [26].

3 The Exclusive-OR (XOR) Gate

XOR gate is a logic circuit that gives high at the output when the number of high inputs is odd. The Boolean equation of XOR is illustrated in Eq. 2.

$$XOR_{A,B} = A \cdot \bar{B} + \bar{A} \cdot B \tag{2}$$

The XOR logic diagram and its symbol are shown in Fig. 6.

3.1 The Proposed XOR Layout

The XOR gate is the brick unit of many digital circuits, such as arithmetic circuits [27] and parity bit generator circuit [28]. There are several XOR layouts presented previously in QCA technology [29–35] but the goal was to minimize the number of majority gate or inverter used by re-forming the XOR equation. While some of them were design based on the inherent capability of QCA. An example of the conventional XOR structures presented previously is illustrated in Fig. 7a, b; while the proposed XOR layout is illustrated in Fig. 7c.

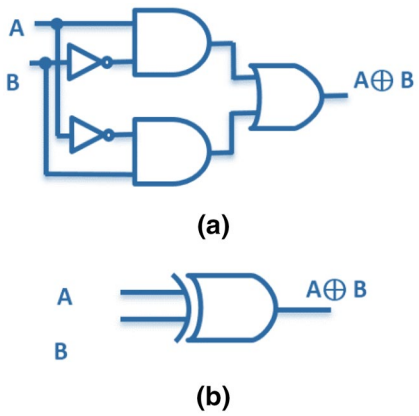

Fig. 6 XOR gate **a** logic circuit diagram, **b** symbol

3.1.1 Physical Verification

The proposed structure verified physically as illustrated in Fig. 11 and Table 1. For the two adjacent cells (i, j), the electrostatic energy $E^k_{i,j}$ can be calculated using Eq. 3.

$$E_{Total} = \sum_{i,j} \frac{q_i q_j}{4\pi\varepsilon_0\varepsilon_r \left| r_{i,j} \right|} \tag{3}$$

where ε_0: free space permittivity; ε_r: relative permittivity; q: the charge of electron inside dot; |ri − rjl: the space between the two dots.

The most stable orientation defined by the configuration have lower energy in a certain input.

The electrostatic energy or called "kink energy" E^k between two cells can be calculated by letting one cell in its original state and switching the other in two contradictory polarization states and then comparing the two results and selecting the smaller one. This was done for many uncertain polarization cells (c1, c2, c3 and c4) as in Fig. 8 before calculating the polarization of the output cell for the proposed gate and the results were the polarization of c1 = 1, c2 = 1, c3 = 0 and c4 = 0. If the input pattern (A, B) = (1, 0), the calculation of the total electrostatic energy at dot p (named Up) for the output cell is shown below: $Up = \frac{K}{D1} + \frac{K}{D2} + \frac{K}{D3} + \frac{K}{D4} + \frac{K}{D5} + \frac{K}{D6} + \frac{K}{D7} + \frac{K}{D8} + \frac{K}{D9} + \frac{K}{D10} + \frac{K}{D11} + \frac{K}{D12} + \frac{K}{D13} + \frac{K}{D14} + \frac{K}{D15} + \frac{K}{D16} = \frac{K}{50.61} + \frac{K}{50.61} + \frac{K}{54.78} + \frac{K}{61} + \frac{K}{40} + \frac{K}{32.28} + \frac{K}{36.89} + \frac{K}{41.48} + \frac{K}{22.83} + \frac{K}{22.83} + \frac{K}{21.93} + \frac{K}{11} + \frac{K}{40} + \frac{K}{32.28} + \frac{K}{44.72} + \frac{K}{42.45} = 11.7 \times 10^{-20}\text{J}$ where $k = \frac{q^2}{4\pi\epsilon_0\epsilon_r} = 23.04 \times 10^{-20}$ and D is the distance between

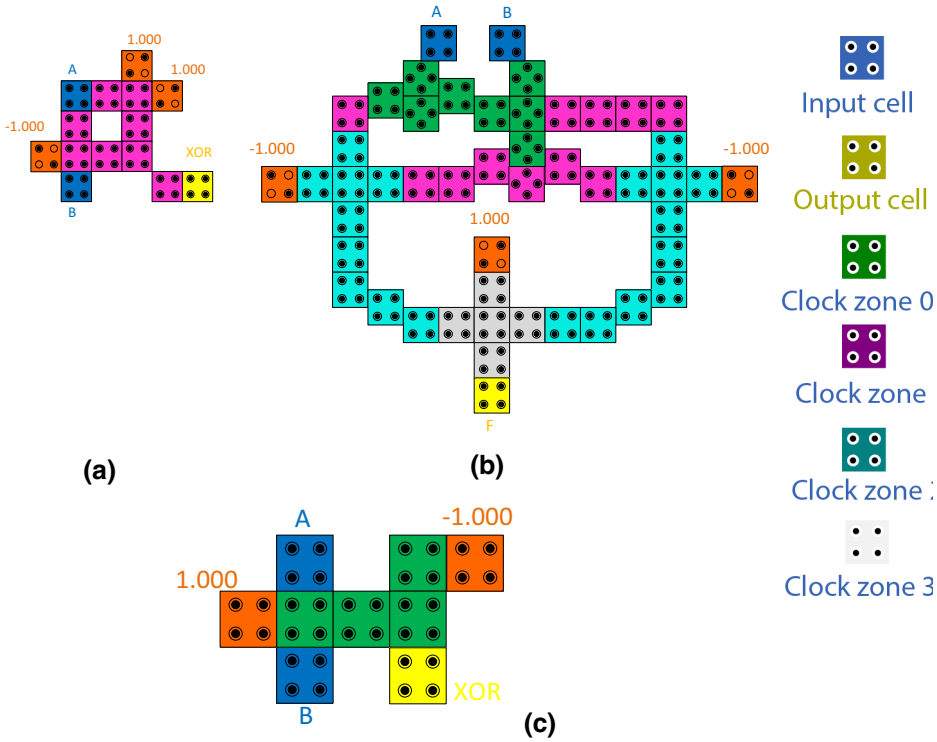

Fig. 7 2-Input XOR gate **a** presented in [36], **b** presented in [37], **c** proposed design

Table 1 The proposed gate validation

Cell	Up	Uq	Ur	Us	Result	Stable position (lower energy required)	Cell polarization
	$\times 10^{-20}$ J						
Output	11.7	10.3	9.33	8.5	$(q+r)<(p+s)$	$q+r$	+1 (Logic 1)

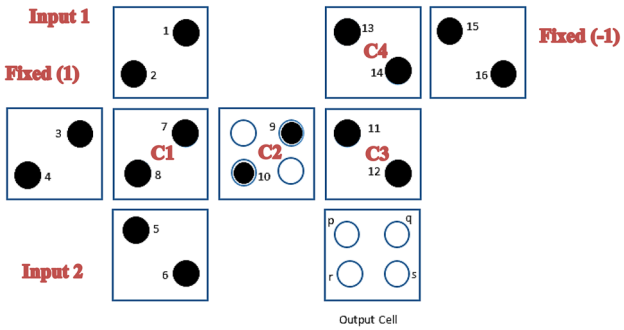

Fig. 8 proposed configuration to analysis the proposed XOR gate

two dots.The proposed XOR is verified by simulating it with QCADesigner software and the results are given in Sect. 5.

3.1.2 Power Consumption Analysis

The estimation of the dissipated power for the proposed gate can be defined using the most common tool called QCAPro. This tool has the ability to manipulate large circuit because it uses fast approximation and it can expect the losses of power in non-adiabatic switching.

The analysis of power dissipation at different tunneling energy levels (0.5 Ek, 1 Ek and 1.5 Ek) for the proposed gate in comparison with previously counterparts is shown in Table 2. The power dissipation map for proposed gate at 0.5 Ek is illustrated in Fig. 9.

4 Adder Circuits

4.1 Half Adder

Half adder responsible for adding two logical inputs and provides two outputs sum and carry, if input variables are A and B. The sum and carry of these two variables can be calculated by Eq. 4.

$$\begin{aligned} \text{Sum} &= A \oplus B \\ \text{Carry} &= AB \end{aligned} \tag{4}$$

Half adder logic circuit is illustrated in Fig. 10.

Table 2 Power dissipation comparison at 2 K for many XOR gates

Circuit presented in	Average of leakage energy dissipation (meV)			Average of switching energy dissipation (meV)			Total energy consumption (meV)		
	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek	0.5 Ek	1 Ek	1.5 Ek
[38]	14.82	40.32	68.10	32.17	26.23	21.41	46.99	66.54	89.51
[39]	11.51	31.91	54.69	35.78	30.48	25.66	47.28	62.39	80.34
[40]	11.64	31.85	53.68	27.42	21.78	17.40	39.06	53.63	71.08
[41]	10.78	28.57	48.15	25.43	21.71	18.4	36.20	50.28	66.58
[36]	5.58	13.99	23.90	5.55	5.1	4.56	11.13	19.09	27.46
Proposed	2.69	7.43	12.72	8.16	6.94	5.87	10.85	14.37	18.59

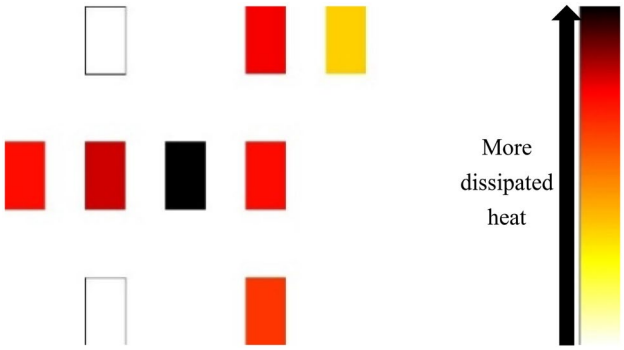

Fig. 9 The power dissipation map for the proposed 2-input XOR gate with the level 0.5 Ek tunnelling energy at 2-Kelvin temperature

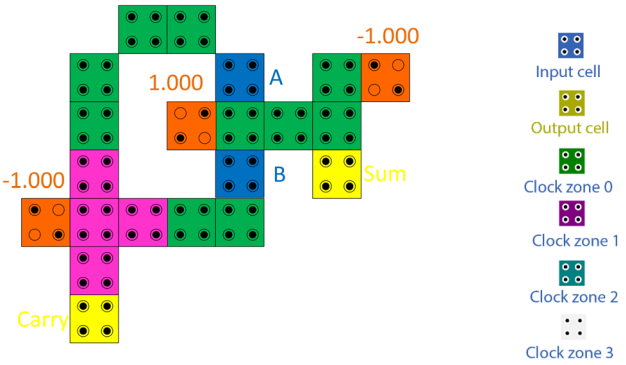

Fig. 11 Proposed QCA-half adder

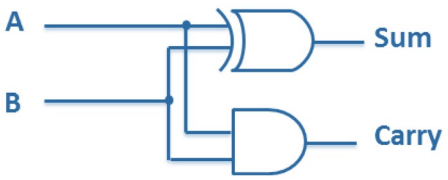

Fig. 10 Half adder logic diagram

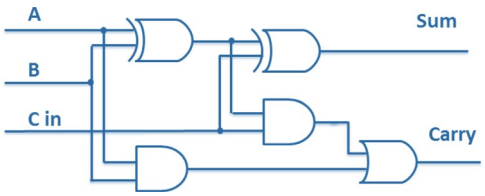

Fig. 12 Full adder logic diagram

On the other hand, the full adder adds three logical variables and provides two outputs, sum and carry. If the input variables are A, B, and C_{in}, the two outputs can be found using Eq. 5.

$$\begin{aligned} \text{Sum} &= (\text{A})\text{XOR}(\text{B})\text{XOR}\left(\text{C}_{\text{in}}\right) \\ \text{Carry} &= (\text{AB})\ \text{OR}\ \left(\text{B}\ \text{C}_{\text{in}}\right)\ \text{OR}\ \left(\text{C}_{\text{in}}\text{A}\right) \end{aligned} \tag{5}$$

By following the logic circuit previously given in Fig. 10, the half adder can be easily designed with proposed XOR gate as illustrated in Fig. 11.

4.2 Full Adder

The full adder logic circuit is illustrated in Fig. 12.

Note: the carry equation is the same as the Maj-3 equation, as previously mentioned in Eq. 1. Therefore, the full adder circuit can be implemented as shown in Fig. 13. Another form of full adder logical representation that utilizes multi-input majority function and its reliability is studied in [42].

The full adder design approach illustrated in Fig. 13b is adopted in most of previous literatures because it produces more efficient circuit with less complexity (number of cells and circuit layout area) and latency (number of required clock phases to produce output) as the circuits reported in [14, 43, 44] as shown in Fig. 14a, b. On the other hand, the design approach shown in Fig. 13a is not commonly used in QCA circuitry due to the high complexity of the produced circuit and the designs reported in [26, 45]. The proposed XOR in this work solve this issue. It was used to design full adder circuit with QCA technology as shown in Fig. 14c.

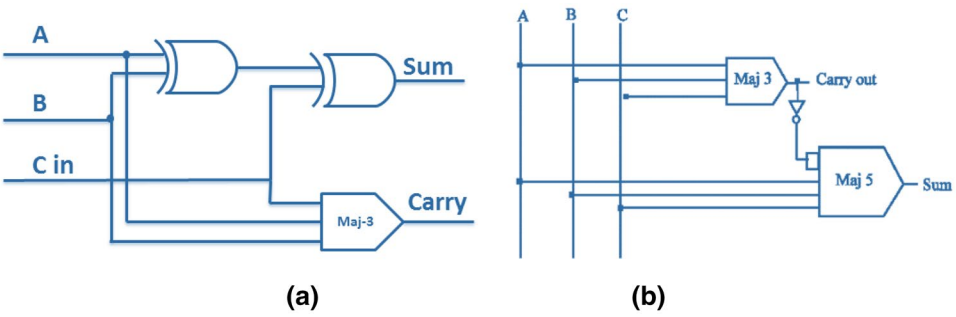

Fig. 13 Full adder logic circuit **a** based on Maj-3, **b** based on Maj-5 [24]

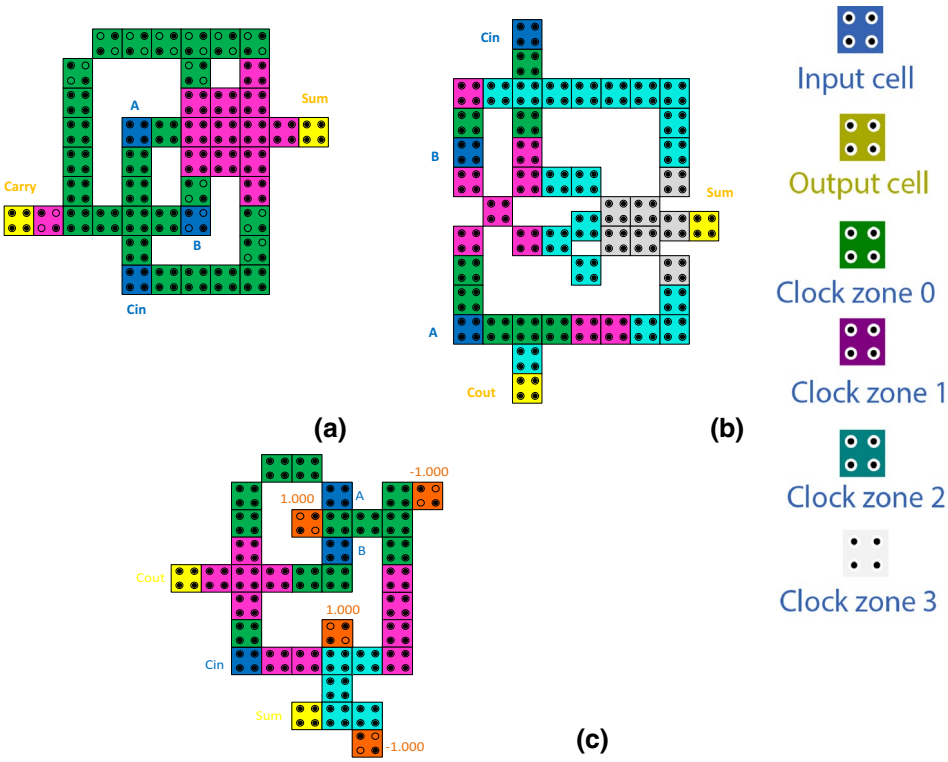

Fig. 14 QCA-full adder **a** presented in [44], **b** presented in [14], **c** proposed structure

5 Simulation Results

In this work, QCADesigner tool V 2.0.3 [46] is used to simulate the proposed circuits with the simulation parameters shown in Fig. 15. The proposed XOR in Fig. 7c produces the output waveform shown in Fig. 16 and it is clear from the output that the proposed gate shows error-free operation for all input possibilities. From noticing the polarization of the output waveform, it can be concluded that the proposed gate has acceptable robustness. The proposed half adder and full adder circuits are simulated under the same conditions and produced the output waveforms shown in Figs. 17 and 18 respectively. In both circuits, the output was correct for all input states.

The proposed gate is superior in terms of area, number of cells, latency when compared with previous reported designs. Table 3 gives the comparison results. Furthermore, the proposed gate makes a reduction in delay time to 50% compared to best previously reported; where it can be implemented in a ¼ clock cycle of the clock signal defined in Fig. 5. The proposed design requires only 9 cells; while the best previous design required 14 cells. Another important aspect of the proposed design is that it does not require wire crossover.

The results of the comparison for the proposed half adder, with existing designs, are shown in Table 4. From this table, it is obvious that the proposed structure is an optimal design in comparison with previously counterparts. The proposed

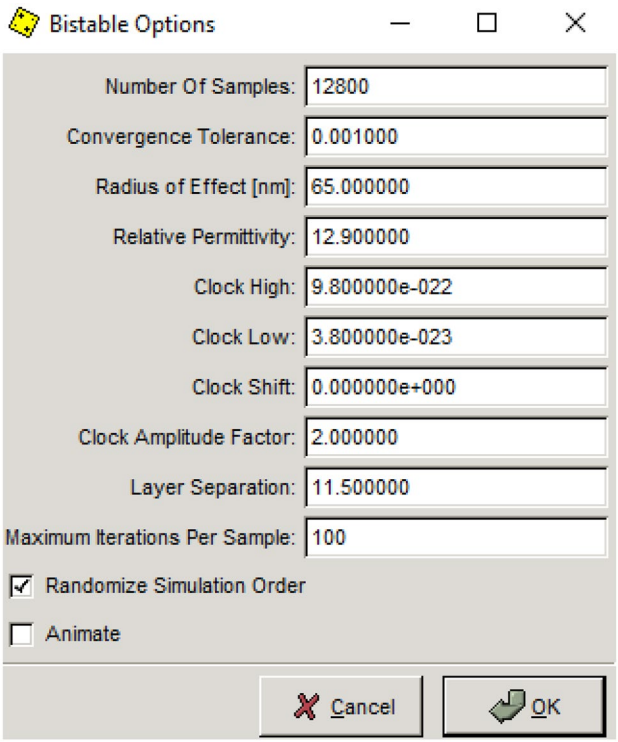

Fig. 15 QCADesigner simulation parameters

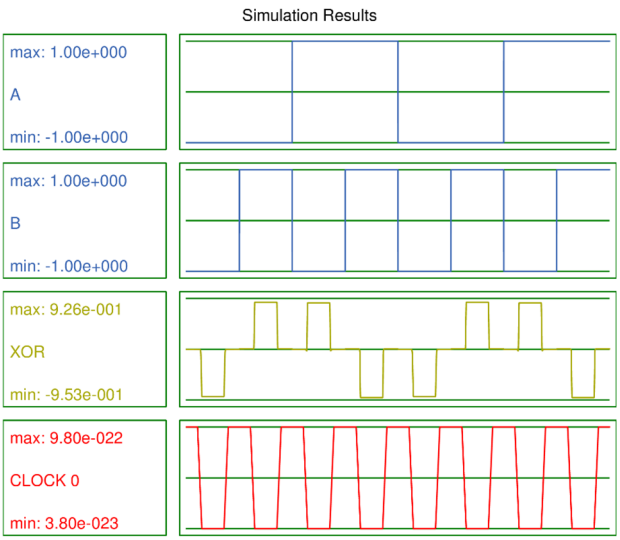

Fig. 16 Proposed XOR simulation result

half adder is crossover free, with minimum cell number and area. Table 5 details the comparison results of the full adder with existing structures. It is clear from this table that the proposed full adder is distinguished in terms of complexity; where it was implemented using only 39 cells, by improving 15% from the nearest competitor structure presented in [43].

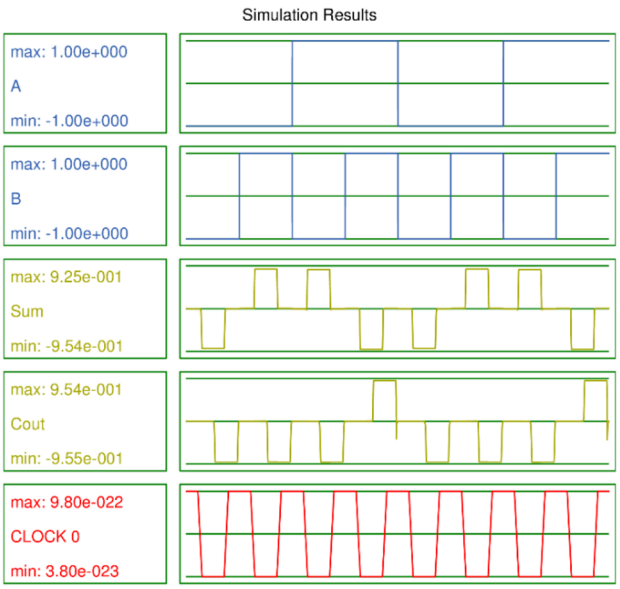

Fig. 17 Proposed half adder simulation result

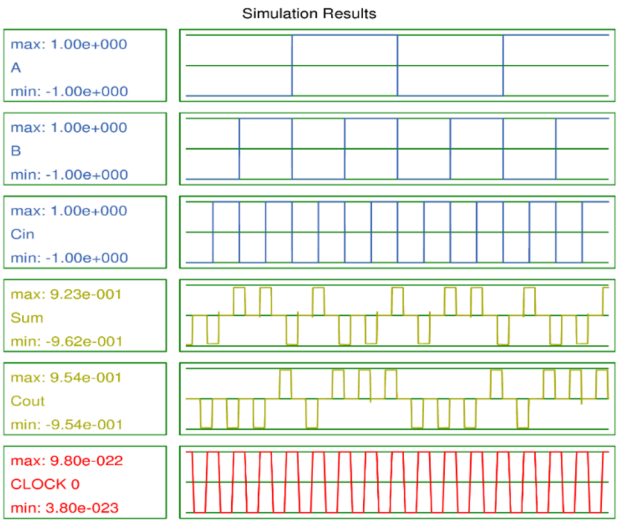

Fig. 18 Proposed full adder simulation result

6 Conclusions

In this paper, a new single layer Exclusive-OR gate design is introduced with QCA technology. The proposed design has a 50% speed improvement and a 35% reduction in the number of cells needed over the best reported XOR. The presented gate is used to design superior half and full adders with a very noticeable reduction in the circuit layout area and number of cells. The proposed XOR gate shows a noticeable reduction in the power dissipation compared to

Table 3 Comparison of proposed XOR with existing structures

XOR	Area (μm^2)	No. of cells	Crossover type	Latency
[47]	0.22	121	Coplanar	1
[48]	0.07	64	Multilayer	1
[49]	0.06	49	Multilayer	1
[50]	0.06	54	Not required	3/4
[29] Fig. 8b	0.08	84	Multilayer	1
[29] Fig. 8c	0.07	64	Multilayer	1
[29] Fig. 9	0.06	34	Not required	1 1/4
[29] Fig. 10	0.07	54	Not required	1 1/4
[29] Fig. 11	0.08	52	Not required	2 1/4
[29] Fig. 12	0.09	52	Not required	2 1/4
[29] Fig. 13	0.06	48	Not required	3/4
[29] Fig. 14	0.07	54	Not required	1 1/4
[29] Fig. 15	0.05	42	Not required	3/4
[51] Fig. 10	0.09	88	Multilayer	1
[51] Fig. 11a	0.07	44	Not required	1
[51] Fig. 11b	0.09	55	Not required	2
[51] Fig. 11c	0.09	62	Not required	1 1/2
[52]	0.17	115	Coplanar	1 1/2
[53]	0.04	40	Coplanar	3/4
[54]	0.08	51	Coplanar	1 1/4
[55] Fig. 9a	0.16	51	Coplanar	1 1/4
[55] Fig. 9b	0.09	30	Not required	1
[30]	0.07	49	Not required	2
[56]	0.05	45	Coplanar	1
[37]	0.05	47	Coplanar	1
[57] Fig. 8b	NA	71	Not required	1 3/4
[57] Fig. 9b	NA	72	Not required	1 1/2
[34]	0.04	32	Not required	3/4
[58]	0.09	60	Coplanar	1 1/2
[59]	0.08	54	Coplanar	1 1/2
[32]	0.03	29	Not required	3/4
[41]	0.02	28	Not required	3/4
[60]	0.01	14	Not required	1/2
Proposed	0.01	9	Not required	1/4

Table 4 Comparison of proposed half adder with existing structures

Half adder	Area (μm^2)	No. of cells	Crossover type	Latency
[61]	0.08	77	Multilayer	1
[50]	NA	61	Not required	¾
[54]	NA	65	Coplanar	1 ¼
[30]	0.08	62	Not required	2
[34]	0.05	34	Not required	¾
[38]	0.05	44	Not required	1
Proposed	0.02	21	Not required	1/2

Table 5 Proposed full adder compared to previously reported structures

Full adder	Area (μm^2)	No. of cells	Crossover type	Latency
[61] Fig. 11	0.2	192	Multilayer	2
[61] Fig. 13	0.114	122	Coplanar	1
[61] Fig. 14	0.1	98	Multilayer	1
[26]	0.15	120	Coplanar	2 ½
[47]	0.04	124	Multilayer	1
[54]	0.28	150	Coplanar	2 ¼
[34]	0.14	105	Not required	1 ¼
[14]	0.04	49	Coplanar	1
[15]	0.28	228	Not required	1 ¾
[45]	0.37	221	Coplanar	2
[43]	0.04	48	Not required	¾
[43]	0.04	46	Not required	¾
Proposed	0.04	37	Not required	¾

the previous designs. The reduction in the complexity of the proposed designs is very encouraging to adapt it to other circuit designs.

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