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REGULAR PAPER

# New Symmetric and Hybrid Multilevel Inverter Topology Employed in Solar Energy Systems

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**Abstract**
In this paper, novel symmetric and hybrid topologies have been proposed for single phase multilevel inverter structures based on a new basic unit. The proposed topologies can be employed in solar energy systems. The main focus of this paper is to reduce the overall cost as well as to increase the efficiency of the multilevel inverters. To generate greater number of voltage levels, the basic units have been cascaded with each other to make extended topology. Different comparisons such as the number of power switches and percentage of THD against the number of voltage levels have been drawn to illustrate the advantages of the proposed topologies. To validate the performance of the proposed topologies, a 20 kW PV arrays based on fifteen-level hybrid inverter has been simulated through MATLAB/Simulink software.

**Keywords** Multilevel inverter · Ladder structure · Hybrid topology · DC–AC converter

**Abbreviations**

| | |
|---|---|
| kW | Kilowatt |
| kVAr | Kilovar |
| PV | Photovoltaic |
| CHB-MLI | Cascade H-bridge inverter |
| IGBT | Insulated gate bipolar transistor |
| NPC | Neutral point clamped |
| FC | Flying capacitor |
| CHB | Cascaded H-bridge |
| qZSDCc | Quasi Z-source DC–DC converter |
| THD | Total harmonic distortion |
| Rms | Root mean square |
| FFT | Fast Fourier transform |

## 1 Introduction

Multilevel DC–AC power conversion systems were first introduced in 1975 by Baker [1]. Multilevel inverters have several advantages over two-level inverters: the former exhibit high efficiency, high power quality, low voltage distortion, less common mode noise generation, less dv/dt lower harmonic components, better electromagnetic compatibility and the ability to operate under low switching frequency [2–8]. Multilevel inverters have been widely used in various industrial applications as PV systems [9, 10], flexible AC transmission line systems [11–13] and electrical drives [14–16]. The primary purpose of designing a multilevel inverter is to generate a large number of desired output voltage levels using fewer power electronic components. There are mainly three conventional multilevel inverters: The CHB-MLI [1], the NPC multilevel inverter [17] and the FC multilevel inverter [2, 18, 19]. Although the introduced conventional multilevel inverters are able to provide large number of voltage levels with best quality, each of them exhibit certain drawbacks, which restrict their applications. The main drawbacks of these topologies are as follows:

a. CHB-MLI: it requires a large number of power switches and gate drivers as well as isolated DC voltage sources.
b. NPC inverter: it uses a large number of clamping diodes and voltage unbalancing in DC-link capacitors in high voltage levels.
c. FC multilevel inverter: complex control mechanism for balancing the floating capacitors; they also use large number of flying capacitors.

In this paper, new symmetric and hybrid multilevel inverter configurations have been introduced with a new basic unit topology. Use of fewer IGBTs, diodes and gate driver

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circuits are the main advantages of the proposed topology in comparison with other topologies. The proposed multilevel inverter topology has been extended for application in PV systems. Moreover, the simulation tests have been done for a 20 kW PV system based on proposed fifteen-level inverter to demonstrate the validity of the proposed topology.

Section 2 explains the proposed basic and hybrid structures. Detailed comparisons between topologies are discussed in Sect. 3. Section 4 illustrates the simulation results.

## 2 Proposed Topologies

### 2.1 First Proposed Topology

Figure 1 illustrates the proposed multilevel inverter topology with a new basic unit. The proposed structure consists of three stages. The first stage includes a PV panel and a qZSDCc. The qZSDCc is employed to increase the output voltage and maximum power tracking of the PV panel [20, 21]. The second stage is the structure of the proposed basic unit. The third stage includes an H-bridge inverter which is used to produce positive and negative voltage levels. The proposed basic unit inverter consists of five power switches and three DC-link capacitors to generate different voltage levels.

To analyze the proposed configuration, in the first stage, the output voltage of qZSDCc is increased to $V_b$ according to the following equation [20, 21]:

$$V_b = \frac{1}{1-2D} Vpv \tag{1}$$

where $D$ is the duty cycle of the converter. The increased voltage $V_b$is then divided into three equal parts as $V_c = \frac{V_b}{3}$ which then is used to generate different voltage levels in the proposed inverter.

In the second and third stage, to generate different voltage levels, different combinations of power switches states

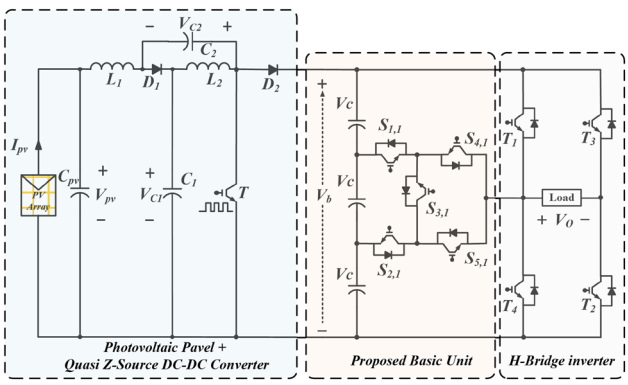


**Fig. 1** The proposed multilevel inverter

exist. Figure 2d–g indicates one of these combinations. In these figures, the pale gray paths indicate the current flow to generate seven different voltage levels. The output voltage levels of multilevel inverter are 0, $-V_C$, $+V_C$, $+2V_C$, $-2V_C$, $+3V_C$ and $-3V_C$. For example, to generate $+V_C$, one of the switching combinations is turning on the power switches $S_{2,1}$, $S_{3,1}$, $S_{4,1}$, and $T_2$. In this mode, when the switches turn on, the antiparallel diodes of power switches $S_{1,1}$ and $S_{5,1}$ get reverse biased. In this mode, the current flows through $V_c$, $S_{2,1}$, $S_{3,1}$, $S_{4,1}$, load, and $T_2$ and the voltage of load becomes $V_o = V_c$. It is important to note that to generate other voltage levels, the same analysis exists.

One of the most important targets in multilevel inverter topologies is to design a structure that decreases the overall cost and volume of the converter. The overall cost and volume of the converter have a near relevance to the number of power electronic elements such as power switches and gate diver circuits. To generate more number of voltage levels, the proposed basic unit can be extended by cascading the basic units. Figure 3 shows the developed proposed topology. In the proposed developed topology, if $n$ indicates the number of basic units, then the number of voltage levels is determined by the following equation:

$$N_{level} = 4n + 3 \tag{2}$$

Moreover, considering the developed topology in Fig. 3, the number of power IGBTs is calculated by the following equation:

$$N_{IGBT} = 5n + 4 \tag{3}$$

By substituting $n$ from (2) in (3), the number of power IGBTs is calculated as:

$$N_{IGBT} = \frac{5N_{level} + 1}{4} \tag{4}$$

### 2.2 Second Proposed Topology

Hybrid topology can be employed to generate greater number of voltage levels with fewer power electronic elements. In order to achieve hybrid topology, a three-level inverter is cascaded with the proposed developed topology, which increases the number of voltage levels. Figure 4 shows the proposed hybrid multilevel inverter.

In the proposed hybrid structure, we choose the magnitude of $E$ equal with $\frac{V_c}{2}$. Therefore, we can calculate the number of voltage levels as in the following equation:

$$N_{level} = 8n + 7 \tag{5}$$

According to the previous subsection 2.1, the number of power IGBTs is also calculated by:

$$N_{IGBT} = 5n + 8 \tag{6}$$

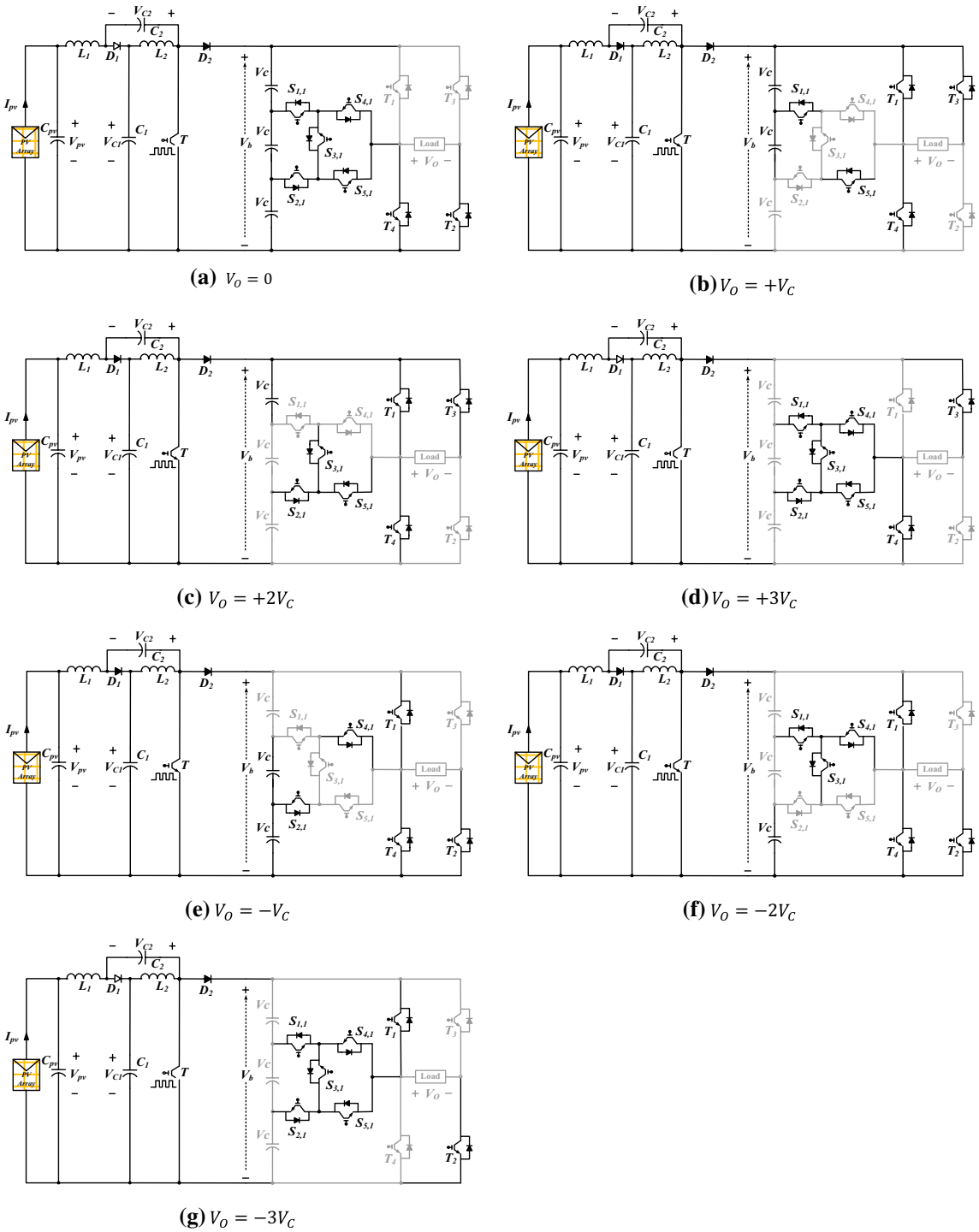


**Fig. 2** Different combination of the switching states to generate different voltage levels. **a** $V_O$=0, **b** $V_O$=+$V_C$, **c** $V_O = +2V_C$, **d** $V_O$=+3$V_C$, **e** $V_O = -V_C$, **f** $V_O$=−2$V_C$, **g** $V_O$=−3$V_C$

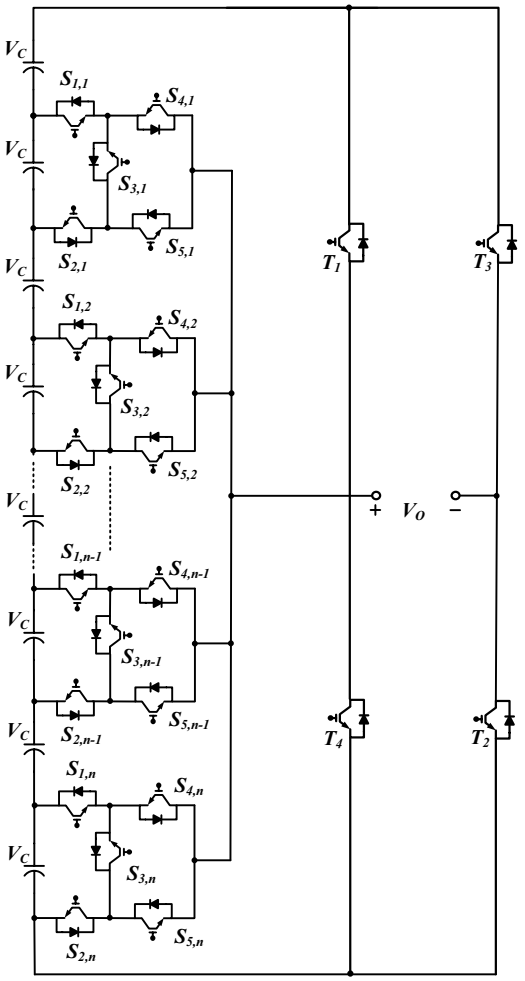


**Fig. 3** Developed proposed topology

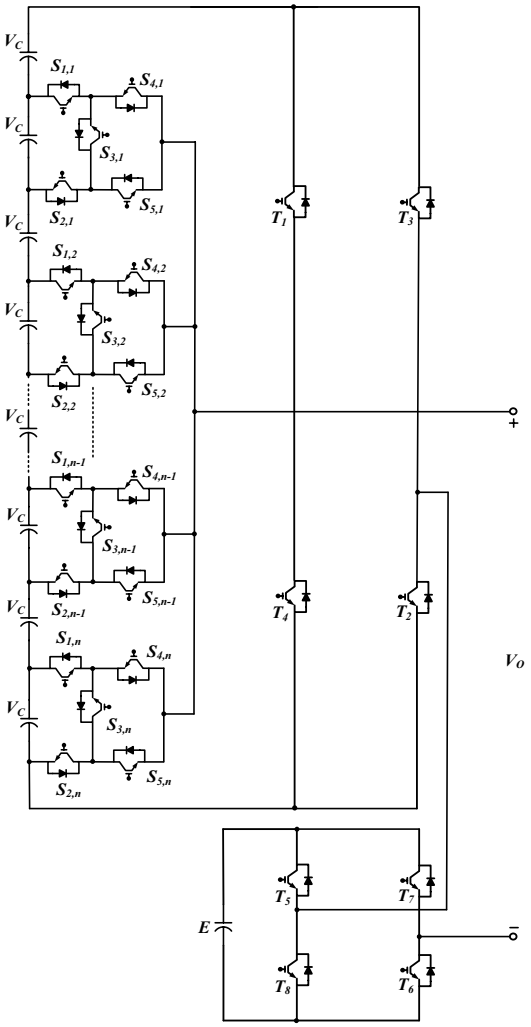


**Fig. 4** The proposed hybrid topology

By combining (5) and (6), the number of power IGBTs versus the number of voltage levels is determined as follows:

$$N_{IGBT} = \frac{5N_{level} + 24}{8} \tag{7}$$

## 3 Comparisons

To illustrate the advantages of the proposed topology, we compared it with the other traditional topologies. Figure 5 illustrates the number of power IGBTs against the number of voltage levels. As can be seen, the first and second proposed topologies use fewer power IGBTs as compared to NPC, FC and CHB inverters.

One of the other important factors in multilevel inverter topologies is the percentage of THD against the number of used power switches. Figure 6 shows the percentage of THD against the used power IGBTs. It is clear that the first and second proposed topologies have fewer power switches in

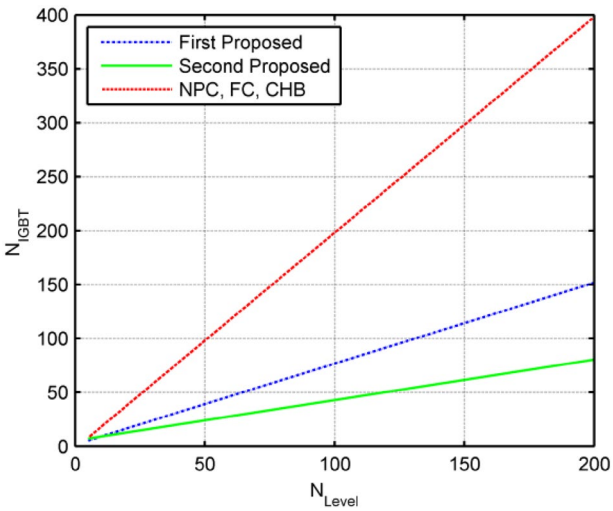


**Fig. 5** The number of IGBTs versus the number of voltage levels

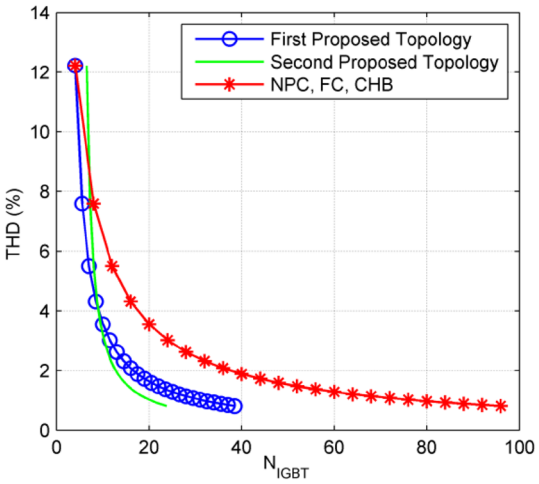


**Fig. 6** The percentage of THD of output voltage versus the number of IGBTs

**Table 1** The used parameters in the simulation

| | |
|---|---|
| $C_{pv}$ | 3000 µF |
| $C_1 = C_2$ | 220 µF |
| $L_1 = L_2$ | 2 mF |
| $C$ | 2000 µF |
| $f_{sw}$ | 30 kHz |
| $E$ | 200 V |
| $f_o$ | 50 Hz |
| Resistive load | 40 Ω |
| Inductive load | 70 mH |

comparison to conventional topologies in the same THD. It is important to note that the low THD with fewer power electronic components reduces the total cost of the converter.

## 4 Simulation Results

To verify the operation of the proposed multilevel inverter, a 20 kW PV system based on the proposed hybrid fifteen-level inverter has been simulated through MATLAB/Simulink software. The fifteen-level inverter includes 19 power IGBTs and 7 DC-link capacitors. The parameters of the simulated system are listed in Table 1. In this simulation, a prototype of KC200GT PV panel with 10 identical modules connected in parallel and 10 in series has been selected and its parameters are listed in [21, 22]. Also, the insolation and environment temperature have been chosen as 1000 w/M$^2$ and 25 °C, respectively.

Figure 7 shows the output voltage, output current and output power of the PV panels with modules connected in series and in parallel. As PV panels operate in standard environmental conditions and each PV panel has 200.143 W output power, 10 number of serried PV panels can produce 20 kW output power. Further, at maximum power point tracking, each PV panel has the maximum voltage and maximum current equal to 26.3 V and 7.61 A, respectively. Further, PV panels with 10 modules connected in series and 10 in parallel can produce 263 V output voltage and 76.1 A output current. According to the simulation consequences, these values have been shown in Fig. 7.

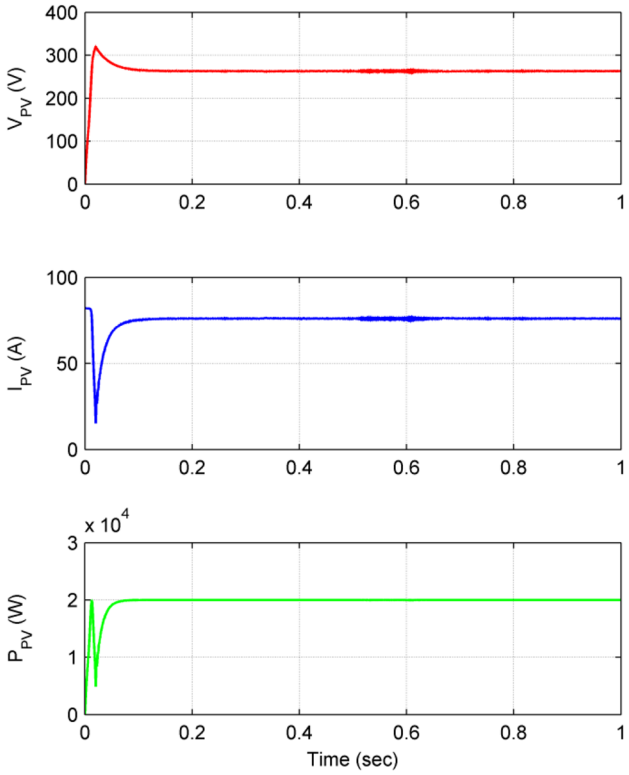


**Fig. 7** The output voltage, current and power of the PV arrays

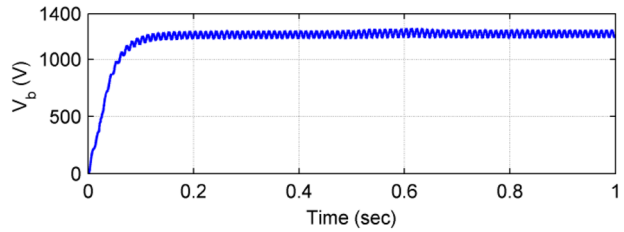


**Fig. 8** The output voltage of the quasi Z-source DC–DC converter

Figure 8 shows the simulation results for the output voltage of the qZSDCc. The increased amount of increased output voltage of the converter is almost 1200 V. This value divided into three and therefore, each input capacitor of the inverter becomes 400 V.

The active and reactive power of the load has been shown in Fig. 9. In this simulation, the converter operates

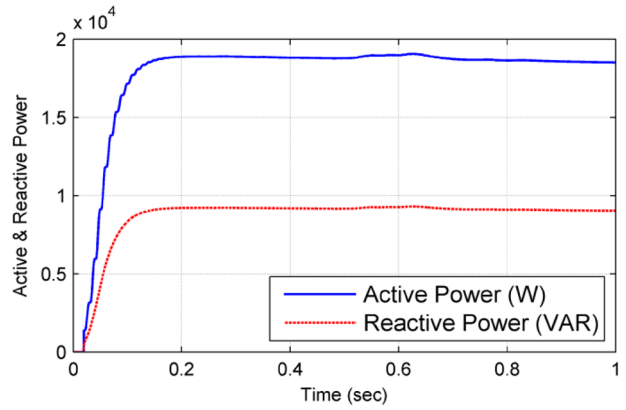


**Fig. 9** Active and reactive power of the load

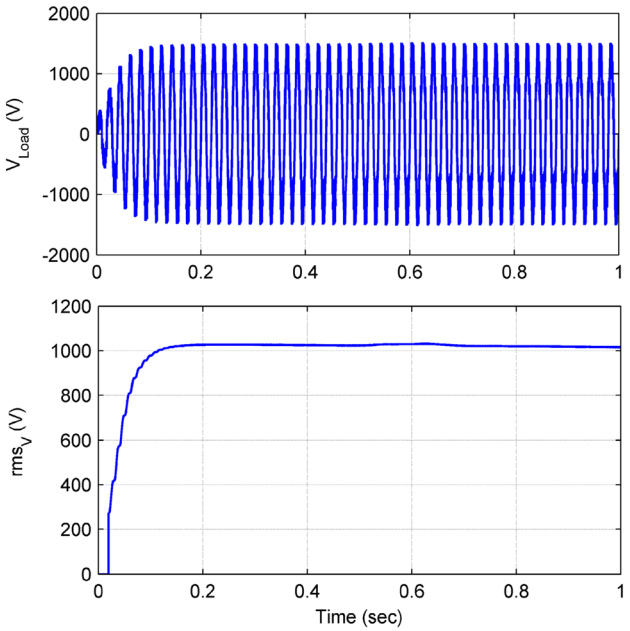


**Fig. 10** Load voltage and its rms waveform

in nominal conditions. Therefore, the amount of active and reactive power of the load which supplied by PV arrays and battery are 18 kW and 0.8 kVAr, respectively.

Figures 10 and 11 show the simulation results for the load voltage. As can be seen from Fig. 10, the rms value of the output voltage is almost 1100 V. Moreover, the FFT analysis shows that the THD of the load voltage is 8.93%.

Figures 12 and 13 illustrate the simulation results for the load current. According to these figures, the rms value of the output current is almost 20 A and the THD of the load is 1.48%. The load current is similar to the sinusoidal

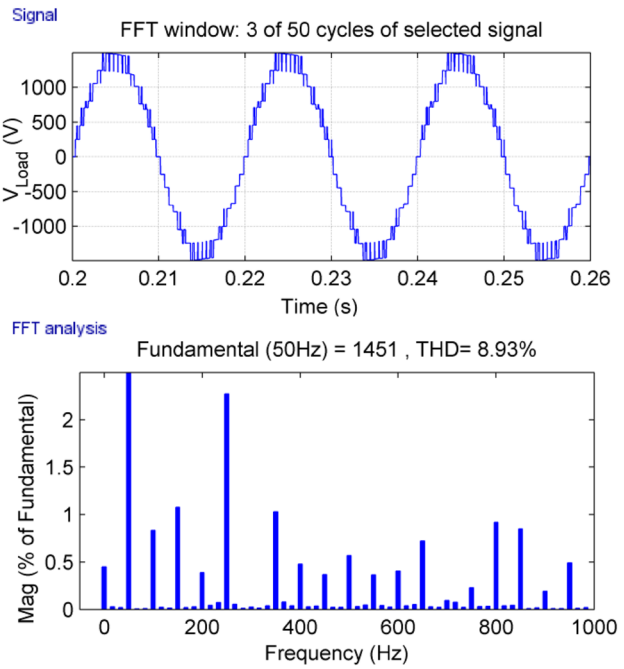


**Fig. 11** Output voltage waveform with its FFT analysis (THD = 8.93%)

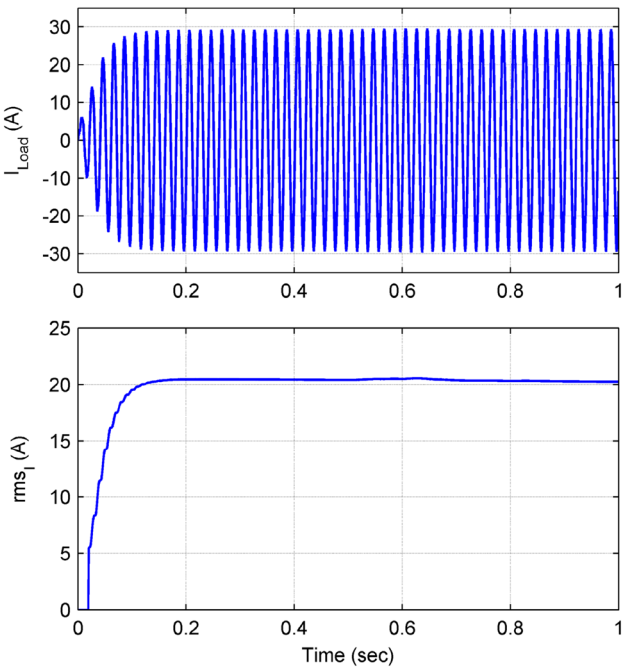


**Fig. 12** Load current and its rms waveform

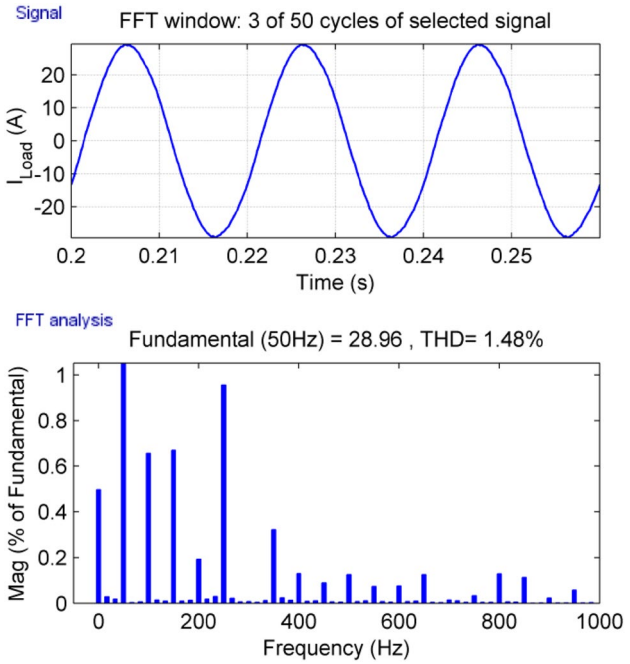


**Fig. 13** Output current waveform with its FFT Analysis (THD = 1.48%)

waveform because the load is inductive and acts as a low pass filter for the current.

## 5 Conclusion

In this article, novel basic and hybrid multilevel inverter structures have been presented, which can be used in photovoltaic applications. The proposed topology used fewer power electronic components in comparison to the other conventional topologies. Evidently, the proposed topology has clear advantages over conventional topologies. Finally, simulation results using MATLAB/Simulink software validated our conclusions.

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