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ORIGINAL RESEARCH

Design of fault tolerant bifunctional parity generator and scalable code converters based on QCA technology

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Abstract In this paper, we focus on novel designs for digital code converter and parity generator circuits in quantum-dot cellular automata (QCA) technology, which is transistor less computation approach and encodes binary information through the configuration of charges among quantum dots. In existing works, code converters and parity generators have been designed using majority gate and inverter-based XOR gates that is the basic structure of these circuits. However, our proposed designs use explicit cell interaction-based XOR gate to designing a compact form of QCA circuits. As a result, novel designs for generating parity bit, Binary to Gray, Gray to Binary code converter are presented with low complexity. Moreover, we will first demonstrate the bifunctional parity generator in QCA. The correct operation of the structures has been verified using the QCADesigner tool. A structural comparison was made with previous works and found that the proposed designs have significant improvements over existing ones.

Keywords Parity generator · Code converter · Fault tolerant design · Quantum-dot Cellular Automata · QCA · Nanocomputing

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1 Introduction

According to scientific estimates, the new transistor-based CMOS technology is approaching its physical limits for nanoscale nanotechnology implementation. The quantum-dot cellular automatic (QCA) proposed by Lent et al. [1] is one of the promising nanotechnologies. This is a solution for the problems, like feature size reduction and high power dissipation. The method of computation is also novel and based on cellular automata and quantum phenomena. This promising technology has pulled in many researchers due to its direct use in quantum computing [2–5].

Using quantum cells, QCA circuits are manufactured and each cell consists of four quantum dots plus two excess electrons. In [6], the experiments and possible physical applications (metal-island, semiconductor, magnetic, and molecular QCA) are investigated. Among them, high-speed switching (THz), high density and ultra-low power consumption are known as clocked molecular QCA. A quantum cell is the underlying aspect of this technology. The basic cell has been successfully manufactured recently [7].

In digital systems, the code converters have a significant importance for enabling fast signal processing [8–12]. The information can be represented within the shape of the particular codes such as binary, octal, and hexadecimal etc. Here, any data can be represented by using two bits '0' and '1'. Different types of code converters are available in the literature and among them, gray to binary and binary to gray code converters are widely used for mainly switching and encryption applications.

In this paper, we focus on the design of QCA code converter and parity generator circuits that are a part of complex QCA circuit design. Our goal is to develop a compact and stable code converter and parity generator

with the least complexity and low power consumption to improve the performance of the QCA computer system. In the context of a vital part of the digital circuit, the exclusive-OR (XOR) gate plays as a structural building block of code converters and parity generator. In this case, we use the most compact design of QCA XOR gate for our proposed designs.

2 Background and related works

In this section, a brief background into operating principles of QCA technology along with basic building clocks and clocking is presented followed by literature review of existing designs of XOR gate in QCA.

2.1 Background of QCA

A potential nanotechnology, QCA, performs logic states as the position of a pair of electrons in a cell, not as voltage state. Two mobile electrons are placed in the corners of a square-shaped cell with four quantum dots. There is electronic motion between the quantum dots, but it does not go out of the cell. Owing to the coulombic repulsion between the electrons, the electrons always organise diagonally. Therefore, two stable positions are formed in the cell, as shown in Fig. 1a, logic '1' (polarization + 1) and logic '0' (polarization − 1). The polarization P is determined as shown in Eq. (1), where ρ_i acts as the electronic charge in dot i [2–8]:

$$P = \frac{(\rho 1 + \rho 3) - (\rho 2 + \rho 4)}{(\rho 1 + \rho 2 + \rho 3 + \rho 4)}. \quad (1)$$

The unique feature of this technology is to encode binary information in the cell, and this provides high speed switching along with low power consumption. Unlike conventional CMOS technology, signal propagation is conducted based on cell-to-cell Coulomb interaction. Side-by-side cell placement forms a QCA array and is known as QCA wire, as shown in Fig. 1b. In Boolean logic, an inverter, an AND gate, and an OR gate form the most basic logic components. But in QCA architecture, the majority gate and inverter form the most basic logic components [12–16]. The QCA cells can simply enforce the logical NOT gate (inverter) by inverting the location of the electrons in the QCA cell, as shown in Fig. 1d. Five cells will recognise the main gate (M-3): three input cells, one system cell, and one output cell, as shown in Fig. 1c.

Logic AND/OR gates can be derived from the majority gate by setting one of its inputs to a constant (logic 0)/(logic 1), respectively. A lot of research has also been done to introduce new logical structures using QCA:

$$M_3(A, B, C) = AB + BC + AC, \quad (2)$$

$$M_3(A, B, 0) = ANDgate = AB, \quad (3)$$

$$M_3(A, B, 1) = ORgate = A + B. \quad (4)$$

The synchronization and power gain of the QCA cells for the signal propagation (polarization) is done by four distinct and cascaded clock phases. They work in a particular sequence as clock0 → clock1 → clock2- → clock3 → clock0, as shown in Fig. 2. Also, there are four stages (switch, hold, release, and relax) in each clock. In particular, in the first phase, the polarization begins and value is generated, in the second phase the full polarity is kept high so that the signal reaches the desired location, in the third phase the polarization barriers move from high to low, and in the last fourth phase, the polarizing tunnels close and the quantum cell returns to its non-polarized state [4–15].

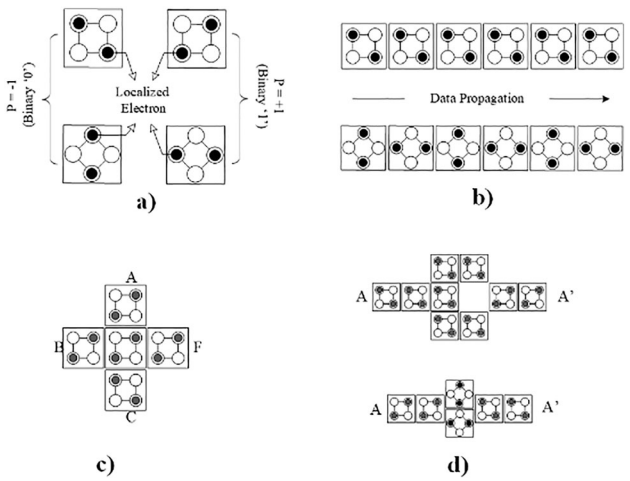

Fig. 1 QCA basic: **a** regular and rotated cells, **b** binary wire using regular and rotated cells, **c** 3 input majority voter gate, **d** inverters

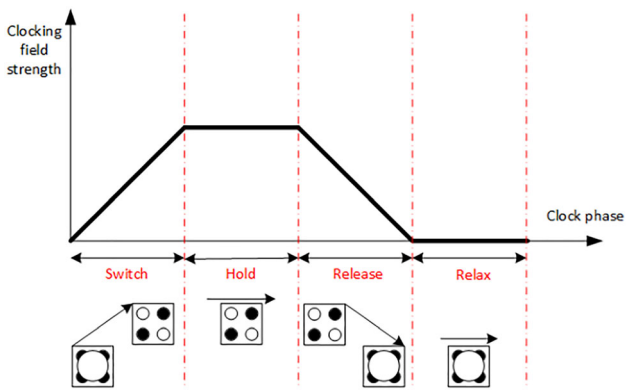

Fig. 2 QCA wire crossing: **a** coplanar, **b** multilayer, **c** logical crossover

2.2 Previous QCA exclusive-OR circuits

The XOR gate is the building block for the design of many digital circuits, such as arithmetic/logic circuits, encoders, parity generators and other circuits [15–17]. The logical implementation is based on this Eq. (5):

$$\begin{aligned} \mathrm{XOR(A,B)} &= \overline{A}\mathrm{B} + \mathrm{A}\overline{B} \\ &= M_3\left(M_3\left(\overline{A}, B, 0\right), M_3\left(A, \overline{B}, 0\right), 1\right). \end{aligned} \tag{5}$$

In QCA technology, many XOR layouts have previously been introduced, but the goal was to minimise the number of inverters and majority gates used by reforming the XOR equation. Figure 3a illustrates an example of the implementation of a traditional QCA XOR gate [9].

There is another widely used majority vote in the QCA, which is a five-input majority vote. Note that, the 3-input majority gate is denoted by M_3 and the 5-input majority gate is denoted by M_5. It can be used to reduce the QCA circuit's complexity. In Fig. 3c, the QCA configuration of the XOR gate using a five-input majority gate [18] is shown and is expressed as follows:

$$\mathrm{XOR(A,B)} = M_5\left(A, \overline{A}\mathrm{B}, \mathrm{A}\overline{B}, \overline{B}, 1\right). \tag{6}$$

There are other programmable basic cells, such as the NAND–NOR-inverter (NNI) gate, along with the common majority gate, that can be used to improve the design process of the QCA circuit. The NNI gate is an acceptable choice for realising NOR and NAND logic by assigning low and high logic levels to its middle input, respectively. In Fig. 3b, the design [10] consists of four NNI gates with a 1.0 clock cycle delay, expressed as follows:

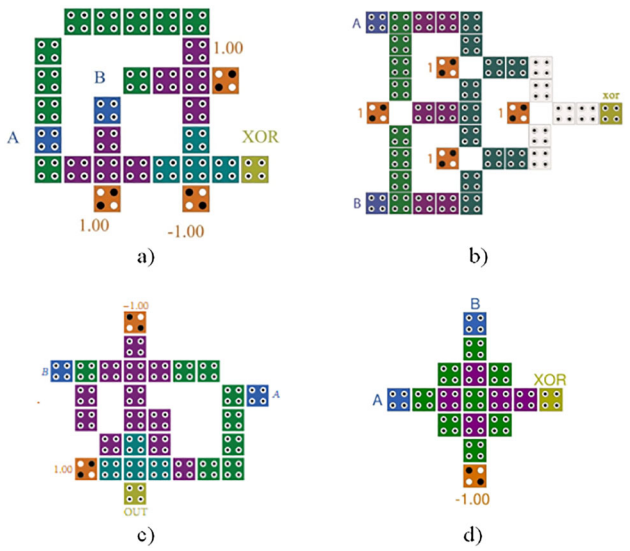

Fig. 3 XOR gates: **a** in [9], **b** in [10], **c** in [18], **d** in [6]

$$\mathrm{XOR(A,B)} = NNI(NNI(A, NNI(A, \mathrm{B}, 1), 1), NNI(B, NNI(A, \mathrm{B}, 1), 1), 1) \tag{7}$$

However, some of QCA XOR designs are implemented based on the inherent capability of QCA. This kind of design technique has advantages in terms of area and latency over gate-based counterparts. An example of XOR structure [6] is illustrated in Fig. 3d.

3 QCA exclusive-or based proposed designs

In this section, various proposed digital circuits such as 4-bit parity generator, 4-bit Binary to Gray and 4-bit Gray to Binary code converters have been presented along with their logic development and simulation results.

3.1 QCA parity generator

A logic component for computing systems is the parity generator that performs verification function of all received and transmitted data. Several works have been done to implement an efficient design of parity generator in QCA due to an important role in digital circuit design [8, 9].

Basically, there are two types of parity generator: Even Parity and Odd Parity generator. The Even or Odd parity generator receives a date if the total number of 1's in the code is an even or odd number, respectively. It works as following principle [7]:

1. The original message is obtained from the input of the parity generator;
2. A parity bit is generated for that message;
3. The transmitter sends the messages along with the generated parity bit to the receiver.

In this section, we demonstrate a proposed QCA design for the 4-bit parity generator. Figure 4 shows the proposed logic block of 4-bit even parity generator with QCA implementation.

Here we use the QCA XOR gate proposed in [6] for the importance of volatility. The design occupies 0.02 μm^2 with 38 cells and consumes 0.75 clock cycles. Note that if we change the fixed cell in the proposed layout to " + 1.00", the function of even parity generator will change to the odd parity generator. This makes our circuit dual function without any other change. It is worth noting that this scheme can be easily expanded to the n-bit form of the QCA parity generator circuit. The simulation waveform of proposed parity generator is shown in Fig. 5. The operation of the proposed design can be verified from this simulation waveform.

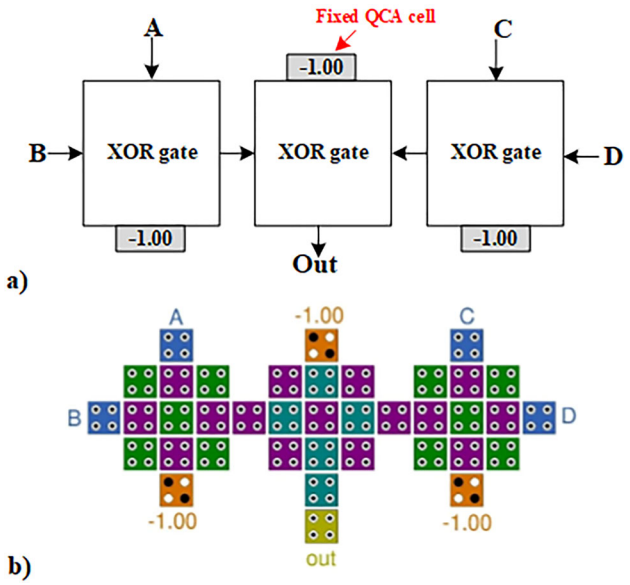

Fig. 4 Proposed Parity generator: **a** block diagram, **b** QCA design

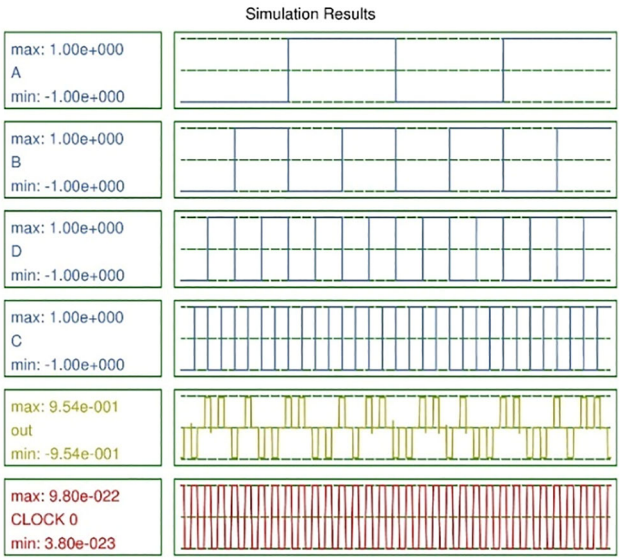

Fig. 5 The simulation result of the Parity generator

3.2 QCA Binary to Gray code converter

The binary to grey converter converts to its comparable grey code through a binary code. Gray code is often represented in a sequence of 0 s and 1 s, much like binary code. In cryptography and digital communication networks, grey code finds its applications. The input code is binary and the grey code is the output code. It is possible to change a binary code (B3, B2, B1, B0) to a grey code (G3, G2, G1, G0) after following Eqs. (8–11):

$$G0 = \overline{B0}B1 + B0\overline{B1} = B0 \oplus B1, \tag{8}$$

$$G1 = \overline{B1}B2 + B1\overline{B2} = B1 \oplus B2, \tag{9}$$

$$G2 = \overline{B2}B3 + B2\overline{B3} = B2 \oplus B3, \tag{10}$$

$$G3 = B3. \tag{11}$$

The Logic diagram and QCA layout of the proposed design are shown in Fig. 6. Three XOR gates are required to generate a 4-bit output gray code. This design comprises of 52 quantum cells and utilizing 0.5 clock cycles. The structure is involved by 0.04 μm^2 with low complexity. There is no need to cross wires in this design due to the compact use of the XOR structure. In addition, the proposed structure is designed properly to connect with different circuits. The simulation waveform of proposed binary to gray converter is shown in Fig. 7. The operation of the proposed design can be verified from this simulation waveform.

3.3 QCA Gray to Binary code converter

In view of the 4-bit grey code to 4-bit binary code, we further suggest a QCA circuit here. In binary representation, we want the stored data back. But we need a converter that will do a reverse operation to the previous converter. We call this a gray-to-binary converter. The gray-to-binary code converter outputs follow these Eqs. (12–15):

$$B0 = G0 \oplus G1 \oplus G2 \oplus G3, \tag{12}$$

$$B1 = G1 \oplus G2 \oplus G3, \tag{13}$$

$$B2 = G2 \oplus G3, \tag{14}$$

$$B3 = G3. \tag{15}$$

In this code converter, the XOR gates are also required. But this time, bits of gray code is XOR'ed with output binary code bits. Logical implementation and QCA layout of this structure are presented in Fig. 8a, b, respectively.

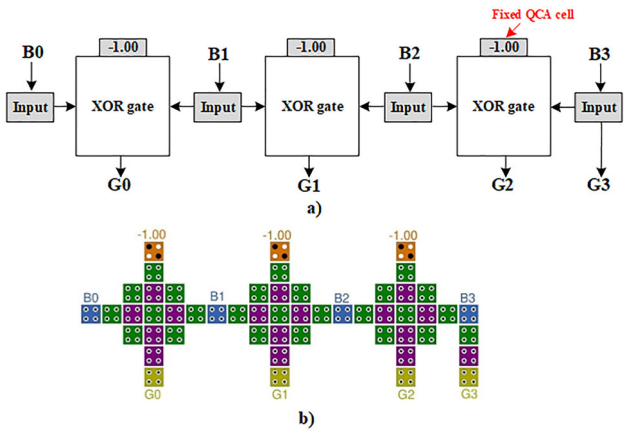

Fig. 6 Binary-to-Gray code converter: **a** block diagram, **b** QCA implementation

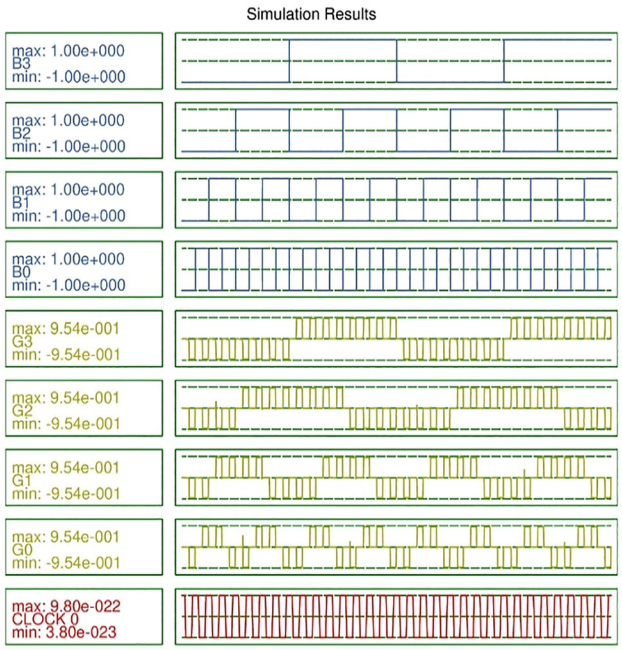

Fig. 7 The simulation result of BTG

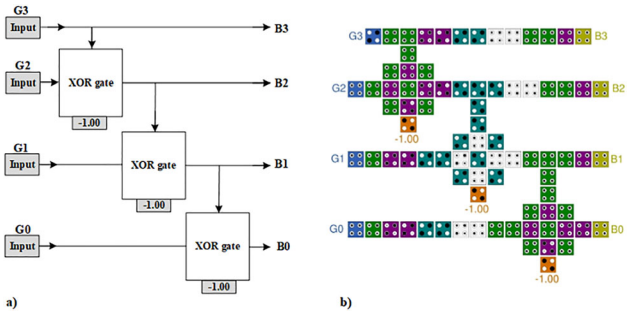

Fig. 8 Gray To Binary code converter: **a** block diagram, **b** QCA implementation

The proposed design has 84 QCA cells with a delay of 1.5 clock cycles and its simulation waveform is shown in Fig. 9. In the proposed structure, we again used compact XOR gates to reduce the complexity of the circuit. Three XOR gates are required to generate the 4-bit output binary code. XOR gates are the basic element of all code converters. The scalability feature of the proposed designs has been considered well.

4 Results and analyses

In this section, fault tolerance of XOR gate against single cell addition and single cell deletion effects have been presented along with the energy dissipation analysis of all proposed designs and their performance comparison with existing designs in the literature.

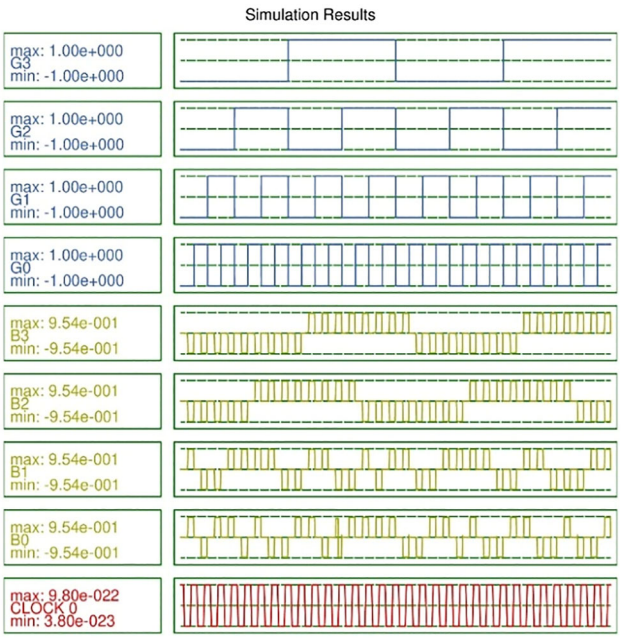

Fig. 9 The simulation result of Gray to Binary Code Converter

4.1 Defect characterization of used XOR gate

For cells to function properly in QCA technology, they need to be adapted in nanoscales with extreme precision. Thus, a precise inspection of the QCA structure for manufacturing defects plays an important role in the detecting the reliability of QCA schemes. Defects in production are categorized into defects in deposition and defects in chemical synthesis phases. The probability of defects in the chemical synthesis process is much lower than the defects caused during deposition phase [19–22]. In QCA structures, missing cell, additional cell and misalignment of cells defects usually occur. In this paper, fault tolerance of the XOR gate against single missing cell and single additional cell defects is presented.

It was observed that test vector $\langle 0\ 0 \rangle$ has fault coverage of $(2/16) \times 100 = 12.5\%$, where 2 is the number of faults for this test vector and 16 is the number of possible tests for this test vector. Similarly, vector $\langle 0\ 1 \rangle$ has $(4/16) \times 100 = 25\%$ fault coverage, $\langle 1\ 0 \rangle$ has $(5/16) \times 100 = 31.25\%$ coverage and vector $\langle 1\ 1 \rangle$ has $(5/16) \times 100 = 12.5\%$ fault coverage. It is thus calculated 16 faults out of total 80 test scenarios occur in the XOR design which leads to fault tolerance of $(80 - 16) \times 100/80 = 80\%$ against single cell addition defect.

Similarly, for single cell missing defect analysis, it was observed that the test vector $\langle 0\ 0 \rangle$ has $(8/28) \times 100 = 28.57\%$ fault coverage, $\langle 0\ 1 \rangle$ has $(5/28) \times 100 = 17.85\%$ coverage, vector $\langle 1\ 0 \rangle$ has $(8/28) \times 100 = 28.57\%$ coverage and finally vector $\langle 1\ 1 \rangle$ has $(7/28) \times 100 = 25\%$ fault coverage. It is thus calculated

that 28 faults occur in the possible 52 test scenarios which leads to the fault tolerance of $(52 - 28) \times 100/52 = 46.15\%$ against single cell deletion defect.

4.2 Structural analysis of the proposed designs

In this section, the correct operation of the structures has been verified and validated using the QCADesigner tool 2.0.3 [23]. This simulation tool has two simulation engines (bistable approximation and coherence vector), and all the proposed designs are examined under both simulation engines. The parameters used for simulation using bistable approximation engine are given in Table 1. The QCA layout generated by the simulator is analyzed to evaluate the relevance of the values based on equations.

The simulation result of the proposed parity generator is illustrated in Fig. 5. As we mentioned above, the proposed QCA parity generator can be used to perform both types of parity generator (even or odd) with a slight change.

In Figs. 7 and 9, simulation results of Binary to Gray and Gray to Binary code converter circuits are authenticated. The simulations prove that both results confirm their conformity to the equations. The obtained simulation results clearly show that all the proposed circuits are stable and reliable.

Table 2 comprises the previous works with the proposed designs in terms of hardware complexity. According to Table 2, the results of the proposed designs have significant improvements over their previous counterparts in terms of area, cell count, and latency.

It is seen that proposed parity generator achieves performance improvement of 97.99% against design in [10], 90% against design [8] and 93.75% against design in [9] in terms of cost of the circuit. Similarly, the proposed binary to gray converter shows improvement in design cost of 93.69% against design in [12], 83.17% against design in [11] and 48.73% against design in [9]. Finally, proposed gray to binary converter designs shows improvement in design cost of 60.63% against design in [11] and 48.16% against design in [9]. Although the cost of gray to binary code converter design in [12] is lower than the proposed design, however it is worth noting that the design in [12] is multilayer is nature which has its own fabrication difficulties compared to coplanar designs. Also, proposed design has 52% less cells in the design and occupies 65% less area than [12], thereby making the proposed design more efficient that design in [12].

In addition, the QCA parity generator that we propose can be used as an even as well as an odd parity generator, namely, it is bifunctional. The coplanar design has an advantage over the multilayer structure during the manufacturing process. That is why all the proposed designs are coplanar. It should be noted that previous works have not been considered to be integrated with other combination schemes, but this feature is well considered in our designs.

Table 1 Parameters of bistable approximation in QCADesigner tool [23]

Parameters	Value
Cell size	18 nm
Dot diameter	5 nm
Clock low	3.8e − 23 J
Clock high	9.8e − 22 J
Clock amplitude factor	2
Layer separation	11.5 nm
Maximum iteration per sample	100
Radius of effect	65 nm
Number of samples	50,000
Convergence tolerance	0.001
Relative permittivity	12.9

4.3 Energy dissipation analysis

For a detailed analysis of the proposed designs, energy dissipation through QCAPro tool [24] was calculated. In QCA circuits, QCAPro analyzes the total energy dissipation in two main energy categories called 'leakage energy' and 'switching energy' dissipation. The energy losses corresponding to the switching cycles and energy losses corresponding to clock transaction of the QCA cells leads to the 'switching energy' and 'leakage energy' dissipation, respectively. The power analysis is conducted by considering three different energy levels ($0.5\ E_k$, $1.0\ E_k$ and $1.5\ E_k$) at temperature of 2 K [24–28].

In Table 3, the energy dissipation results of the proposed designs are given in according to the average leakage energy, switching energy, and total circuit energy dissipation, respectively, for the three different tunnelling energy levels at 2 K temperature.

Energy dissipation (Thermal) maps for the proposed designs are illustrated in Figs. 10 and 11. According to thermal map, it is seen that the high-energy cells generate a lot of heat which are seen as hot spots that appear in darker colors in the map.

5 Conclusions

This paper presented the designs of a parity generator, Gray to Binary and Binary to Gray code converter. The proposed designs occupy a small area and consume a small delay in comparison with existing analogs. In addition, unlike other existing QCA parity generators, the proposed parity

Table 2 Structural comparison of the designs

Circuits	QCA circuit complexity			Cost (area × latency^2)	Cross-over type
	The cell count	Total area (μm^2)	Latency (clock cycle)		
Parity generators					
[10]	111	0.14	2.00	0.56	Coplanar
[8]	37	0.05	1.50	0.1125	Coplanar
[9]	86	0.08	1.50	0.18	Multilayer
Proposed	38	0.02	0.75	0.01125	Coplanar
Binary to Gray converter					
[12]	111	0.08	2.00	0.32	Coplanar
[11]	127	0.12	1.00	0.12	Multilayer
[9]	99	0.07	0.75	0.0394	Multilayer
Proposed	52	0.04	0.50	0.0202	Coplanar
Gray to Binary converter					
[12]	175	0.20	0.75	0.1125	Coplanar
[11]	100	0.10	2.00	0.4	Coplanar
[9]	76	0.06	2.25	0.3038	Coplanar
Proposed	84	0.07	1.50	0.1575	Coplanar

generator performs two (even and odd) functions with a slight change. The proposed structures were simulated and verified using the QCADesigner tool version 2.0.3. A structural comparison was made with previous works and found that the proposed designs have significant improvements over existing ones. Moreover, along with structural analysis, energy dissipation aspect of the proposed structures is carried out. It is seen that the proposed designs are cost efficient. In future work, these proposed designs can be used for designing higher order circuits in various applications such as nano-communication systems, error detection systems, arithmetic units, etc. In addition to this,

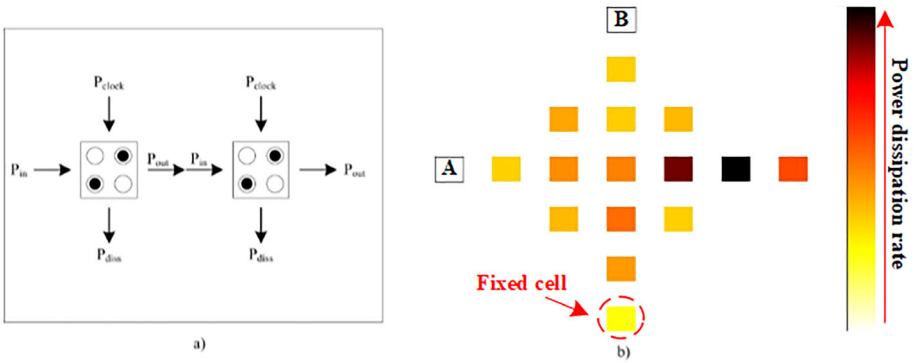

Fig. 10 **a** Energy flow in a QCA cell, **b** Energy dissipation map of XOR gate

Table 3 Energy dissipation analysis

Circuits	Avg. leakage energy dissipation (meV)			Avg. switching energy dissipation (meV)			Avg. energy dissipation of circuit (meV)		
	0.5 E_k	1.0E_k	1.5 E_k	0.5 E_k	1.0E_k	1.5 E_k	0.5 E_k	1.0E_k	1.5 E_k
XOR gate	8.35	19.48	30.89	7.66	6.04	4.88	16.01	25.52	35.77
Parity generator	18.04	44.06	70.34	15.01	11.03	8.50	33.05	55.08	78.84
Binary to Gray	23.12	58.30	95.20	22.00	17.66	14.31	45.13	75.96	109.51
Gray to Binary	33.28	89.90	151.46	85.24	69.63	56.96	118.52	159.53	208.42

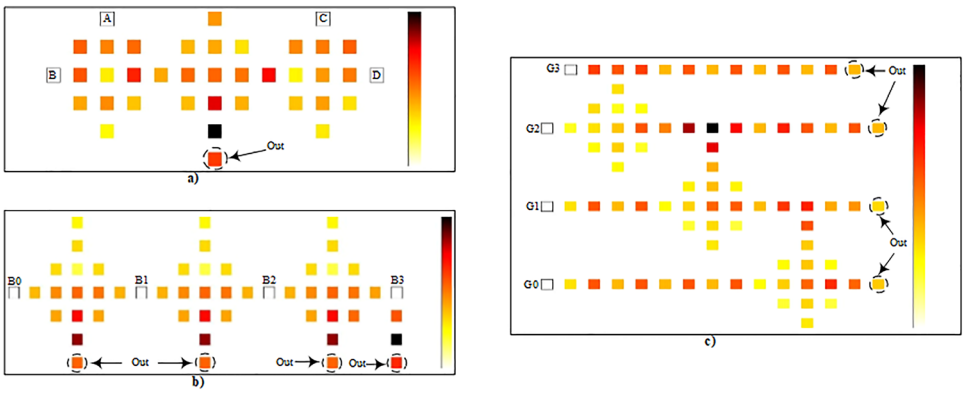

Fig. 11 The energy dissipation map of the proposed designs **a** parity generator, **b** Binary to Gray converter, **c** Gray to Binary converter

fault tolerance against multiple cell missing and addition defects, fault tolerance against cell displacement and misalignment can also be done.

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