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Design and development of multi-channel front end electronics based on dual-polarity charge-to-digital converter for SiPM detector applications

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Abstract
With the development of silicon photomultiplier (SiPM) technology, front-end electronics for SiPM signal processing have been highly sought after in various fields. A compact 64-channel front-end electronics (FEE) system achieved by field-programmable gate array-based charge-to-digital converter (FPGA-QDC) technology was built and developed. The FEE consists of an analog board and FPGA board. The analog board incorporates commercial amplifiers, resistors, and capacitors. The FPGA board is composed of a low-cost FPGA. The electronics performance of the FEE was evaluated in terms of noise, linearity, and uniformity. A positron emission tomography (PET) detector with three different readout configurations was designed to validate the readout capability of the FEE for SiPM-based detectors. The PET detector was made of a 15×15 lutetium–yttrium oxyorthosilicate (LYSO) crystal array directly coupled with a SiPM array detector. The experimental results show that FEE can process dual-polarity charge signals from the SiPM detectors. In addition, it shows a good energy resolution for 511-keV gamma photons under the dual-end readout for the LYSO crystal array irradiated by a Na-22 source. Overall, the FEE based on FPGA-QDC shows promise for application in SiPM-based radiation detectors.

Keywords Readout electronics · Charge measurement · Radiation detector · Silicon photomultiplier · Field-programmable gate array

1 Introduction

Semiconductor-based detectors have been widely used as radiation detectors in various fields, such as astrophysics [1], medical imaging applications [2–6], and high-energy physics [7, 8]. Recently, silicon photomultipliers (SiPMs) have been found to provide a high gain of approximately 10^6, which is comparable to that of photomultiplier tubes. The performance of SiPMs is unperturbed in the presence of a strong magnetic field. Moreover, the biased supply is decreasing (~24 V). Considering these advantages, this type of detector has become a new candidate for various experiments [9, 10]. In nuclear medicine, combinations of SiPMs and scintillators are commonly used in PET detectors. With current SiPMs, PET detectors can achieve good performance in terms of energy resolution, crystal discrimination, coincidence timing resolution, and depth of interaction. In addition, strip SiPMs have gained attention because of their precise timing and positioning measurement [11, 12].

There are many ways to read the signals of SiPM-based detectors. Traditional charge readout schemes for single-pixel SiPMs, including front-end electronics (FEE) [13–16] based on signal integration and shaping and a data acquisition system based on a commercial analog-to-digital converter (ADC) [17], provide a rapid way of customizing the signal processing electronics system. For multi-pixel SiPMs, it is difficult to use the traditional readout method. Efforts have been made from different perspectives to mitigate the complexity of signal processing for the SiPM array. On the SiPM detector side, multiplexing schemes with different multiplexing ratios (8:1 and 16:1) were designed [18].

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Resistor-based and capacitor-based multiplexing circuits have become available [19, 20]. On the electronics design side, there are two research paths to resolve the electronics readout for SiPM-based radiation detectors. One is based on commercially available off-the-shelf discrete components and programmable chips. In this study, many methods of handling the readout of SiPMs have been discussed. For example, the time-over-threshold (ToT) method is widely used because of its simple circuit structure [21, 22]. The ToT results exhibit poor precision owing to the intrinsic nonlinearity between the deposited energy and pulse duration. Taking advantage of the abundant inputs/outputs (I/Os) and logic resources in field-programmable gate arrays (FPGAs), an FPGA-ADC scheme based on carry chain time-to-digital converter (TDC) was developed to achieve a multi-channel design with a compact size [23]. At present, however, the sampling frequency of the FPGA-ADC can only reach 25 MHz because of its low dynamic range and poor resolution. Further studies are required in the future. The other path of research involves the application specific integrated circuit (ASIC)-based readout method, such as Triroc ASIC [24] and TOFPET2 ASIC [25]. ASICs can perform well, but high cost and long periods are needed to develop and validate these ASICs.

There are still strong motivations for seeking cost-efficient, multi-channel, easy-to-design FEE for SiPM-based detectors. Several studies have shown potential in regards to implementing highly integrated readout electronics for SiPM-based detectors [26, 27]. Among these, the linear discharge scheme based on the current low-cost FPGA can achieve not only good linearity but also perfect timing performance [27]. The linear discharge scheme provides a direct charge-to-digital converter (QDC). In the linear discharge scheme, the analog part incorporates a capacitor, two resistors, and an operational amplifier (op amp for short). The digital part only requires an FPGA. It is feasible to address multi-channel analog signals using rich resources and I/Os in the FPGA. In the initial version, the linear discharge QDC could only process negative polarity signals, limiting its potential applications. In our previous study [28], the linear discharge-based QDC was improved in an easy way to process both negative and positive charge signals (i.e., dual-polarity charge signals). This improvement extends the scope of the application of the linear discharge circuit. In this study, based on the linear discharge QDC, we propose a compact, power-efficient, multi-channel FEE readout system for SiPM-based radiation detectors. The system consists of two parts: an analog board and FPGA board. The hardware design of the system is described in detail. Evaluations, including the electronics performance and detector applications, are conducted. Electronics evaluations include noise, linearity, and uniformity measurements. Detector applications are assessed using three different detector modules combined with a lutetium–yttrium oxyorthosilicate (LYSO) array and SiPM array.

2 Dual-polarity QDC based on linear discharge

The dual-polarity QDC based on a linear discharge scheme is shown in Fig. 1. An analog circuit and a digital circuit is necessary to achieve a linear discharge QDC. The analog circuit consists of an op amp, an integration capacitor, and two resistors ($R_{\text{discharge}}$ and R_{L}), whereas only an FPGA is required in the digital circuit. At a quiescent status when there is no current pulse from the SiPM detector, a 3-state buffer that is controlled by a control module in the FPGA maintains a high impedance ('hz'). This corresponds to a disconnection between the resistors ($R_{\text{discharge}}$ and R_{L}) and FPGA, resulting in a circuit structure of the traditional charge-sensitive amplifier with a constant value of $(R_{\text{discharge}}+R_{\text{L}})C_{\text{f}}$. When the SiPM detector is fired, the current pulse signal from the detector is first integrated on the feedback capacitor C_{f}. The output voltage of the op amp increases, turning the output of the voltage comparator, which is a low voltage differential signaling (LVDS) comparator, over upon going across the preset threshold V_{Thr}. The logic output of the LVDS comparator determines the start of the discharge process. In the case of negative current pulse injection, V_{Thr} is slightly higher than the baseline of the op amp in quiescence. The logic output of the LVDS comparator is '0'. The *T* port of the 3-state buffer is driven by the control module whereby the 3-state buffer outputs a 'hz' state. The negative current pulse causes the output of the LVDS comparator to turnover, i.e., logic '1'. In this case, the *I* port of the 3-state buffer is set to '1' by the control module, resulting in a positive voltage V_{IO} at the FPGA discharging pin, typically 2.5 V (I/O bank voltage). Subsequently, the discharging current $i_n(t)=V_{\text{IO}}/R_{\text{discharge}}$ becomes constant. The discharging process lowers the output voltage

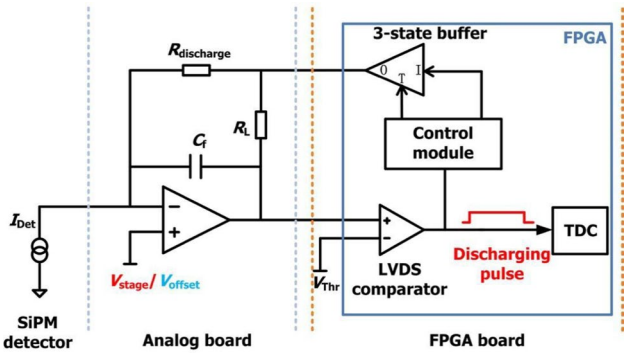

Fig. 1 Schematic of dual-polarity QDC based on linear discharge scheme

of the op amp. It does not end until the output voltage of the op amp is lower than V_{Thr} the second time. The V_{offset} at the noninverting port of the op amp is applied to adjust the output baseline to ground. Theoretically, the pulse width T_{pulse} at the output of the LVDS comparator is strictly proportional to the total charge Q injected into the QDC circuit if V_{Thr} is set to ground, which is given by:

$$T_{\mathrm{pulse}} = \frac{Q}{i_n(t)} = \frac{Q \times R_{\mathrm{discharge}}}{V_{\mathrm{IO}}}. \tag{1}$$

If the pulse is digitized with a counter in the FPGA driven by the system clock of F_{S}, code D is expressed as:

$$D = \mathrm{floor}\left(\frac{T_{\mathrm{pulse}}}{T_{\mathrm{S}}}\right) = \frac{Q \times R_{\mathrm{discharge}} \times F_{\mathrm{S}}}{V_{\mathrm{IO}}}, \tag{2}$$

where the floor function returns the nearest integer for $T_{\mathrm{pulse}}/T_{\mathrm{S}}$.

For a positive charge injection, the output of the op amp generates a 'negative' voltage pulse. However, the FPGA can only address signals above the ground. In this case, a stage voltage V_{stage}, typically 2.5 V, is applied to pull up the output baseline of the op amp such that the FPGA can be managed. In contrast to that in the case of negative charge, V_{Thr} is slightly lower than V_{stage}. In quiescence, the output logic of the LVDS comparator is '1'. The T port of the 3-state buffer is driven, which is controlled by the control module, resulting in a high-impedance 'hz' output of the 3-state buffer. Charge integration on the C_{f} lowers the output voltage of the op amp when a positive current pulse arrives. The output logic of the LVDS comparator becomes '0' when the output voltage of the op amp is less than the preset V_{Thr}. Consequently, the I port of the 3-state buffer is set to '0', whereby the output of the 3-state buffer is ground. In contrast to the discharging current in the case of a negative charge, this gives rise to a reverse discharging current $i_{\mathrm{p}}(t) = V_{\mathrm{stage}}/R_{\mathrm{discharge}}$. The subsequent process is similar to that for a negative charge. It should be noted that the discharging current directions are different for the positive and negative charges. In the linear discharge scheme, the leading edge of the discharging pulse indicates the arrival of the event, enabling simultaneous charge and timing measurements.

3 Hardware design

A stacked configuration was designed to achieve compact FEE, as shown in Fig. 2. In multi-channel FEE, the analog and digital circuits are designed on an analog board and FPGA board, respectively.

3.1 Analog board

The analog board consists of analog circuits for dual-polarity QDC based on linear discharge, four 30-pin connectors (FH12 series, Samtec), and two 100-pin high-density connectors (ST4 series, Samtec). The 64 charge signals are divided into four groups. Each group has 16 signals connected to one FH12 connector. Two ST4 series connectors are used to implement a board-to-board interconnection with the FPGA board. In the ST4 series connectors, the outputs of the op amp are referenced to the analog ground, whereas the discharging signals are referenced to the digital ground. The analog circuit for the dual-polarity QDC consists of 16 high-performance quad amplifiers, resistors, and capacitors that are used to achieve linear discharge circuits. At the noninverting port of each op amp, V_{stage} and V_{offset} are selected to enable negative and positive charge measurements, respectively. To increase feasibility, an alternatively coupling capacitor C_0 is assembled for each channel. In direct coupling mode, the capacitor can be replaced by a resistor. Figure 3 shows all the components in a 12-layer printed circuit board with an overall size of 70 mm × 70 mm. Thus, the linear discharge based QDC covers an average

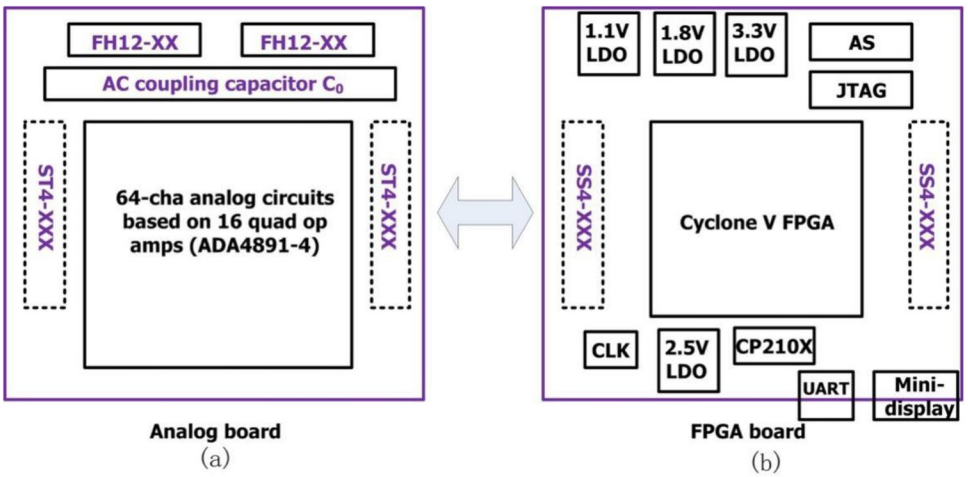

Fig. 2 Simplified block diagram of analog board **a** and FPGA board **b**

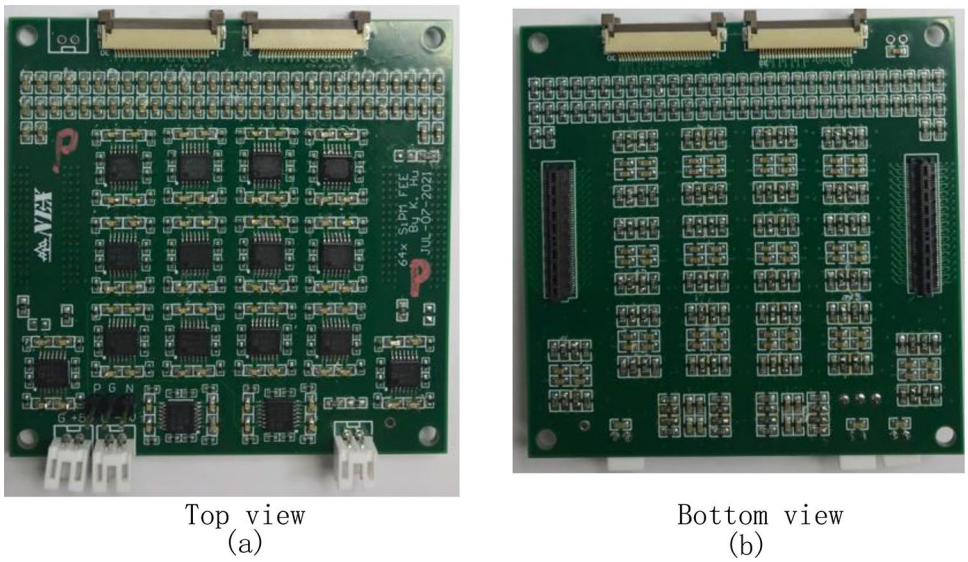

Fig. 3 (Color online) A snapshot of discrete components assembled on the top **a** and bottom **b** of the analog board

area of 0.77 cm^2 for one channel. In normal operation, a 5-V power supply (2231A-30-3, Tektronix) was applied on the analog board, and a current of 0.310 A was observed. Thus, it resulted in an average power dissipation of 24.2 mW for one channel.

3.2 FPGA board

On the FPGA board, the core comprises a low-cost Cyclone V FPGA (5CEBA7 series, Intel) that implements all functions, such as discharging control and data buffering. An external 128-Mb EPCS flash memory is used to store the FPGA firmware via an active serial (AS) configuration. In the debug mode, an excellent low-jitter 200-MHz oscillator (DSC1103, Microchip) on the FPGA board is utilized to drive a phase-locked loop in the FPGA, providing global clocks for firmware development. A USB-to-UART bridge chip (CP2103, Silicon Labs) with a 921,600-bps baud rate is applied to transmit the detector data and related debug information. A B-type USB connector is used for plug-and-play communication with a PC. A mini display port was designed for external clock distribution, synchronization, and communication. Four pairs of LVDS I/O ports with a maximum rate of 1.25 Gbps were deployed to enable user-defined command communications and detector date transmissions. Notably, multiple FEE modules can be conveniently scaled to a large-scale distributed system for particle detectors.

Most of low voltages on the FPGA board, such as 1.8 and 2.5 V, are generated by low-dropout (LDO) linear regulators (TPS74401, TI). However, the V_{Thr} voltage is from another LDO regulator (LT3080, Analog Device), which supports an adjustable output down to zero. In experiments, V_{Thr} thresholds for the positive and negative charge signals are 2.47 and 30 mV respectively. Two SS4 connectors were used to implement a board-to-board interconnection with the analog board. Notably, the voltage comparators and 3-state buffers in the linear discharge scheme are instantiated with digital LVDS receivers and digital low-voltage complementary metal oxide semiconductor output ports in the FPGA, respectively. Figure 4 shows the customized FPGA board. The size of the FPGA is the same as that of the analog board (i.e., 70 mm × 70 mm). They are connected to two board-to-board connectors (SS4 and ST4 series).

3.3 FPGA firmware

Figure 5 shows the firmware framework of the FEE system. The internal functional blocks include: (1) an LVDS comparator and 3-state buffer array for 64-channel linear discharge implementation, (2) charge calculations and timing pickoff using the counters in the FPGA, (3) event buffering and formatting, and (4) communication interfaces including the UART engine and LVDS data engine. In the final design, the UART engine is used for debugging, whereas the LVDS interface is used for system integration. In addition, time measurement involves high-precision TDC implementation based on the carry chain in the FPGA [29–32], which is under development. In the performance evaluations of the FEE for the SiPM detector application, only a coarse counter is applied.

4 Evaluation experiments

Evaluation experiments for FEE are grouped into two categories: electronics and detector tests. All experiments were conducted at room temperature. The experimental setup is described below.

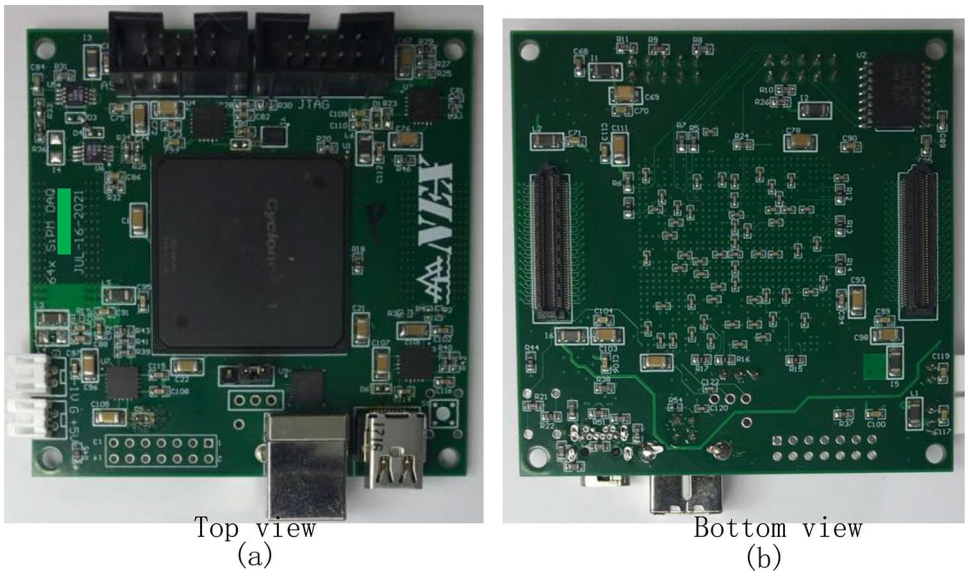

Fig.4 (Color online) Pictures of the top **a** and bottom **b** of the FPGA board

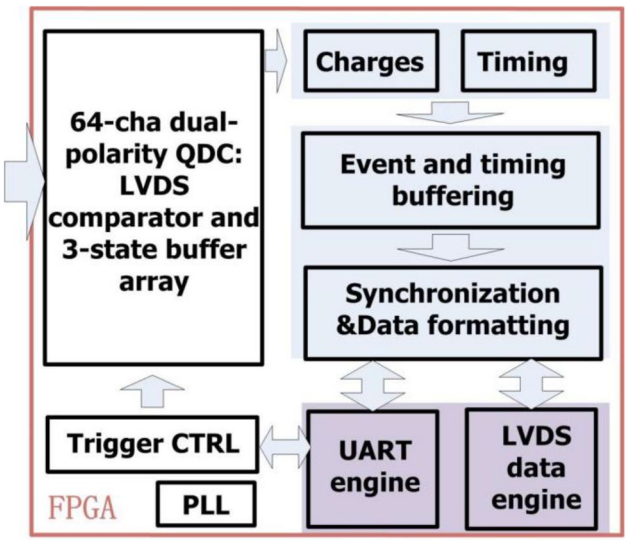

Fig. 5 Firmware framework of the proposed front end electronics modules

4.1 Electronics test setup

The evaluation experiments were conducted to measure electronics noise, channel linearity, and uniformity.

a) The baseline fluctuations of the op amp were used to quantify the electronics noise of the analog board. The noise was observed using an oscilloscope. Subsequently, the noise data were filled into a histogram. The noise value was represented as the root mean square (RMS) of the noise spectrum.

b) Channel linearity plays an important role in FEE for particle detectors. A pulse generator (AFG3252, Tektronix) was used to drive the capacitor $C_G = 200$ pF. The relationship between the charges and digital codes of the QDC was obtained by stepping up the amplitude V_G of the pulse, which corresponded to an injected charge $Q = C_G \times V_G$. The pulse generator was controlled to provide a pulse amplitude of 50 mV per step (i.e., 10 pC/step). The pulse width of the QDC was measured using a coarse counter. The 64-channel data were packaged and sent to a host PC for post-processing. For each stepped amplitude of the output pulse from the generator, 2000 events were acquired to measure the mean value. In electronics tests, the standard deviation in the histogram was negligible. The calculated mean values were plotted in a graph and fitted using least-squares estimation. A block diagram of the experimental setup used for the linearity test is shown in Fig. 6.

c) The linearity results for multi-channel electronics are different, owing to the nonuniform parameters in the channels. Channel uniformity was evaluated using the fitted slope and intercept distributions. Slope uniformity is expressed as mean ± standard deviation. Notably, half of the QDC channels were configured as negative polarity inputs, while the other half were configured for positive polarity in the linearity test.

4.2 Detector setup

An 8 × 8 SiPM (S13361-3050, Hamamatsu) array was used to evaluate the dual-polarity multi-channel FEE. The size of the SiPM array was 25.8 mm. Each pixel covered an active area of 3 × 3 mm^2. The gap between adjacent pixels was 0.2 mm. The breakdown voltage V_{BR} was 53 V. Under normal operation in our experiments, the applied voltage was $V_{BR} + 2.4$ V. The SiPM array was biased using a DC power

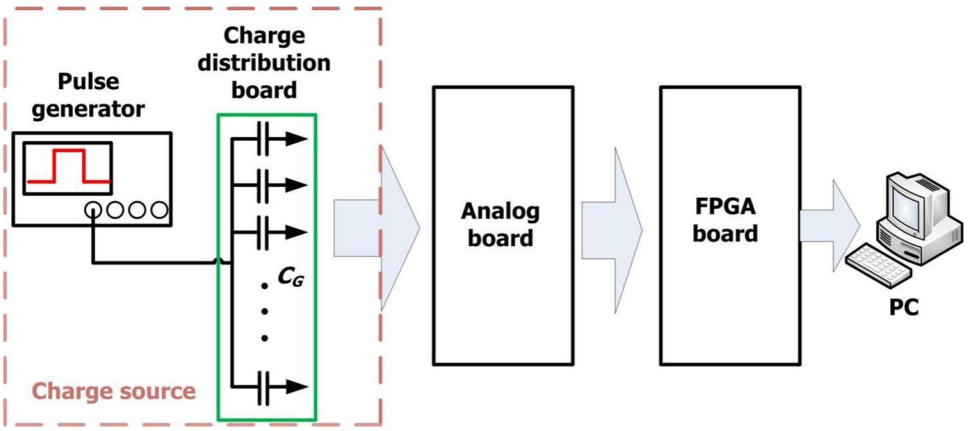

Fig. 6 Simplified block diagram of the linearity test system

supply (E3617A, Agilent). Another 15 × 15 LYSO crystal array (Epic Crystal Co., Ltd.) was designed to generate light signals. In the LYSO array, each bar had the dimensions 1.535 mm × 1.535 mm × 20 mm. Four lateral surfaces of the LYSO crystal bar were unpolished, whereas the two ends were polished. In the gap between crystals, enhanced specular reflectors with a thickness of 0.065 mm were placed. Thus, the center-to-center distance between two adjacent crystals was 1.6 mm. The combination of a scintillator and SiPM forms a PET detector. In the PET detector, the LYSO array is directly coupled to the SiPM with silicon grease. A half-of-crystal shift was used to achieve 4-to-1 coupling, whereby the LYSO array was located at the center of the SiPM [28]. The PET detector was irradiated using a Na-22 point source. The FPGA was programmed to automatically perform event triggers, charge and timing calculations, data formatting, and data communications with a host PC via the UART interface.

The SiPM array is configured using three readout methods. In the first one, all the cathodes are connected, and charges are read out though the 64-channel anode electrodes. Positive charge signals are induced on the anode electrodes, resulting in positive polarity configurations for the 64-channel FEE, namely, V_{stage} at the noninverting port of the amplifiers. However, in the second scheme, all the anodes are connected, and the signals on the cathode electrodes are fed to the 64-channel FEE. Conversely, the polarity of the induced charge is negative. In this case, the analog board is configured as a negative-polarity input mode (i.e., V_{offset} at the noninverting port of all amplifiers). In these two schemes, 64-channel signals are used for energy-weighted positioning. If a particle strikes a crystal bar, thousands of visible light molecules are generated after excitation. Light is transmitted along the crystal bar. The light is divided into several parts when arriving at the sensitive surface of the SiPM pixels. This is also called the 'light-sharing mechanism' [33–35]. According to the location of the different bars, the lights can be divided into 1, 2, and 4 parts, which are received by the adjacent pixels in the SiPM. Thus, the coordinate (X, Y) of the fired crystal bar based on energy-weight positioning is expressed as:

$$X = \frac{\sum_j x_j (\sum_i Q_{ij})}{\sum_{ij} Q_{ij}}, \tag{3}$$

$$Y = \frac{\sum_i y_i (\sum_j Q_{ij})}{\sum_{ij} Q_{ij}}, \tag{4}$$

where x_j and y_i are the relative coordinates of the SiPM pixels along the columns and rows, respectively. In addition, i and j are the row and column indices of the pixel, respectively. Q_{ij} is the total charge at the output of each pixel.

For the third readout scheme presented in our previous study [36], anodes and cathodes are combined into 8-row and 8-column outputs, respectively, which is referred to as '8 + 8 SiPM'. Specifically, the anodes in each row are connected, whereas the cathodes in each column are connected. Under this configuration, only eight positive-polarity electronics channels and eight negative-polarity electronics channels are needed. In the analog board, only one FH12 series connector is used to connect to the adapter board. The energy-weighted position (X, Y) is simplified as:

$$X = \frac{\sum_i x_i Q_i^{\text{c}}}{\sum_i Q_i^{\text{c}}}, \tag{5}$$

$$Y = \frac{\sum_i y_i Q_i^{\text{r}}}{\sum_i Q_i^{\text{r}}}, \tag{6}$$

where Q_i^{r} and Q_i^{c} are the readout charges along the rows and columns, respectively. x_i and y_i are the relative coordinates

of the SiPM pixels. Taking advantage of the dual-polarity QDC scheme, the 8 + 8 SiPM reduces the number of readout electronics channels, thereby facilitating large-scale, multi-channel detector development. Three adapter boards with different configurations are shown in Fig. 7.

In the first two configuration schemes, one end of the LYSO array is coupled to one SiPM. The other end is sealed with Teflon tape. Crystal position decoding maps, also called 'crystal discrimination maps, were generated using an energy-weighted algorithm. The quality of the position decoding maps was evaluated qualitatively via profile analysis. In the third readout configuration, the LYSO crystal array was coupled with two 8 + 8 SiPMs at the two ends because of the sufficient electronics channels. In total, 32 electronics channels were used for the dual-end readout method. In this case, dual-end energy information can be obtained. The energy spectrum of the gamma photons was plotted. The energy resolution is given by the full width at half maximum. Figure 7 shows the detectors and adapter boards for the three readout configurations.

5 Results

5.1 Electrical performance

Figure 8 shows the baseline and noise spectrum from one of the negative-polarity channels. A baseline offset of − 1.233 mV originates from the input bias current of the op amp and unbalanced parameters at the differential input ports. Fitting with a Gaussian function shows an RMS noise of 1.357 mV_{rms}. The baselines of all the channels were measured to set a unified threshold V_{Thr} for all the electronics channels. Figure 9 shows a graph with error bars illustrating

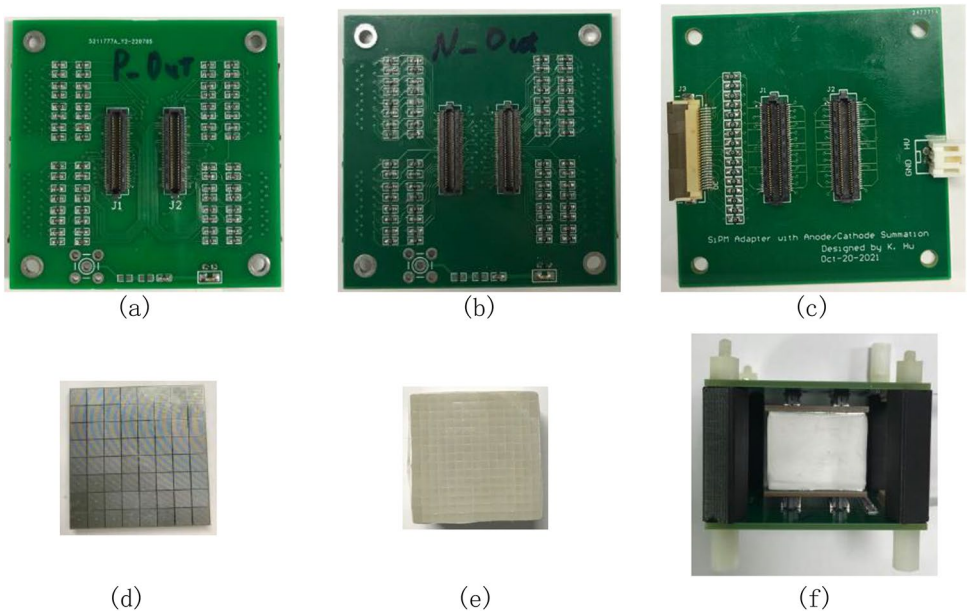

Fig. 7 (Color online) Photographs of the detectors and adapter boards. **a** Adapter board for first detector readout configuration in which all anode signals are read out. **b** Adapter board for second readout configuration. **c** Adapter board for third readout configuration. **d** 8 × 8 SiPM array. **e** 15 × 15 LYSO crystal array. **f** The PET detector is made up of LYSO array coupled with SiPM arrays at two ends; a 3-D printing holder is applied to assemble detectors and adapter boards

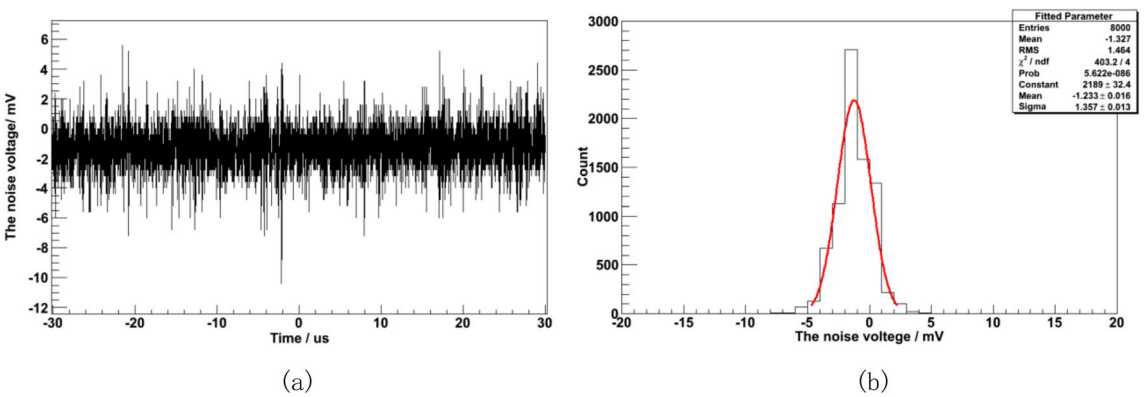

Fig. 8 Baseline **a** and noise spectrum **b** from one negative-polarity channel

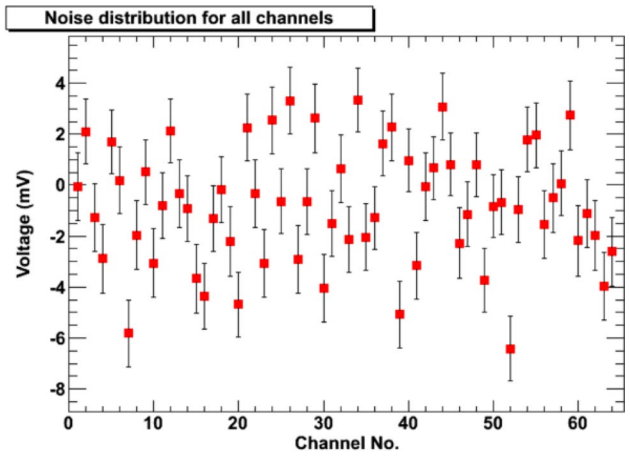

Fig. 9 Baseline noise distribution for all channels

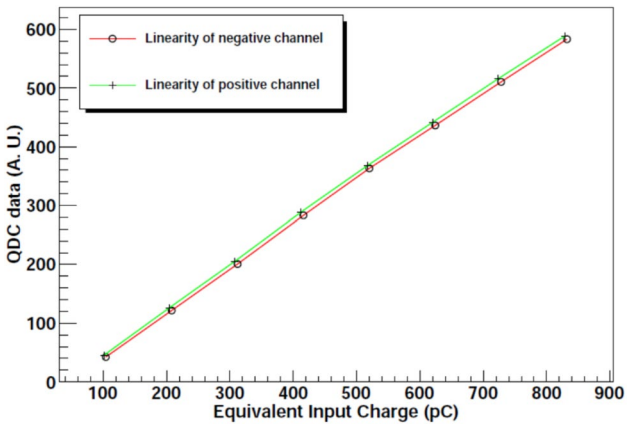

Fig. 11 (Color online) Linearity results for one (red) of the negative channels and one (light green) of the positive channels. (Color figure online)

the baseline offset and noise distribution for these 64 channels. Notable, all channels are configured as negative-polarity input modes in the noise measurement. The electronics noise originates from the thermal noise of the resistors and intrinsic noise of the op amp. A resistor value ($R_{\text{discharge}}$ and R_{L}) less than 50 kΩ is recommended to achieve a better electrical performance.

Figure 10 shows the typical signal waveforms and discharging waveforms in the linearity test for the negative and positive charge injections, respectively. The results of the linearity test for the dual-polarity charge channels are shown in Fig. 11. The correlation coefficient R of the linear least-squares estimate expresses the degree of linear correlation between the two parameters. Therefore, R^2 is referred to as the linearity of the least-squares estimate. To compare the differences between the positive and negative channels, half of the 64 channels were configured as the negative-polarity input mode and the other half were configured as the positive polarity. The linearity results for the positive and negative channels are slightly different, as shown in Fig. 11. The intercept difference for both channels originates from nonuniform baselines under different configurations, which can be easily corrected when necessary. However, both exhibit excellent linearity, with correlation coefficients $R^2 = 0.998$. From Eq. (2), it can be seen that fewer factors have an impact on the linearity compared with traditional readout electronics, including preamplifiers, main amplifiers, and ADCs [37]. Figure 12 shows the slope distribution of the 32 positive-polarity channels and 32 negative-polarity channels. The means and standard deviations of the fitted slopes for the positive and negative channels were 0.786 ± 0.009 and 0.795 ± 0.008, respectively. The linearity results showed excellent uniformity over the 64 channels. In the subsequent detector experiments, there was no electronics calibration and correction.

5.2 Detector results

Figure 13 shows typical crystal discrimination maps made of 15×15 arrays of 1.5 mm × 1.5 mm × 20 mm LYSO crystals irradiated by a Na-22 point source. All crystals can be

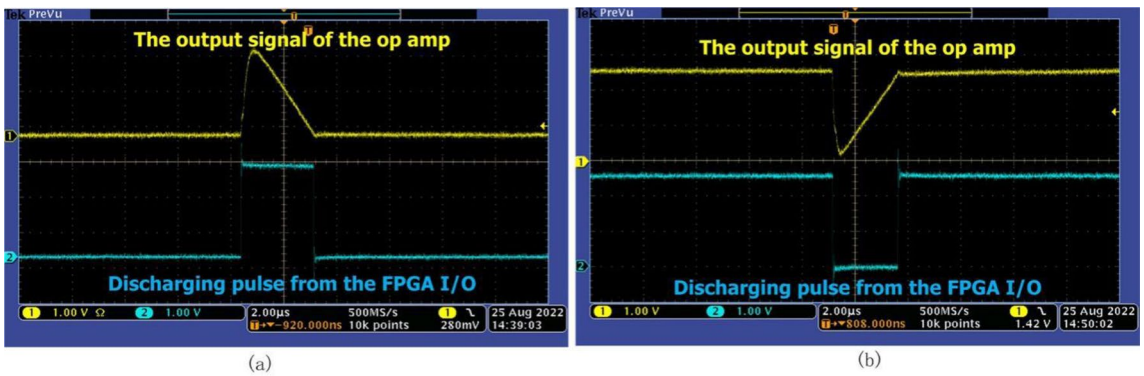

Fig. 10 (Color online) Typical waveforms of the dual-polarity QDC for the negative **a** and positive **b** charge measurements

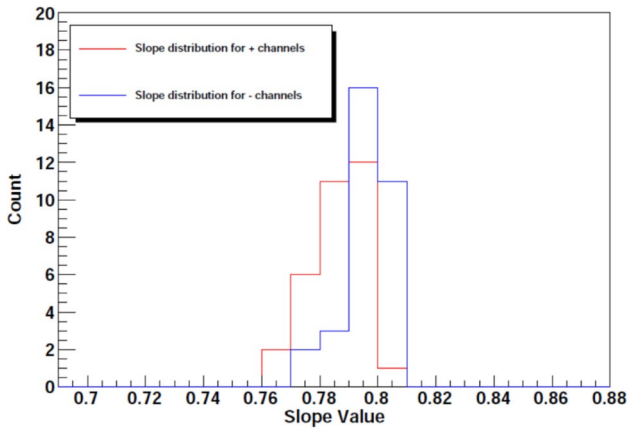

Fig. 12 (Color online) Slope distributions for all positive- (red) and negative-polarity (blue) channels. (Color figure online)

clearly distinguished. The left one is under the condition of the first detector configuration in which 64-channel anode signals are read out for positioning. The middle one is under the second detector configuration that shows a selected row for both maps. The profile analysis indicates that the peak-to-valley ratios (PVRs) under both detector configurations are 12.1 and 14.4. These results indicate that the designed FEE system has an excellent readout ability for dual-polarity current signals.

Figure 13(c) shows a one-end crystal map of a 15×15 LYSO crystal array coupled with two $8+8$ SiPMs at the two ends. A one-row profile was also plotted. The profile analysis indicates that the average PVR under the $8+8$ SiPM readout configuration is 13.5. The dual-end readout for the LYSO array results in a good energy spectrum for PET development. The energy spectrum analysis shows that the energy resolutions of 511-keV gamma photons for all crystals range from 14.4 to 18.2%. It worsens at the edges of the map because of light leakage. Figure 14 shows a typical energy spectrum for the selected crystal, where the energy resolution for the 511-keV gamma is 16.8%. Notably, only negative-charge signals were applied to the dual-end energy summation. Overall, the dual-polarity QDC exhibits good performance in terms of noise, linearity, and uniformity. In the electronics tests, the selected trigger thresholds for the negative and positive charge measurements are 30 mV and 2.47 V, respectively. The difference between the trigger threshold and output baseline of the op amp is 30 mV for both negative and positive charges. Based on the electronics noise, it can be decreased to 10 mV, contributing to the timing pickoff when enabling fine-time measurement.

In the Cyclone V FPGA, the pulse width after the LVDS comparator is digitized by a coarse counter driven by a 200-MHz system clock. The discharging resistor $R_{\text{discharge}}$ is 10 kΩ. From Eq. (2), we obtain:

$$Q_{\text{LSB}} = \frac{V_{\text{IO}}}{R_{\text{discharge}} \times F_{\text{S}}} = 1.25\,\text{pC}. \tag{7}$$

The discharging resistor $R_{\text{discharge}}$ can be increased to obtain better measurement accuracy. However, this widens the discharge time. During discharge, the QDC circuit cannot accept another signal [28]. A tradeoff should be made between the accuracy and count rate.

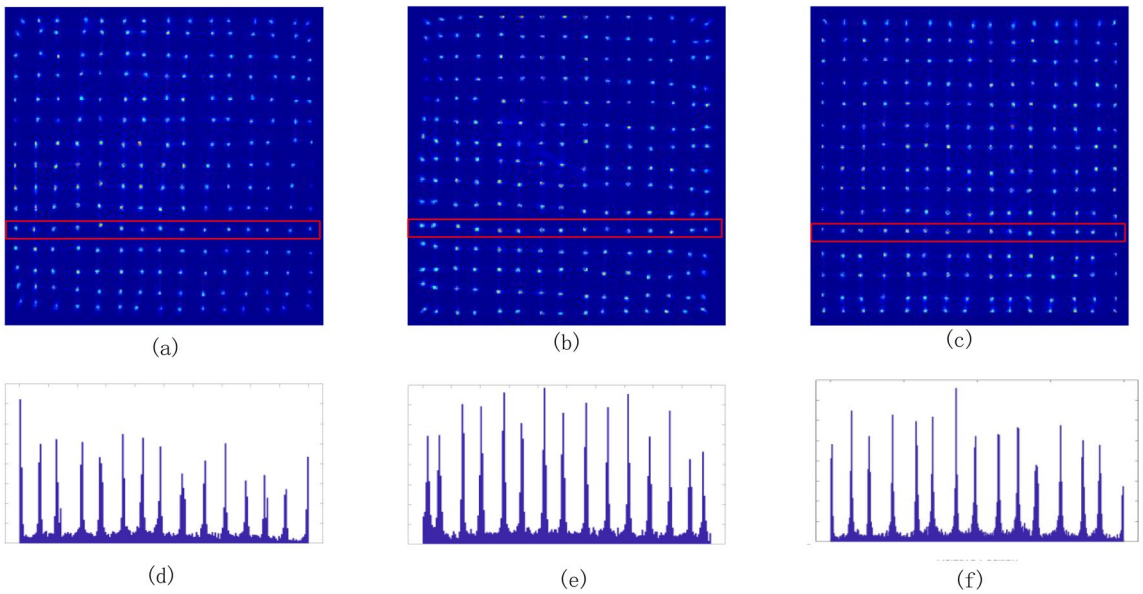

Fig. 13 (Color online) Crystal discrimination maps under first **a**, second **b**, and third **c** readout configurations. **d** The profile plot of selected row in the map (**a**). **e** The profile plot of selected row in the map (**b**). **f** The profile plot of selected row in the map (**c**)

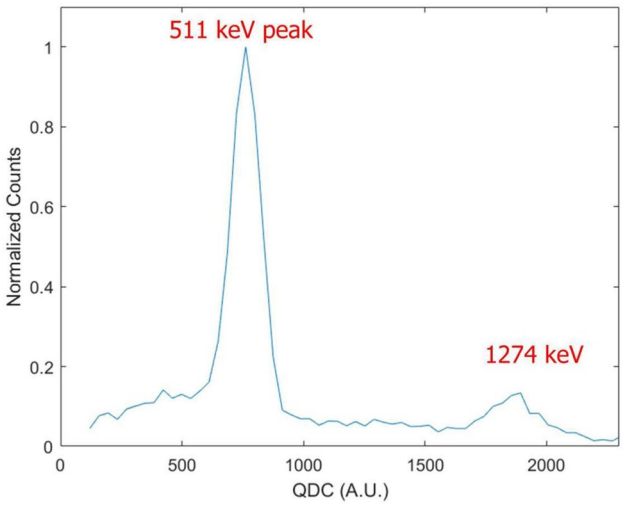

Fig. 14 Typical energy spectrum of the selected crystal in the crystal discrimination map

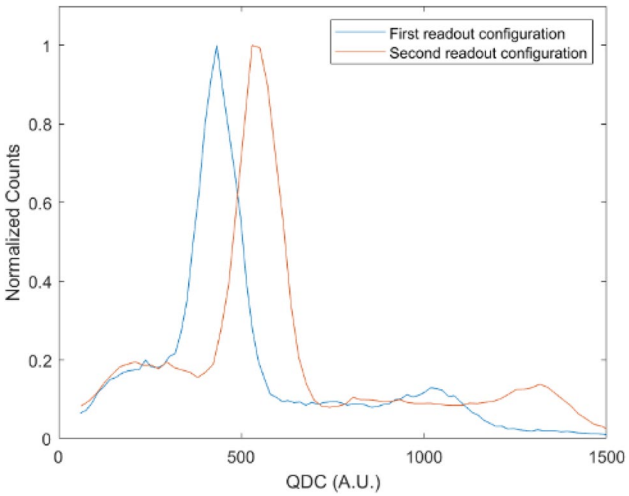

Fig. 15 Energy spectrum of the selected crystals under the first and second readout configurations

In the detector experiments, three readout configurations of the PET detector were applied to verify the capability of the dual-polarity QDC circuit. The single-end readout for the LYSO array was applied in the first two configurations. After detecting a gamma event in the LYSO crystal bar, the generated light signals were transmitted along the bar. For the single-ended readout, one part of the light is detected by the corresponding SiPM pixels. The other part is transmitted along the crystal bar and reflected by the Teflon tape. Finally, the reflected light is received by the SiPM pixels. Compared to the dual-end readout of the LYSO array in the third readout configuration, more light escapes from the crystal bar in this case. Light loss degrades the energy resolution of both the configurations. The calculated energy resolutions in the first two configurations range from 24 to 30%. Figure 15 shows the typical energy spectrum of the selected crystals in the first two configurations. The energy spectrum was obtained by the summation of the 64-channel positive signals in the first readout configuration, whereas the 64-channel negative signals were used in the second readout configuration. Notably, the peak value of the 511-keV photon for the positive charge is less than that for the negative charge. This is because the holes have a shorter drift length. The severe trapping of the holes in the semiconductor detector decreases the induced signal on the electrode [38].

6 Conclusion

With the continuous development of SiPM technology, FEE systems for SiPM signal processing are highly sought after in many research fields. By taking advantage of the FPGA-based QDC scheme, a compact 64-channel FEE system for a SiPM-based radiation detector was designed and developed. FEE can process dual-polarity charge signals from detectors and shows good electronics performance in terms of noise, linearity, and uniformity. A PET detector with different readout configurations was used to evaluate the FEE. Under three readout configurations, the PET detector could be read out with good crystal discrimination maps. Good energy resolutions are obtained under the dual-end readout configuration. Overall, the FPGA-QDC-based FEE is promising and has potentially useful applications in SiPM-based radiation detectors.

Author contributions All authors contributed to the study conception and design. Material preparation, data collection and analysis were performed by Yu-Ying Li, Chang-Yu Li and Kun Hu. The first draft of the manuscript was written by Kun Hu and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

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