



# Design of an energetic particle radiation diagnostic spectroscopy system based on national core chips and Qt on Linux in EAST

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**Abstract** Energetic particle radiation diagnoses mainly detect the particles (such as neutrons, gamma rays, hard X-rays, and escaping electrons) that are radiated in the discharge process of the experimental advanced superconducting tokamak device to characterize the operating state of the plasma in real time. The upgrading of these diagnoses requires new instruments based on national (here, “national” means developed and produced by a Chinese company) core chips and open-source software with advanced digitization, a high sampling rate, and a high time resolution. The new spectroscopy system designed in this study adopts the national field-programmable gate array (FPGA) and an analog-to-digital converter as the core chip, and it is developed using Qt on Linux. The communication between the FPGA and embedded controller occurs via a high-speed peripheral component interconnect eXtension for instrument express protocol with a direct memory access mode. On this basis, the time resolution of the system is improved from 2 to 1 ms, the maximum channel address is increased to 4096, and the sampling rate is increased from 10 to 80 Msps. Calibration experiments of the spectroscopy system with <sup>152</sup>Eu and <sup>137</sup>Cs sources

demonstrate that the best energy resolution is 0.27% and the measurement error is less than  $\pm 0.5$  keV.

**Keywords** Spectroscopy system · National chip · Qt · Energetic particle radiation · Experimental advanced superconducting tokamak

## 1 Introduction

The experimental advanced superconducting tokamak (EAST) is the most advanced experimental superconducting tokamak platform in China [1, 2]. Several new operating parameter records have been achieved by EAST since the first discharge operation in 2006; for example, 100-s pulse H-mode steady-state operation was realized in 2017 [3, 4], and the plasma center electron temperature reached one million degrees ( $T_{e0} = \sim 10$  keV) in 2018 [5]. Notably, certain components of the device aged as the service lifetime increased [6].

To enable upgrading of the plasma diagnostic system and plasma control system (PCS), the accuracy and stability of these diagnoses should be improved, and the PCS feedback control speed should be increased to realize real-time and stable control [7]. In these diagnoses, the energetic particle radiation diagnostic spectroscopy (EPRDS) system is important for measuring the energy spectrum of the radiated particles (such as neutrons, gamma rays, hard X-rays, and escaping electrons) during the discharge process of the EAST device to characterize the operating state of the plasma in real time, or to calculate and retrieve various important operating parameters and behavior states of the plasma [8–12]. EPRDS system upgrades should employ national instruments that are based on national core

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chips (i.e., chips that are produced by Chinese companies), including a field-programmable gate array (FPGA) and an analog-to-digital converter (ADC), as well as open-source software. Advanced digitization, a high sampling rate, and a high time resolution are required in the development of these national instruments to replace imported instruments. Furthermore, the data acquisition speed, data communication speed, and response efficiency of the central control system must be improved.

Considering the above requirements, in this study, an EPRDS system with significant improvements is developed, as follows: (A) To achieve rapid feedback control of the PCS and high-precision measurement of the diagnoses, new network and hardware architectures are installed, as described in Sect. 2. (B) The national FPGA and ADC chips are employed instead of the imported chips in the EPRDS hardware design, as outlined in Sect. 3. (C) The peripheral component interconnect eXtension for instrument express (PXIE) bus is adopted in the international thermonuclear experimental reactor (ITER) to design the diagnosis development hardware platforms [13]. On this basis, the PXIE bus is used for the EPRDS design. The direct memory access (DMA) [14] mode of the PXIE bus on Linux is implemented as the communication mode of the EPRDS system, instead of the programmed input–output mode of the PXIE bus on Windows. This change can significantly improve the data transmission speed, as explained in Sect. 4. (D) Qt [15], which is open-source software, is used on Linux in the design of the EPRDS system instead of LabVIEW, which is used for the original electronics of energetic particle radiation diagnoses, as described in Sect. 5. (E) The time resolution of the system is improved from 2 to 1 ms for the enhanced study of ion-transport processes and rapid electron behaviors. Furthermore, the maximum channel address reaches 4096 and the sampling rate is increased from 10 to 80 Msps [11]. In the experiments, the highest energy resolution is 0.27% and the measurement error is less than  $\pm 0.5$  keV, as outlined in Sect. 6.

## 2 Architecture design

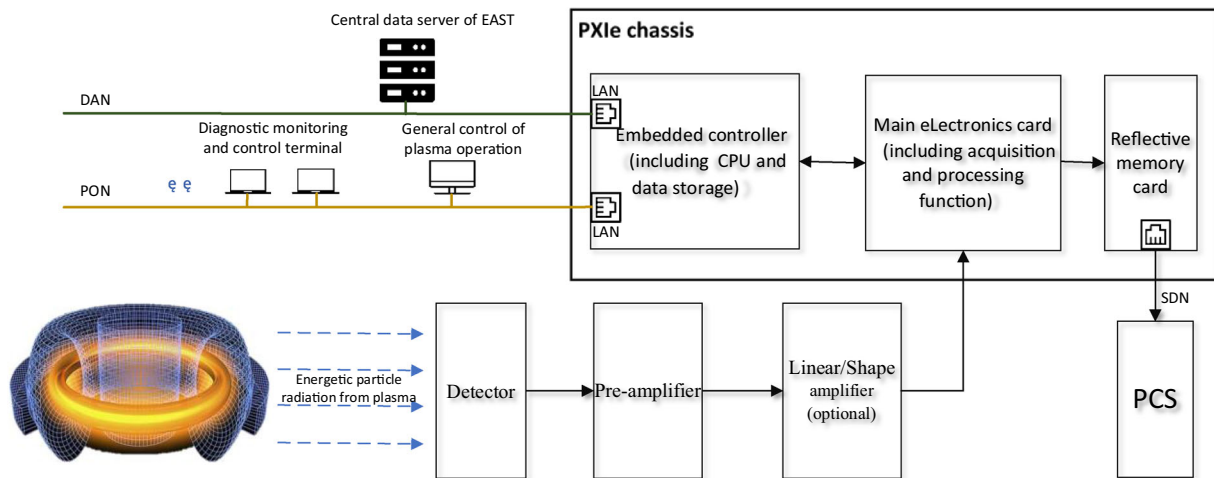
The EPRDS system mainly consists of a detector, pre-amplifier, linear/shape amplifier (optional), main electronics card that includes data acquisition and processing functions, reflective memory (RFM) card, PXIE chassis with an embedded controller, and computer software, as illustrated in Fig. 1. The radiation of energetic particles from the plasma discharge process in EAST is detected by the detector, which produces a charge or current signal. The charge or current signal is transformed to a voltage signal, which is immediately amplified by the pre-

amplifier. A linear/shape amplifier is used for signal programmable control amplification, shaping, and filtering. Subsequently, the signal is acquired and processed by the main electronics card. The final measurement result data are transmitted to the embedded controller through the PXIE bus on the back-plane of the chassis for temporary data storage. The RFM card is used for real-time experiment data transmission from the main electronics card to the PCS. As components of the EPRDS system, a commercial off-the-shelf or custom-made detector was selected according to the measurement object; a CPCI-5565PIORC card, which was manufactured in China, was used as the RFM card; a portable PXIE chassis with an embedded controller was designed in partnership with a manufacturer, and this national rugged chassis was deemed suitable for field experiments with one main controller slot and eight PXI/PXIE full hybrid expansion slots; and the pre-amplifier, linear/shape amplifier, and main electronics card were all designed by our group [16].

The network architecture design for the data transmission and control commands is based on the ITER Control, Data Access, and Communication (CODAC) system [17]. The embedded controller in the PXIE chassis is separately connected to the data archive network (DAN) and plant operation network (PON) through two network ports. The RFM card is connected to the synchronous databus network (SDN). The massive experimental data that need to be uploaded to the EAST central data server from the embedded controller in the PXIE chassis of each diagnosis are transmitted through the DAN [18]. The control command (including the discharge shooting number, discharge time, amplification, and countdown) and configuration information of each diagnosis are sent to the embedded controller in the PXIE chassis from the central control computer of the plasma operation through the PON. The status parameters are read back from the diagnostic acquisition chassis controller through the PON.

The PCS uses the SDN for rapid data transmission and feedback control. The SDN is realized using the RFM card or a 10-gigabit network based on optical fiber communication [19, 20]. Although the RFM card can also be used for multipoint networking and convenient data transfer without the intervention of the embedded controller, its memory space is limited (128 MB/256 MB) and its upper transmission speed limit is 170 MB/s; therefore, to increase the transmission rate in the future, communication based on a 10-gigabit network card will be more suitable. The DAN uses a gigabit local area network (LAN) or 10-gigabit LAN. As the PON is not a fast data transmission network, a 100-megabit network is sufficient in the current state.

Owing to the thermal, electromagnetic, and nuclear radiations in the EPRDS operating environment, certain front-end functional devices (including the detectors and



**Fig. 1** (Color online) Schematic of the EPRDS architecture

pre-amplifiers) need to be designed with a cooling system, magnetic shielding box, and nuclear shielding box [21–23]. For the hardware design of the main electronics card, the FPGA code programming and computer software for the EPRDS system are mainly improved based on their compatibility with the hardware architecture of the traditional spectroscopy system in EAST.

### 3 Hardware circuit design

The design of the main electronics card that includes acquisition and processing functions is based on the PXIe bus architecture. Moreover, the core chips that are used in the hardware circuit of the main electronics card, including the FPGA and ADC, are manufactured in China. This enables Chinese institutes to contact the manufacturing company to obtain information on the circuits and development tools with ease, as well as to carry out cross-development and collaboration. An ADC (type: YA16D80L [24]) with an 80 Msps sampling rate and a 16-bit resolution was selected. A high-performance and irradiation-resistant FPGA (type: JFM7K325T [25]) was used in the core logic processing and computing unit. The main electronics card typically contains four synchronized analog input channels and a hardware trigger input interface, as illustrated in Fig. 2.

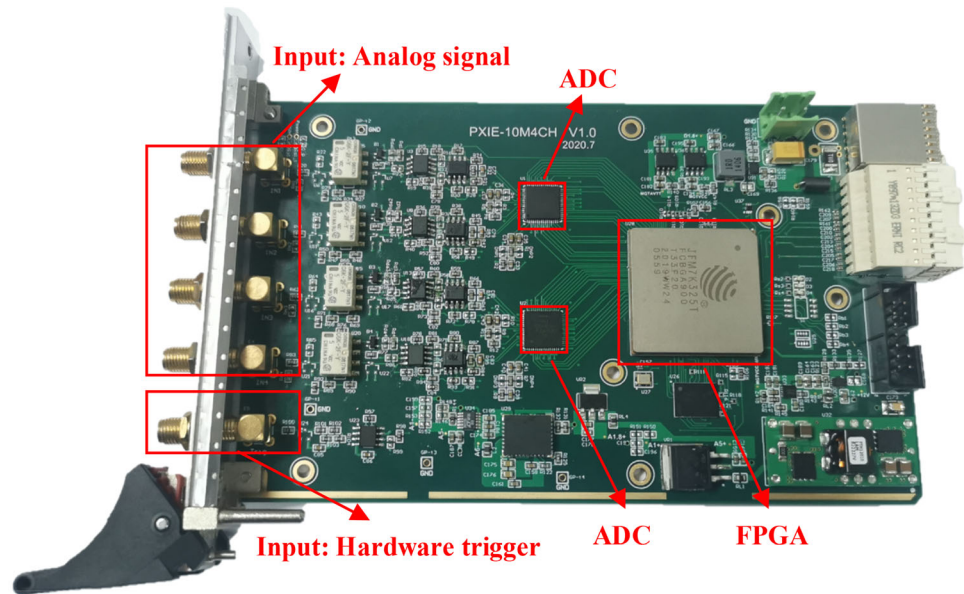
JFM7K325T is widely used in the aerospace, communications, and other scientific areas. The linear energy transfer threshold of JFM7K325T for a single event latch-up is greater than  $84 \text{ MeV cm}^2/\text{mg}$ . Its pin definition, pin distribution, and packaging are compatible with XC7K325T [26] from Xilinx (USA). However, the performance differs slightly. The advantage of JFM7K325T is that it uses the GTX core ( $1.0 \text{ V} \pm 3\%$ ), which is more

widely applicable than that in XC7K325T (when the data rate  $\leq 10.3125 \text{ Gbps}$ , the bias range =  $0.97\text{--}1.08 \text{ V}$ ; when the data rate  $\geq 10.3125 \text{ Gbps}$ , the bias range =  $1.02\text{--}1.08 \text{ V}$ ). Conventionally, JFM7K325T can operate at  $1.0 \text{ V}$  with a normal bias at high data rates, and there is no need to differentiate the power supply requirements according to the data rates. The disadvantage of JFM7K325T is that the functions of the DXN and DXP pins are not available; therefore, it needs to be suspended or grounded. CSI\_B, RDWR\_B, and FCS pins can only be used for configuration functions and not for general IO functions. However, these functions do not affect the design of the main electronics card for data acquisition and processing [27].

YA16D80L is a double-channel ADC that must be configured by the serial peripheral interface (SPI) protocol, following which the acquired data are sent to the FPGA by parallel data transmission. Its pin definition and packaging are compatible with those of AD9269 [28] from Analog Devices (USA); however, the signal-to-noise ratio (SNR) of YA16D80L is slightly higher than that of AD9269. The SNR of AD9269-80 is  $76.3 \text{ dFs}$ , whereas that of YA16D80L is  $77 \text{ dFs}$ , when  $F_{in}$  is  $70 \text{ MHz}$ . The SNR of AD9269-80 is  $77.6 \text{ dFs}$ , whereas that of YA16D80L is  $79 \text{ dFs}$ , when  $F_{in}$  is  $9.7 \text{ MHz}$ . This national ADC is produced as part of a series, the products of which have the same pin definition, packaging, and configuration methods. Among the series of national ADCs, YA16D125 (sampling rate:  $125 \text{ Msps}$ ; resolution: 16-bit) is the fastest.

A relay (type: g6k-2f-y-tr dc12) is used to switch the input signal amplitude range from  $-1 \text{ V}$ – $+1 \text{ V}$  to  $-10 \text{ V}$ – $+10 \text{ V}$ . However, when the relay is in the energized state, it produces weak electromagnetic radiation, which increases the noise of the input analog signal. The influence of electromagnetic radiation on the input analog signal can be reduced by adjusting the wiring position of

**Fig. 2** (Color online)  
Photograph of the main  
electronics card



the analog signal line (thereby ensuring that it does not pass under the relay) and by adding a filter capacitor to the No. 8 pin of the relay.

The power-on sequence and power consumption of different voltage rails for the FPGA are considered in the design of the power supply module for the main electronics card. By controlling the power-on sequence, the FPGA can operate more stably and its service life can be increased.

In the PCB design, the analog ground (GND) and digital GND are effectively separated, and the analog GND of the analog signal for each channel is independent. Finally, the addition of a 100-MHz inductor between the analog GND and digital GND can effectively improve the SNR of the collected effective signals.

#### 4 FPGA code design

JFM7K325T can be programmed using the Procise [29] or Vivado [30] software, or a combination of both.

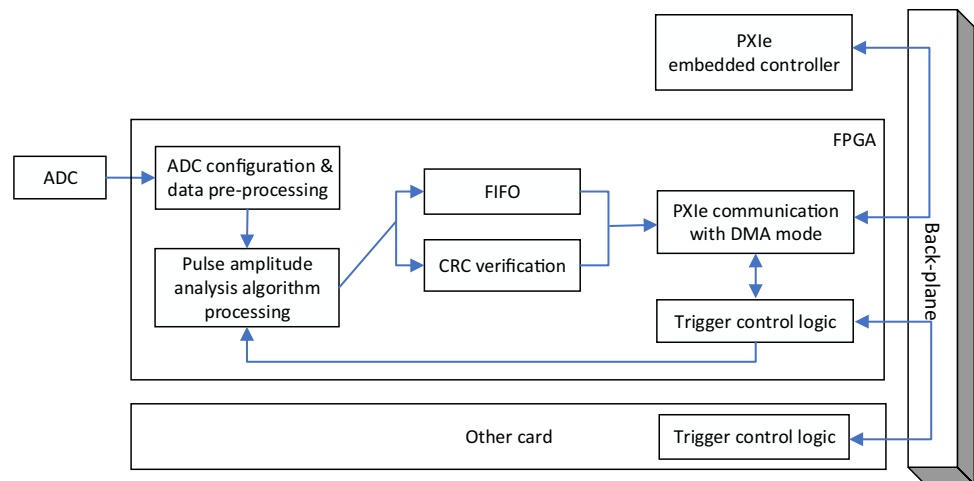
Procise, which is a new generation of the million-gate-level FPGA supporting development tool, is the first national very large-scale integration process electronic design automation software. It is a completely independent research and development design tool with a user-friendly interface. It is powerful and easy to use and can provide large-scale FPGA including the entire process of automatic design services and can be integrated with numerous IP resources. These features can aid users in the rapid development of application solutions. Verilog and VHDL can both be used in the design of the FPGA code for Procise. Verilog was used in the design of the FPGA code for the EPRDS system.

The logic structure design of the FPGA in the main electronics card, which is depicted in Fig. 3, mainly includes the ADC configuration and data pre-processing module, pulse amplitude analysis algorithm processing module, first input first output (FIFO) module, cyclic redundancy check (CRC) verification module, PXIe communication module with the DMA mode, and trigger control logic module.

The ADC configuration and data pre-processing module mainly completes the SPI communication and register configuration for the ADC. Furthermore, this module converts high-speed raw data into pre-processed data that can be recognized by the subsequent module according to the defined rules. The ADC configuration and data pre-processing module uses a synchronization clock with the pulse amplitude analysis algorithm processing module, the data processing methods of which mainly include peak search processing and subsequent time-sharing counting of the corresponding channel address. The advantage of this method is that the time resolution and channel address can be set by the user; the best time resolution is 1 ms, and the maximum channel address is 4096. FIFO is the data cache and clock adjustment module that is located between the pulse amplitude analysis algorithm processing module and the DMA mode of the PXIe communication module. The DMA mode of the PXIe communication module adopts high-speed data packet transmission, which is controlled by interrupts. Furthermore, the mode must cooperate with the driver module of the computer. The CRC verification module carries out CRC verification on the data that need to be sent, and the results of the CRC verification algorithm are sent to the PXIe communication module as the tail part of a packet and FIFO data. The control logic trigger



**Fig. 3** The logic structure design of the FPGA in the main electronics card



module is bidirectional; that is, if the card is a master card, it can receive a hardware trigger signal from the trigger input and convert it into the back-plane trigger (the trigger 0 pin in the back-plane), which can trigger the other slave card to operate simultaneously. If the card is a slave trigger card, the card can receive a hardware trigger signal from the back-plane, following which it triggers the pulse amplitude analysis algorithm processing module and PXIe communication module to work simultaneously.

To facilitate user debugging and testing, an oscilloscope mode is included in the FPGA code, which has the same functions as the normal four-channel oscilloscope, including the automatic, single trigger, and continuous trigger modes. The sampling rate, trigger source, trigger threshold, and trigger location can also be set by the user.

A digital baseline recovery function is added to the FPGA code and the computer software of the ERRDS system to eliminate the influence of the hardware circuit baseline offset, and the baseline can be adjusted to almost zero through calibration.

The IP\_patch, bit patch, and burn patch should be incorporated into the Vivado software for the JFM7K325T, according to the functional requirement of the FPGA. The procedure is as follows: (A) Once the synthesis step is completed, the command to run the IP\_patch tool is entered in the TCL command input box of Vivado. The tool will automatically modify the differences in the IP and network table to adapt to JFM7K325T. Several differences exist between JFM7K325T and XC7K325T in the high-speed transceiver circuit: The TXOUT\_DIV/RXOUT\_DIV of JFM7K325T can only be set to 1 and not to 2, 4, 8, or 16; conversely, for XC7K325T, the value can be set to 1, 2, 4, 8, or 16. Furthermore, there are differences in the CTLE tail current configuration: XC7K325T defaults to 1, whereas JFM7K325T must be configured to 0. Consequently, the PCIe core of Vivado does not work properly with JFM7K325T; thus, an IP\_patch is required to

accommodate the use of a high-speed transceiver in JFM7K325T [27]. (B) Following the first step, the traditional step for generating the bit file proceeds. Finally, the original bit file is converted by Procise to generate a new bit file, based on which mcs and other burn files are generated.

## 5 Software design

The EPRDS software is designed using Qt on Linux. The main reason for this is that Linux and Qt are open-source software platforms, and the possibility of copyright restriction is relatively low. Qt is a cross-platform C++ GUI library. It includes Qt Creator, Qt Embedded, Qt Designer, Qt Linguist, Qt Assistant, and Qt Make. It also supports all Linux/UNIX systems, Windows platforms, Solaris, iOS, and others, with excellent cross-platform features. Its effective encapsulation mechanism accounts for its very high modularization degree and strong reusability; therefore, Qt is highly suitable for user development. As an excellent GUI programming platform, Qt can enable application developers to establish an artistic graphical interface function design, based on modularization and object orientation, to enhance its extensibility.

Moreover, the processing efficiency of Linux is higher than that of Windows in real time; thus, it is preferable for high-speed feedback control [31–33]. Finally, in the future the diagnosis of the energetic particle radiation will be designed using the experimental physics and industrial control system (EPICS) on Linux. In this study, Qt on Linux is used to complete the system design, driver development, software testing, and system coordination, thereby creating a technical foundation for the development of the EPICS system using the Linux platform.

## 5.1 Software functions and interface design

The design of the EPRDS software interface is depicted in Fig. 4. The software interface includes four functional modules: parameter configuration, energy spectrum display, data recall and display, and status monitoring.

The parameter configuration module has many functions: (A) enabling and disabling the connection of hardware devices; (B) manual starting and stopping of the spectrum measurement; (C) configuration of the channel address, time resolution, noise threshold, and 10 times attenuation; (D) data compression, data storage, and hardware trigger settings; and (E) reception of UDP experimental information from the diagnostic central control, including the discharge shooting number, discharge time, and countdown.

The energy spectrum display interface can display a four-channel energy spectrum diagram with different colors simultaneously; alternatively, the user can select an interesting channel energy spectrum diagram to display. The user can select the time-sharing spectrum or total spectrum to display, as well as accumulate the time-sharing energy spectrum of any period into the total spectrum. In the upper-left corner of the energy spectrum display interface, information regarding the card appears, including the bus number, slot number, and function code. In our improved design of the FPGA code and software, the embedded controller identifies different cards using the slot and bus numbers on the chassis to determine where the cards are inserted, rather than identifying the ID number of the cards directly. This implies that cards with the same function use the same product ID number; thus, the same FPGA code and software driver are used for the same

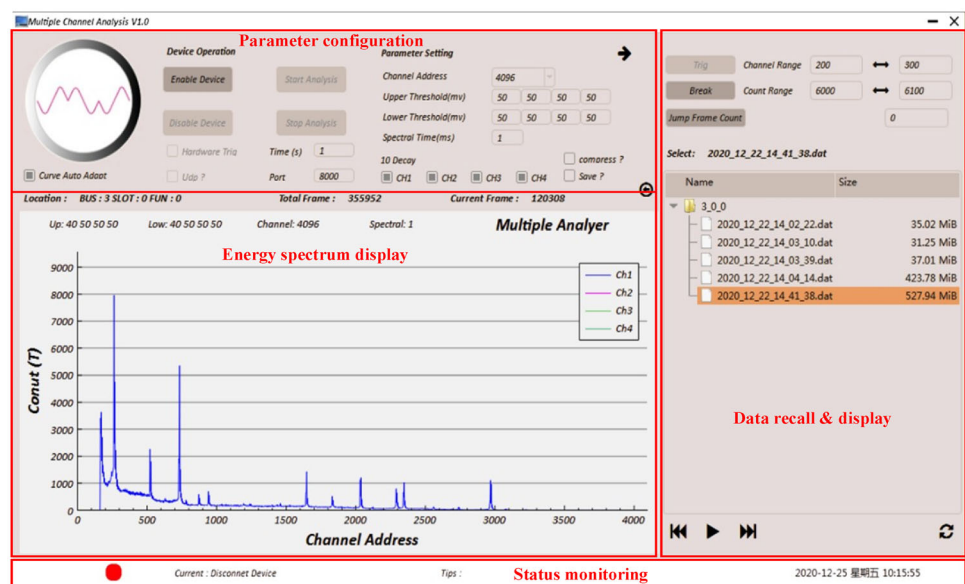
product. The data recall module can display the entire data measurement process through the broadcast or accelerated broadcast function, and it allows users to select the data segment in which they are interested in using for the data trigger method. The trigger range of the channel address and trigger threshold for the count can be set for the trigger condition. The status monitoring module indicates the system mode, that is, the system operation mode, system stop mode, or data recall mode. Furthermore, it indicates the hardware connection status, error log during the system operation, date, and time.

An arrow pointing to the right can be observed in the upper-left corner of the parameter configuration module. This arrow is clicked to switch to the oscilloscope function interface for signal debugging or system testing. In the oscilloscope mode, the original signal characteristics that are acquired by the FPGA in the main electronics card can easily be displayed, including the amplitude, width, frequency, baseline offset, and noise.

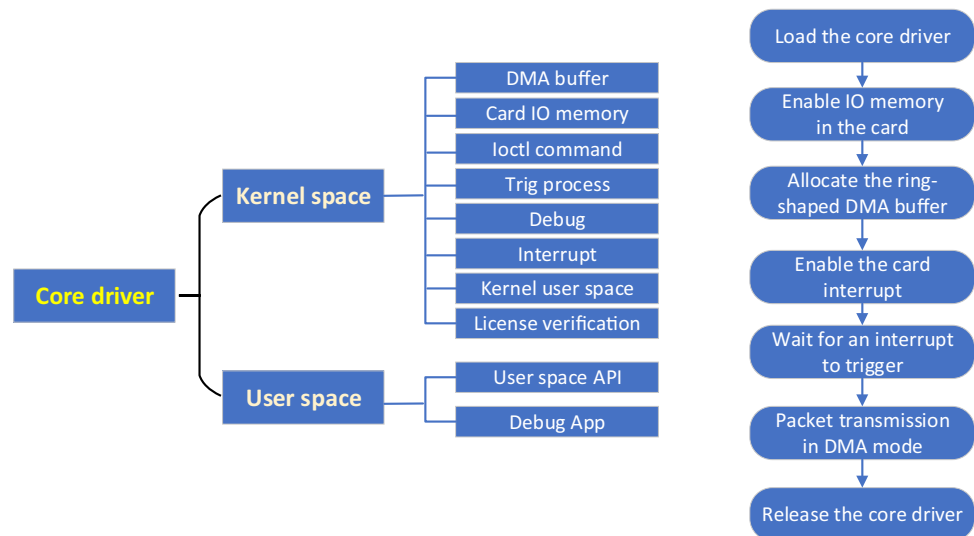
## 5.2 Hardware driver development on Linux ring buffer

Hardware driver development on the Linux platform is a core aspect of software development. The structure and operation logic flowchart of the designed core driver module is presented in Fig. 5. The driver consists of the kernel space and user space. The kernel space includes the DMA buffer module (the allocation of a ring DMA buffer for data transmission), card IO memory module (the register space for the card), Ioctl command module (the interaction between the user and kernel layers), Trig process module (the trigger control for the back-plane in the

**Fig. 4** (Color online) The design of the EPRDS software interface



**Fig. 5** The structure and operation logic flowchart of the designed core driver module



chassis), debug module (the debug information of the user and kernel layers, which is sent to the debug APP), interrupt module (interrupt handling for the card), kernel user space module (which maps the DMA and IO memory to the user space), and license verification (which verifies the license used in the driver). The user space includes the user space API module (for the rapid development of user API functions) and the debug API module (for printing debugging information).

The operation logic flow of the hardware driver on the Linux system is divided into the following six steps: (A) the core driver is loaded, (B) the IO memory in the card is enabled, (C) the ring DMA buffer is allocated, (D) the interrupt function of the card is enabled, (E) triggering of an interrupt is awaited, (F) packet transmission occurs in the DMA mode, and (G) the core driver is released.

## 6 Experimental research

Following completion of the hardware circuit, the FPGA code and computer software for the EPRDS system were developed, and system debugging was carried out in the energetic particle diagnostic laboratory. Subsequently, performance tests and a gamma radiation experiment were conducted to evaluate the performance parameters of the main electronics card. The tests included linear, full width at half maximum (FWHM), long-term stability, noise, DMA mode transmission rate, and synchronous running of several cards tests. The gamma radiation experiment was used to verify the combination properties of the EPRDS system, such as the energy measurement error and energy resolution.

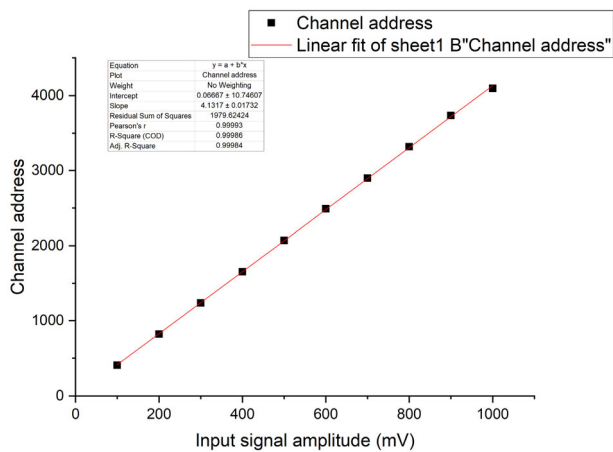
### 6.1 Performance test

The standard test was adopted to analyze the performance of the EPRDS system [11], and the parameters of the EPRDS are configured as follows: (A) The dynamic range of the input signal was set in the range of  $-1\text{ V}$  to  $+1\text{ V}$ ; (B) the maximum channel address was set to 4096; (C) the time resolution was set to 1 ms; and (D) the noise threshold value was set to 20 mV.

A signal generator was employed for the linear test of the EPRDS. The signal frequency was 10 kHz, the rise time of the edge was 500 ns, the fall time of the edge was 500 ns, and the pulse width was 2  $\mu\text{s}$ . Furthermore, the amplitude was changed from 100 to 1000 mV with a step size of 100 mV. As a result, the channel addresses of the energy spectrum peaks were 406, 820, 1237, 1653, 2071, 2490, 2900, 3318, 3734, and 4095 when the input signal amplitudes were 100, 200, 300, 400, 500, 600, 700, 800, 900, and 1000 mV, respectively. The linear correlation coefficient (R) of the pulse height and channel address was 0.999, as indicated in Fig. 6. The FWHM of each pulse in the spectrum was calculated. In the range of the 4096 channel addresses, the FWHM of the main electronics card was not higher than three channel addresses. Therefore, the channel address (energy) resolution of the main electronics card of EPRDS was 0.073% ( $3 \div 4096 = 0.073\%$ ).

For the long-term stability test, a signal generator was used to generate a 5-V TTL trigger signal with a time interval of 1000 s. The EPRDS system was operated continuously for 10 s at a time, and the data were saved automatically. The experiment lasted for 168 h, and 604 sets of data were recorded. No data loss occurred.

For the tests of the DMA mode data transmission rate and the synchronous running of several cards, the test data were generated by FPGA and the highest data transmission



**Fig. 6** Linear fit of the input signal amplitude and energy spectrum channel address

rate of the EPRDS was tested, which reached up to 320 MB/s. The maximum parameters of the synchronous operation of multiple main electronic cards could support 16 cards ( $4 \times 16 = 64$  channels), with a time resolution of 1 ms, 2048 channel addresses operating normally, and no data loss. At this moment, the total data size could reach up to 262 MB/s ( $16 \text{ bits} \times 2048 \times 1000 \times 64 \div 8 \approx 262 \text{ MB/s}$ ). The protocol overhead was not calculated.

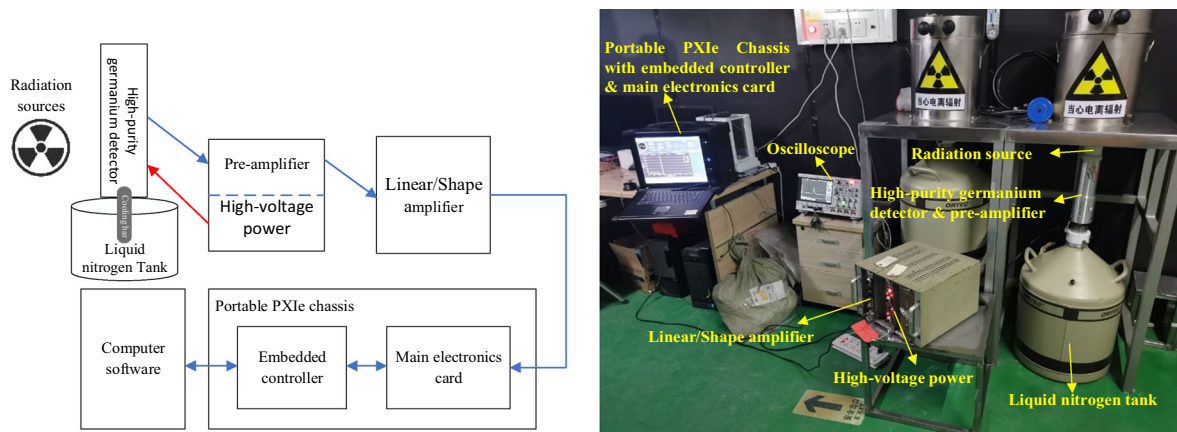
In the oscilloscope mode test, the peak–peak voltage ( $V_{p-p}$ ) noise of the main electronics card was approximately 2 mV, and the baseline offset was no higher than  $\pm 3$  mV for all of the analog input channels.

## 6.2 Gamma radiation experiment

The gamma radiation experiment was performed with  $^{152}\text{Eu}$  and  $^{137}\text{Cs}$  radioactive sources. A diagram and photograph of the experimental system in the laboratory are presented in Fig. 7. The measurement system of the experiment comprised a high-purity germanium detector,

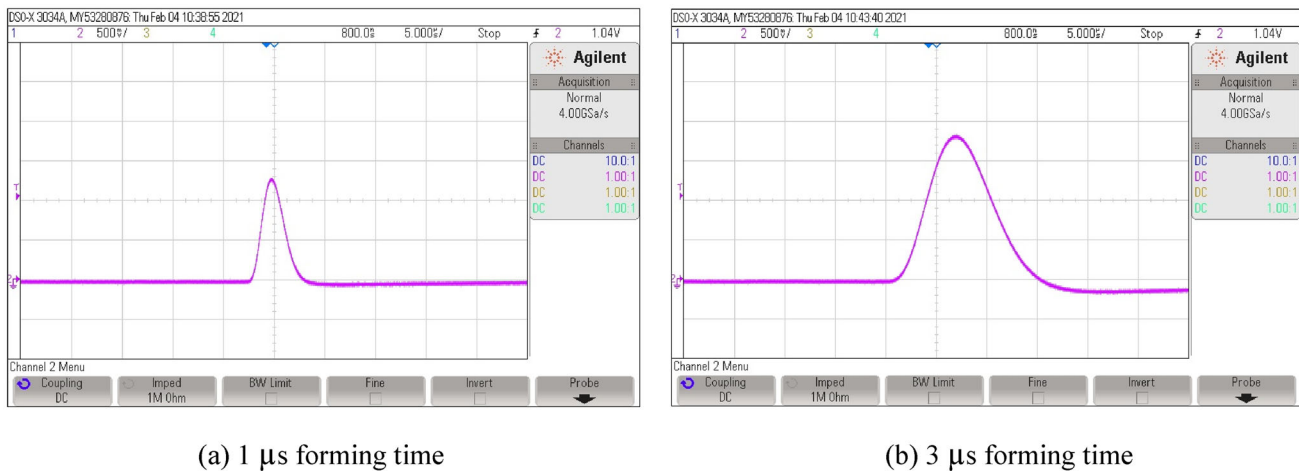
high-voltage power supply, pre-amplifier, linear/shape amplifier, main electronics card, portable PXIe chassis with an embedded controller, and supporting computer software. The high-purity germanium detector (type: GEM40-76-PL) from ORTEC (USA) must be cooled by a cooling bar that is inserted in the liquid nitrogen tank at a low temperature to reduce the thermal noise. The pre-amplifier adopts charge integral amplification, and the linear/shape amplifier has gain control and pulse-forming functions. The high-voltage power supply was set to 2000 V. The  $^{152}\text{Eu}$  and  $^{137}\text{Cs}$  radiation sources could emit gamma rays spontaneously. The high-purity germanium detector detected the gamma radiation signals and converted these into pulse current signals. The detector output signal was amplified and formed by the pre-amplifier and linear/shape amplifier, following which it was transformed into a nearly Gaussian voltage pulse signal, as illustrated in Fig. 8. Figure 8a depicts the signal waveform outputted by the linear/shape amplifier with a 1  $\mu\text{s}$  forming time. The half-height width of the pulse signal was approximately 2.5  $\mu\text{s}$ , and the pulse amplitude was 1.3 V. Figure 8b presents the signal waveform outputted by the linear/shape amplifier with a 3- $\mu\text{s}$  forming time. The half-height width of the pulse signal was approximately 8  $\mu\text{s}$ , and the pulse amplitude was 1.8 V. The output signal of the linear/shape amplifier was directly entered into the main electronics card for energy spectrum measurement, and the final result was transmitted to the embedded controller through the PXIe bus for display and storage.

The  $\gamma$ -radiation spectrum of the  $^{152}\text{Eu}$  radioactive source was obtained through the experimental measurement and energy calibration of the EPRDS and is shown in Fig. 9a, whereas that of the  $^{137}\text{Cs}$  radioactive source is shown in Fig. 9b. By searching and comparing the standard energy spectrum of  $^{152}\text{Eu}$  and  $^{137}\text{Cs}$ , it is evident that the standard full-energy peak position of the  $^{137}\text{Cs}$  standard energy spectrum was 661.6 keV and the measured value was

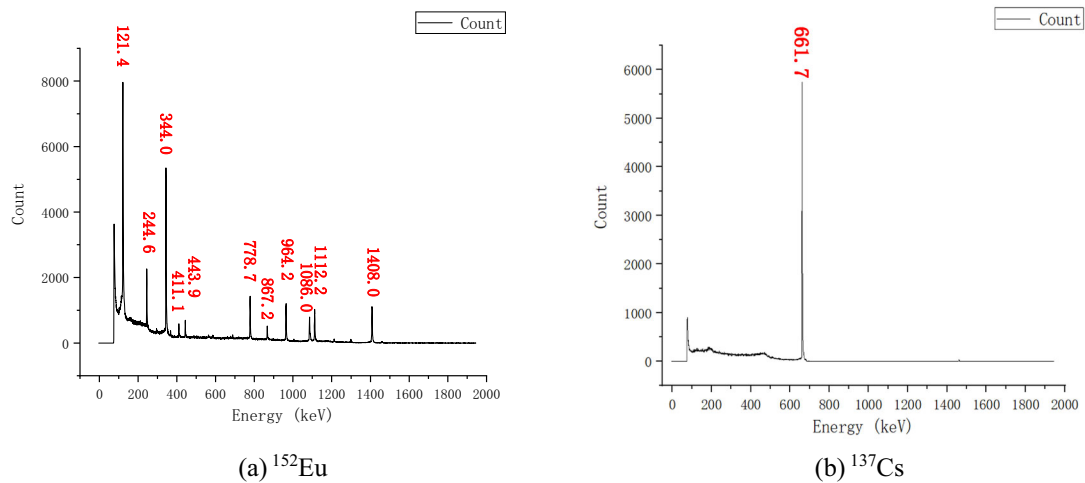


**Fig. 7** (Color online) Diagram and photograph of the experimental system in the laboratory





**Fig. 8** (Color online) The signal waveform outputted by the linear/shape amplifier



**Fig. 9** The experimental measurement and energy calibration spectra of the EPRDS system

661.7 keV. The measured energy spectrum of  $^{152}\text{Eu}$  also had a high degree of agreement with the standard energy spectrum. The measured energy spectrum peak position of this spectroscopy system was accurate, and the measurement error was less than  $\pm 0.5$  keV. The half-height width of the full-energy peak measured by  $^{137}\text{Cs}$  was 2.8 keV; thus, the energy resolution was 0.42% ( $2.8 \div 661.7 \text{ keV} = 0.42\%$ ). The measured half-height width of the 1408.0 keV peak for the  $^{152}\text{Eu}$  radioactive source was 3.8 keV; thus, the energy resolution was 0.27% ( $3.8 \div 1408.0 \text{ keV} = 0.27\%$ ). Globally, the energy resolution of the energy spectrum measurement system comprising a high-purity germanium detector was in the range of 0.15–0.3%. The energy resolution of the EPRDS system was close to the international advanced level [34, 35].

## 7 Summary

A high-performance EPRDS system was designed using the national core chip (ADC and FPGA) and Qt on the open-source Linux platform. High-speed data transmission from the main electronics card to the embedded controller was realized using the DMA mode communication via the PXIe bus. Following the circuit design, FPGA code programming, software interface design, and drive design for the EPRDS electronics system, performance tests were conducted on the main electronics card to verify the capacity of the electronics. The linear correlation coefficient ( $R$ ) of the pulse height and channel address was 0.999, and among the 4096 channel addresses, the FWHM of the main electronics card was no higher than three channel addresses (the channel address resolution of the main electronics card was 0.073%). The noise was approximately 2 mV, and the baseline offset was no higher

than  $\pm 3$  mV. Finally, a gamma experiment was conducted to test the combination performance of the EPRDS using  $^{152}\text{Eu}$  and  $^{137}\text{Cs}$  sources in the energetic particle diagnostic laboratory. The experimental results revealed that the energy spectrum measurement of the EPRDS for the  $^{152}\text{Eu}$  and  $^{137}\text{Cs}$  sources was accurate compared to the standard spectrum [36, 37]. The measurement error was less than  $\pm 0.5$  keV, and the highest energy resolution of 0.27% was achieved. The experimental results provide a useful guideline for the development of high-performance spectroscopy systems. Following the upgrading process, the EPRDS system will be employed to perform more rigorous plasma discharge operation experiments on the EAST device for comprehensive performance verification.

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