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Abstract A double-sided silicon strip detector (DSSD) with active area of $48 \text{ mm} \times 48 \text{ mm}$ and thickness of 300 µm has been developed. Each side of DSSD consists of 48 strips, each with width of 0.9 mm and inter-strip separation of 0.1 mm. Electrical properties and detection performances including full depletion bias voltage, reverse leakage current, rise time, energy resolution and cross talk have been studied. At a bias of 80 V, leakage current in each strip is less than 15 nA, and rise time for alpha particle at 5157 keV is approximately 15 ns on both sides. Good energy resolutions have been achieved with 0.65–0.80% for the junction strips and 0.85–1.00% for the ohmic strips. The cross talk is found to be negligible on

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both sides. The overall good performance of DSSD indicates its readiness for various nuclear physics experiments.

Keywords Double-sided silicon strip detector \cdot P-stop \cdot Detection performance · Cross talk

1 Introduction

Development of silicon detectors has been receiving benefits from the rapid technological advancement of the integrated circuit (IC) since the 1970s, when the earliest attempts to introduce planar process to the fabrication of silicon detectors took place [[1–4\]](#page-4-0). Techniques like oxide passivation, ion implantation and photolithography have successfully resolved the key issues encountered prior to the planar technology, granting feasibility to the fabrication of silicon strip detectors (SSDs). The advantages of an SSD include precise positioning, high energy resolution, long range of linear response, rapid response time and its feasibility to be fabricated into various designated shapes, facilitating its applicability in many research areas.

Since the beginning of the twenty-first century, many detector arrays composed of SSD-like CD [\[5](#page-4-0)], DRAGON [\[6](#page-4-0)], HiRA [\[7](#page-4-0)], LEDA [\[8](#page-4-0)], MUST [[9\]](#page-4-0) and MUST2 [[10\]](#page-4-0) have been constructed to meet individual experimental objectives. In China, several institutions such as the China Institute of Atomic Energy (CIAE), the Beijing Kelixing Photoelectric Technology Co., Ltd. and the Institute of Modern Physics, Chinese Academy of Science (IMP) have begun the development of double-sided silicon strip detectors (DSSDs). Prior to this project, CIAE had successfully developed the single-sided silicon strip detectors (SSSDs) that have been used in many nuclear experiments

[\[11–14](#page-5-0)] for about a decade. A more recent development by CIAE in the quadrant-silicon detectors (QSDs) [[15\]](#page-5-0) has also been shown successful in providing a new detector technology to various nuclear experiments [[16–18\]](#page-5-0). In this article, a cooperative production of DSSD by CIAE and the Beijing Kelixing Photoelectric Technology will be introduced, and performance test conducted at the University of Hong Kong will be presented.

2 Detection principle

The DSSD being developed in this work has an active area of 48 mm \times 48 mm and a thickness of 300 µm. The P⁺ doped junction side and the N^+ doped ohmic side comprise the basic framework of PN junction. At each side, all the 48 strips are evenly distributed and mutually parallel, each with a strip width of 0:9 mm and an inter-strip distance of 0:1 mm (Fig. 1). At an adequate supply of bias voltage around 60 V, the depletion region will expand and occupy the entire Si wafer.

When charged particle penetrates into the active region, electron–hole pairs will be produced. Due to the presence of electric field, electrons will be drifted toward the ohmic side, while the holes will be drifted toward the junction side. Electrical pulses at the electrodes are then being generated due to the induction caused by the motions of these charges. Positive signal pulses and negative signal pulses will be received by the junction side and the ohmic side, respectively, with energy loss information of the particle being encoded in the pulses. Each silicon strip could be treated as an individual detector during the signal collection.

3 Manufacturing procedure

The entire manufacturing procedure of the DSSD takes place inside a clean room. An N-type 4-inch silicon wafer of 300 μ m in thickness and 10 k Ω cm in resistivity is used for fabrication. After polishing and cleaning, the Si wafer undergoes the following manufacturing procedure:

- a. Oxide passivation The Si wafer is being exposed under high-temperature environment, with O_2 gas stream flowing past its surface so that an oxide layer $SiO₂$ of 600 nm thick is formed on top of it.
- b. Photolithography With the use of photolithographic equipment and proper etching techniques, some segments of the oxide layer are removed to form pattern of inter-strips on both sides.
- c. Ion implantation Junction side is doped with boron ions, forming a P^+ region; ohmic side is doped with

Fig. 1 (Color online) Photograph (top) and schematic view (bottom) of DSSD. Strips on the two sides are mutually perpendicular, equipping the detector with $48 \times 48 = 2304$ pixels

phosphorus ions, forming an N^+ region. At both sides, the thickness of doping is around 400 nm. This step creates the P^+ -Intrinsic-N⁺ (PIN) diode structure for the detector. In order to improve isolation on the ohmic side, P-stop technique has been employed to isolate the N^+ strips, i.e., boron ions have been doped into the N^+ inter-strip region and its surrounding to form P^+ isolation implants.

- d. Thermal annealing The doped Si wafer is being exposed under dry nitrogen gas at 600° C for 30 min.
- e. Al metalization and patterning A thin layer of Al is being sputtered onto both sides, and those which fall on top of the oxide layer are then being removed.
- f. Alloy and encapsulation Each individual strip is being separated and encapsulated before the detector chip is mounted onto the printed circuit board (PCB). The mounting employs ultrasonic soldering to establish permanent connection between the readout contacts on the PCB and the Al electrodes of DSSD which have been alloyed at 380° C.

All these procedures follow the fabrication parameters which have been optimized beforehand based on simulations or previous experience. One noteworthy issue is the tendency for N^+ strips to accumulate charges, which can easily introduce electrical breakdown across inter-strip region. Hence, P-stop technique has been implemented in this work to enhance strip isolation. A schematic figure that illustrates the important structural features of DSSD is given in Fig. 2.

4 Characterization

A schematic diagram for the readout electronics is shown in Fig. 3. Each junction strip is supplied with a negative bias from the Mesytec MHV-4 via a preamplifier of internal resistance $100 \text{ M}\Omega$, while each ohmic strip is connected to ground through an $100 \text{ M}\Omega$ resistor. Self-developed integrated charge-sensitive preamplifiers SPA02 (bandwidth of 275 MHz and signal-to-noise ratio of $5 \text{ nV}/\sqrt{\text{Hz}}$) have been used to perform current-to-voltage conversion and linear amplification on the signals collected from the strips on both sides. All preamplified signals are then be sent to the Mesytec MSCF-16 amplifier for further amplification and Gaussian shaping, with shaping times of 1 and 2 µs both being tested. After the MSCF-16 amplifier, energy signals from both sides are being sent to V785 ADC before being recorded by the computer, while time signals from the two sides are being processed differently. Two time signals, ECL timing and trigger output (NIM), have been extracted from MSCF-16 that connects the junction strips. The ECL timing is sent toward V775 TDC as start signal, while the trigger output is sent to trigger the ADC after consecutively undergoing an octal constant-fraction discriminator CF8000, and an octal gate and delay generator GG8010, in which an output is taken to serve as the common stop. For the ohmic side, only the ECL time signal is extracted and sent to the TDC as start signal. In this test, both energy signal and time signals are acquired by the RIBFDAQ system [\[19](#page-5-0)].

To investigate the performance of DSSD, alpha response is chosen to be studied by locating a triple alpha source that consists of 239 Pu, 241 Am and 244 Cm at approximately

Fig. 2 (Color online) Schematic figure for the structure of DSSD. (Not to scale)

Fig. 3 (Color online) Electronics block diagram of the detector test

3:0 cm away from the detector. Throughout the test, the entire piece of DSSD as well as the preamplifiers is all placed within a vacuum chamber with an air pressure of 10^{-3} Pa.

4.1 Voltage amplitude, rise time and leakage current

Voltage amplitude and rise time of preamplified signals have been measured as functions of bias voltage using an oscilloscope. When increasing bias voltage from 0 to 80 V, both signal amplitude and rise time turn saturated after 60 V (Fig. 4). At full depletion, body capacitance of each strip to the opposite side is around 50 pF. In practice, a bias higher than the saturation voltage could be taken, provided

Fig. 4 (Color online) Rise times and amplitudes of signals from the preamplifiers as functions of bias voltage when alpha particles coming from the junction side

that the bias does not exceed breakdown voltage. Throughout the test, a bias of 80 V has been adopted and the total leakage currents for all strips were found to be less than 720 nA, that is, each strip has less than 15 nA on average (Fig. 5).

4.2 Energy resolution of a single strip

A triple alpha source containing 239Pu, 241Am and 244Cm has been used. Their primary peak energies are given by 5157, 5486 and 5805 keV, respectively. Energy calibration has been performed for each strip individually prior to analysis. Using linear calibration, $E(x) = mx + c$, where x is the channel number, we find that m fluctuates less than 5% in all strips, while c shifts less than 1% of the full energy range (10,000 keV). Energy spectra collected by the 24th junction strip and the 24th ohmic strip are given in Fig. 6 for illustration. Limited by the energy resolution of detector, a low-energy tail is formed from the superposition of primary peak with non-primary peaks—take ²³⁹Pu for example, the major alpha decay paths include 5157 keV (71%), 5144 keV (17%) and 5106 keV (12%). At a bias of 80 V, the energy resolutions of all strips are found to fluctuate within 0.65–0.80% for the junction strips and 0.85–1.00% for the ohmic strips, while the electronic noise is found to contribute around 0.20% to the resolution [\[20](#page-5-0)].

4.3 Absence of cross talk between adjacent strips

Geometry of the strips inevitably introduces unwanted coupled capacitance. When an incoming charged particle hits a particular strip, charges are being accumulated in it, causing induced charges to arise in its adjacent strips due to the presence of inter-strip capacitance [[9,](#page-4-0) [21\]](#page-5-0). Being referred as cross talk in the literature [\[22](#page-5-0), [23\]](#page-5-0), this effect introduces pseudo-signal in the electronics at low-energy region, even though it has no apparent effect on the energy resolution of alpha signal. The significance of cross talk

Fig. 5 Total leakage current as a function of bias voltage

Fig. 6 (Color online) One-dimensional α spectra for the 24th junction strip and the 24th ohmic strip. Employing Gaussian fit at the 5157 keV peak, the junction strip yields an energy resolution of 37 keV (FWHM) or 0.71%; the ohmic strip yields 48 keV (FWHM) or 0.93%

depends on inter-strip capacitance C_i and body capacitance of the strip to the opposite side C_b . Significance of cross talk is associated with the ratio C_i/C_b , so it is desirable to have it as small as possible. Nevertheless, increasing C_b leads to weakening of signal amplitude, and hence, elimination of cross talk was approached by minimizing C_i . For our detector, $C_b \approx 50$ pF and C_i is small enough to reject cross talk between adjacent strips, as will be discussed in the next paragraph.

Ideally during the absence of cross talk, only the incidences that have successfully penetrated through the interstrip $SiO₂$ layer and injected into the active region will generate coincidence signals at adjacent strips. When plotted as a two-dimensional spectrum, these events are expected to have their energies shared by the adjacent strips, where the energy distribution is linearly related to the proximity of electron–hole pair creation point to the strip edge. This provides us a way to check the absence of cross talk by plotting the coincidence events between the adjacent strips. As illustrated in Fig. [7](#page-4-0), the expected energy distribution is observed for adjacent ohmic strips when particles enter from the junction side, indicating the absence of cross talk on the ohmic side; if cross talk had indeed occurred, clusters besides from those three belts of alpha signals would have shown up. The absence of cross talk on the junction side has also been confirmed by a similar manner. In our previous development, elimination of cross talk could only be achieved on the junction side but not on the ohmic side $[24]$ $[24]$. In this test, such issue has been overcome as P^+ isolation implants have successfully been implemented to the ohmic strips.

Fig. 7 (Color online) Two-dimensional spectrum that plots coincidence events between 24th and 25th ohmic strips with charged particles coming from the junction side

4.4 Pixel

The primary objective of developing DSSD is to acquire two-dimensional spatial position information of the charged particles with the pixels resulted from the intersection of strips on both sides. In this development, 48 strips have been equipped on each side, yielding a total of $48 \times 48 = 2304$ pixels on the detector. The two-dimensional energy spectra of pixels have been investigated as illustrated in Fig. 8, where the clusters of events correspond to the alpha peaks in Fig. [6](#page-3-0).

Fig. 8 (Color online) Two-dimensional spectrum of a pixel. The three clusters of events correspond to the energy peaks of the triple alpha source

5 Summary

In summary, a DSSD with 48 strips on each side has been developed and performance test has been conducted at a bias voltage of 80 V. Each strip carries a leakage current of around 15 nA. When alpha particles of 5157 keV enter from the junction side, rise time of signal after preamplifiers is about 15 ns on both sides. Energy resolutions are good, with the junction sides ranging within 0.65–0.80% and the ohmic sides ranging within 0.85–1.00%. Cross talk is found to be insignificant on both sides. The detectability of pixels has been demonstrated. Overall, the results indicate that the DSSD being developed is ready to be used in nuclear physics experiments. In the future, we plan to develop DSSD of different thicknesses as well as of different shapes to best meet the goals of various experiments. At the same time, we also wish to improve the success rate of production.

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