

A real-time online data acquisition system for Dragon-I linear induction accelerator

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Abstract An extensible high-speed accelerator data acquisition system (ADAS) for the Dragon-I linear induction accelerator has been developed. It comprises a VXI crate, a controller, four data acquisition plug-ins, and a host computer. A digital compensation algorithm is used to compensate for the distortion of high-speed signals arising from long-distance transmission. Compared with the traditional oscilloscope wall, ADAS has significant improvements in system integration, automation, and reliability. It achieves unified management of data acquisition and waveform monitoring and performs excellently with a 107-ps high-accuracy trigger and 32-channel signal monitoring. In this paper, we focus on the system architecture and hardware design of the ADAS, realization of the trigger, and digital compensation algorithm.

Keywords ADAS · LINAC · Beam position monitor · FPGA

1 Introduction

A linear induction accelerator (LIA) accelerates charged particles by utilizing the induced electromotive force produced by magnetic flux change. It has been widely applied

in areas of radiography, free electron lasers, high-power microwaves, and heavy ion fusion [1, 2]. The Dragon-I, a new LIA constructed at the Institute of Fluid Physics, Chinese Academy of Engineering Physics, is able to provide 20 MeV, 2.5 kA electron beams with a pulse width of 70 ns (FWHM) [3, 4].

The accelerator data acquisition system (ADAS), as a key component of Dragon-I, receives output signals from a detector subsystem to provide diagnosis for working conditions of the accelerator and relevant information about beam quality. The detectors include resistive wall, B-dot, and D-dot [5–7]. The detector unit is shown schematically in Fig. 1, where four or eight detectors, with equal distance and the beam centered, are located around the vacuum chamber [8, 9].

Under the circumstances of four detectors (A – D), the average voltage induced is determined by Eq. (1), where d is the electrode diameter; R is the load resistance; \bar{I}_c is the average current; a is the vacuum chamber radius; e is the elementary charge; σ_z is the bunch length; f is the repetition frequency; (x, y) is the beam position; and δ , θ , and $F(\delta, \theta)$ are defined in Eqs. (2), (3), and (4), respectively [10].

$$V_{A,B,C,D} \approx \frac{d^2 R \bar{I}_c F(\delta, \theta_{A,B,C,D})}{8a\sqrt{2\pi e \sigma_z^2} f}, \quad (1)$$

$$\delta = \sqrt{x^2 + y^2}, \quad (2)$$

$$\theta_{A,B,C,D} = n \frac{\pi}{4} - \tan^{-1} \left(\frac{y}{x} \right), \quad (3)$$

$$F(\delta, \theta) = \frac{a^2 - \delta^2}{a^2 + \delta^2 - 2a\delta \cos \theta}, \quad (4)$$

Excessive number of parameters would lead to complexity in calculation. Thus, we propose a simplified

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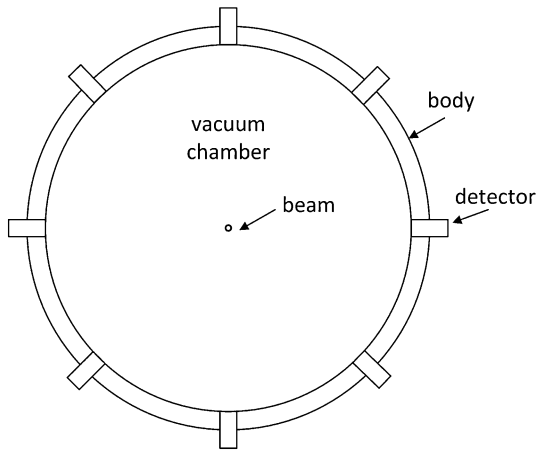


Fig. 1 Schematic showing the position of the equally spaced detectors

calculation model of normalized voltages. Equations (5) and (6) are the definitions of the normalized electrode signals.

$$U = [(V_B + V_C) - (V_A + V_D)] / (V_A + V_B + V_C + V_D), \tag{5}$$

$$V = [(V_A + V_B) - (V_C + V_D)] / (V_A + V_B + V_C + V_D), \tag{6}$$

With U and V , Eqs. (7) and (8) are expressions for the value of beam position (x, y).

$$x = \sum_{i=0}^k \sum_{j=0}^i A_{i-j,j} U^{i-j} V^j, \tag{7}$$

$$y = \sum_{i=0}^k \sum_{j=0}^i B_{i-j,j} U^{i-j} V^j, \tag{8}$$

Dragon-I produces high-speed single-pulse beam, and the ADAS shall be able to measure the high-speed signals. In practical operation, long-distance transmission usually causes analog signal distortion, which affects negatively on beam monitoring. In multi-channel operations, the electronic systems need a synchronous trigger with high accuracy for channel alignment. To solve these problems, the ADAS shall possess functions of multi-channel high-speed sampling, high-accuracy trigger, and customizable data processing. The key requirements of ADAS are as follows:

- High integration, 32 acquisition channels;
- 1 Gsps sampling rates, signal bandwidth ≥ 100 MHz;
- ENOB ≥ 7 bit @ 100 MHz;
- Digital compensation function;
- Low DC drift, low gain error, self-calibration;
- Multi-channel trigger, trigger accuracy, i.e., root mean square (RMS) < 500 ps;

- Automatic operation, automatic storage, and real-time data processing.

2 Realization of the ADAS

2.1 System structure

Figure 2 shows the architecture of ADAS [11]. It consists of four data acquisition plug-ins, one VXI crate with its controller, and one host computer. The plug-ins are responsible for data acquisition and processing. Each plug-in has eight acquisition channels that offer 8-bit 1-Gsps sampling. The VXI crate provides sufficient space and power supply for over 32 channels. The host computer is responsible for controlling, data receiving, and displaying for the entire system, and an IEEE 1394 cable is applied to transmit data between the VXI crate and the host computer.

2.2 Hardware design

The VXI-based instrument is primarily in charge of signal acquisition and processing [12]. Figure 3 shows architecture of the plug-in. It consists of eight analog front-ends (AFEs), four analog-to-digital converters (ADCs), two field-programmable gate arrays (FPGAs), the power supply unit, and a clock generator. The function of the VXI bus is to transmit data from the plug-in to the host.

The AFE focuses on receiving and conditioning the input signals [13]. Since the detectors are located in high-frequency electromagnetic interference (EMI) environment, a five-step LC anti-alias filter (AAF) is needed in

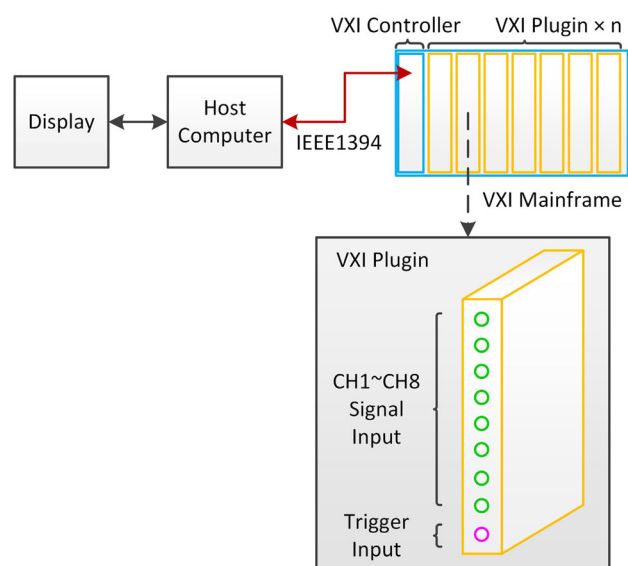


Fig. 2 Architecture of the ADAS

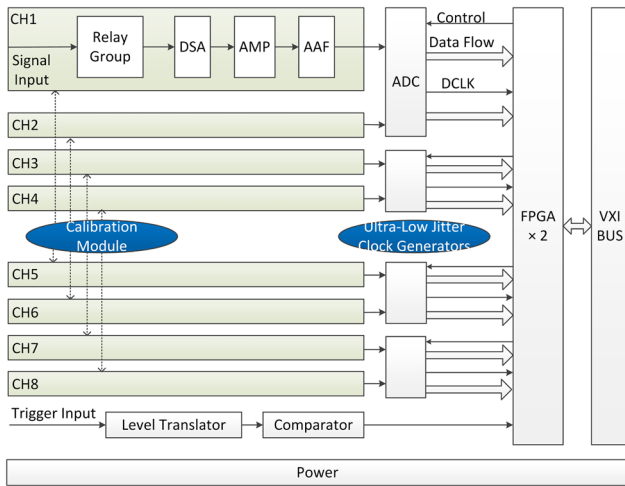


Fig. 3 Architecture of the plug-in

front of the ADC. It can block high-frequency noise and limit the passband at DC-125 MHz to increase signal-to-noise ratio (SNR).

Signals from Dragon-I detectors are of variable dynamic ranges, so the AFE gain should be adjustable to match dynamic range of the ADC input. Based on resistance adjustment, traditional method of gain control fails to meet the requirements of high integration and automation, and a fixed-gain amplifier cooperating with a digital step attenuator (DSA) is used for digital control. The gain parameters can be adjusted by regulating attenuation ratio of the DSA through VXI bus. Taking advantage of the high-performance DSA, the AFE gain ranges from -21.5 to $+10$ dB in 0.25-dB steps.

Calibration of the AFE is always necessary, since the AFE would introduce gain error and DC offset, hence the decrease of accuracy. Automatic AFE calibration based on FPGA and ADC is used, rather than traditional manual calibration. As the input bias and the ADC gain are adjustable, the AFE input is first connected to the ground so that the AFE input bias can be removed through adjusting the ADC input bias. Next, a stable reference voltage is used as the AFE input, and by regulating the ADC gain, the AFE gain can be modified. The self-calibration process carries on automatically right after the system is powered on. Meanwhile, manual recalibration is available if necessary.

As function core of the VXI plug-in, the two FPGAs are responsible for data receiving and processing, and control of slave devices as well [14, 15]. Figure 4 shows the architecture of inner logic of the FPGAs. The serializer/deserializer (SerDes) and data acquisition units receive data from the ADCs, while the data processing unit accomplishes signal analysis. Other units are responsible for system communication, coordinated control, and operation support.

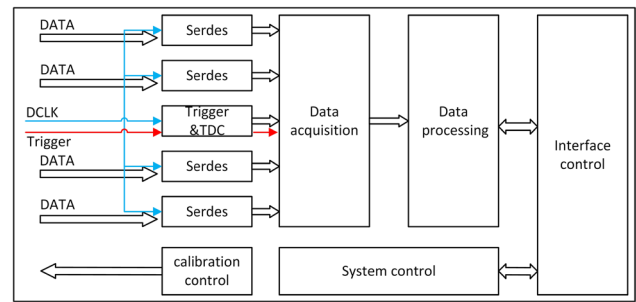


Fig. 4 Architecture of FPGA logic

2.3 Data acquisition and processing

To achieve high SNR sampling, a clock with extremely low aperture jitter (t_j) is needed. Equation (9) is the definition of SNR [16].

$$\text{SNR} = 20 \lg \left[\frac{1}{2\pi f t_j} \right], \quad (9)$$

As the jitter of sampling clock of this system must be less than 5 ps, the clock chip of LMK04821 is adopted to provide a 1-GHz synchronous sampling clock for ADCs with clock output jitter less than 300 fs.

ADC08D1000, an 8-bit 1-Gsps ADC, is used for analog signal sampling. It has a 1:2 demultiplexer that deserializes the 8-bit 1-GHz data stream into a 16-bit 500-MHz data stream, exporting the data stream via a low-voltage differential signaling (LVDS) bus. In the FPGA, the SerDes unit deserializes the 16-bit 500-MHz high-speed data stream into 64-bit 125-Mbps low-speed data stream, which is then written into ring storage, where a section of the latest data can be captured and stored when triggered. Next, the processing module performs real-time analysis to obtain characteristic parameters of the signals, including amplitude peak, pulse width, rising and falling time, and average voltage of a specified region. Finally, the plug-ins upload both the raw data and the analysis results to the host.

The ADAS is located considerably far away from the detector, connected by tens or hundreds of meters of coaxial cables, making signal distortion a common issue during high-speed pulse transmission. Therefore, digital compensation in FPGA achieves raw signal reconstruction.

In general, skin effects of cables under high frequency cause signal attenuation and the insulating medium causes high-frequency loss, as described in Eqs. (10) and (11), respectively, where f is the signal frequency, E and F are the coefficients determined by the cable material and structure, d is the diameter of the conductor, ϵ is the relative dielectric constant, D is the insulation diameter, and δ is the dielectric loss angle [17].

$$a_r = 2.6 \times 10^{-3} \sqrt{\varepsilon} \left(\frac{E}{d} + \frac{F}{D} \right) \frac{1}{\lg(D/d)} \sqrt{f}, \quad (10)$$

$$a_G = 9.1 \times 10^{-5} f \sqrt{\varepsilon} \tan \delta, \quad (11)$$

Considering the influence of DC resistance, the attenuation expression $a(f)$ can be simplified as Eq. (12).

$$a(f) = C + B\sqrt{f} + Af, \quad (12)$$

Equation (12) indicates the relationship between signal frequency and signal attenuation ratio through cables. With a digital sweeper, the frequency spectrum of the signals through each coaxial cable can be measured, and the coefficients of A , B , and C can be calculated using least square method (LSM). When capturing the valid signal, the data processing unit obtains its discrete frequency spectrum using fast Fourier transform (FFT) and then modifies the spectrum using Eq. (12). Finally, the unit reconstructs raw signal through the inverse fast Fourier transform.

2.4 Realization of the trigger unit

The trigger unit determines the initial time of signal acquisition, playing a key role in data alignment. As the external trigger signal arrives randomly, a 16-ns jitter can occur between any two channels since the inner clock of the FPGA is up to 125 MHz. To reduce jitter between channels, high-accuracy trigger position should be determined.

For this purpose, two time-to-digital converters (TDCs) [18–21] are used to obtain time-measuring capability using the FPGA’s logic resources. As excessively short measuring time leads to low accuracy, the TDC measures the time interval between rising edges of the trigger and the next third rising edges of data clock (DCLK) to locate trigger position. However, the TDC will miss recording the rising edges if the time interval between the rising edges of the trigger and the nearest DCLK is less than 110 ps, leading to inaccurate calculation. Therefore, once receiving a trigger, the FPGA shall produce a 1250-ps delayed signal called *Trigger_d* through the IO delay primitive. The correct measured time is then calculated by analyzing the results of the measurements, t and t_d , as illustrated in Fig. 5.

There are three cases worth considering, each of which is described below.

1. If $t - t_d$ is approximately 1250 ps, neither of the TDCs miss recording a rising edge; t is the measured time T .
2. If $t - t_d$ is approximately -2750 ps, TDC_A does not miss recording a rising edge; t is the measured time T .
3. If $t - t_d$ is approximately 5250 ps, TDC_B does not miss recording a rising edge; $t_d + 1250$ ps is the measured time T .

Suppose the ADC sampling rate is 1 Gsps, the ADC’s output data are highly synchronous with the DCLK. Thus,

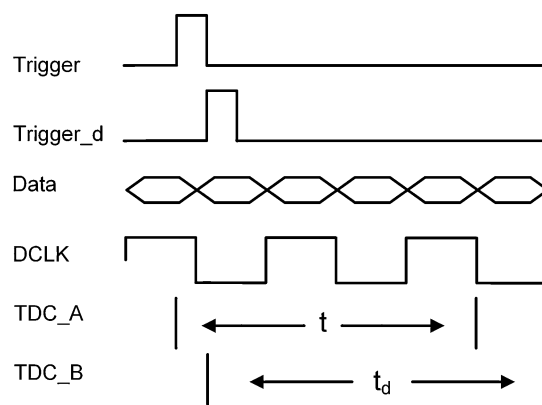


Fig. 5 Diagram illustrating triggered time measurements t and t_d

suppose that the pre-trigger number is N , and the calculated trigger position is $(N + 12 - T)$ ns. When a plug-in receives a trigger signal, it simultaneously broadcasts the signal to the rest of the plug-ins via the VXI backplane with an emitter-coupled logic (ECL) signal. Since the broadcast signal and clock synchronization pulse use the same transmission path, the time delay caused by different transmission distances cancels each other out. Through this method, the trigger position in the dataflow of every plug-in is definite, thus realizing high-accuracy trigger across plug-ins.

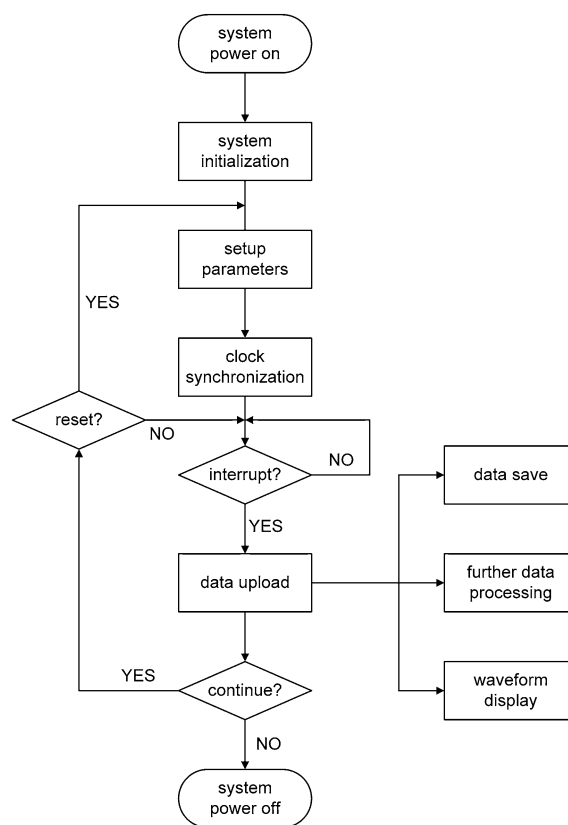


Fig. 6 Software workflow of our system

2.5 Software design

The software is in charge of system initialization, data receiving, and waveform displaying. Figure 6 is its workflow. In system initialization, the software sends operation parameters according to the detector’s type and working conditions. It also specifies a plug-in that is responsible for external trigger signal receiving. Next, the software commands the specific plug-in to send a clock synchronization pulse via the ECL line to synchronize other plug-ins. On receiving an interrupt, the system reads data from the plug-in and stores them on the computer’s hard drive. The host displays the signal waveforms on the monitor. In addition, the software provides an API for other programs to obtain data for further processing.

3 Test results

3.1 System performance test

For bandwidth test, we used a Fluke 9500B oscilloscope calibration workstation to generate fixed-amplitude sine

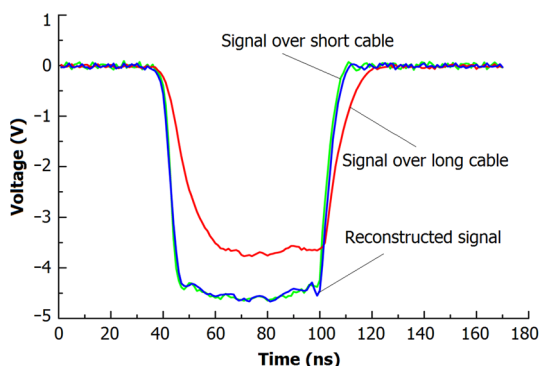
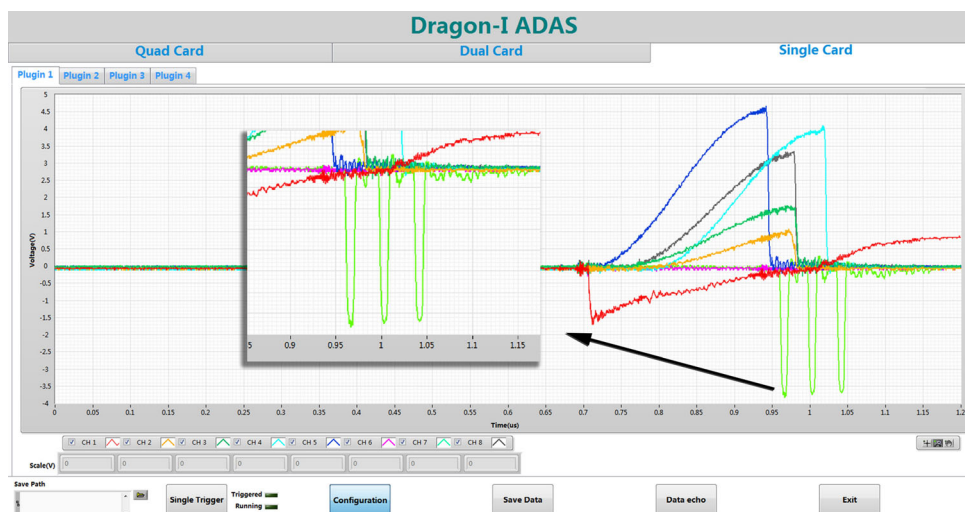


Fig. 7 Results of the waveform reconstruction test

Fig. 8 The ADAS-detected signals in the field test on Dragon-I



waves with variable frequencies as input signal. Results showed the bandwidth of the 32 channels ranging from 117 to 132 MHz.

For gain error test, we used an AFG3102C arbitrary function generator to generate linear sweep signal V_s (-4.75 to $+4.75$ V, 100 kHz). Then, the plug-in measured the voltage and calculated the gain error by linear fit of the measured data. The results indicated that the maximum gain error of each channel was less than 0.75%.

For ENOB performance test, we generated three sine waves of different frequencies using the Fluke 9500B as analog inputs (9.971 MHz with a 20-MHz low-pass filter, 59.971 MHz with a 100-MHz low-pass filter, and 99.971 MHz with a 200-MHz low-pass filter separately; 9.5 V in amplitude). The ADAS sampled the analog signals and calculated the ENOB. Test results showed that ENOB was always greater than 7.05 bits under the three conditions.

Finally, to test accuracy of the trigger, we used a pulse signal synchronized with the DCLK as trigger input, with repetitive measurement over 1000 times. Test results showed that the RMS accuracy of the trigger was 107 ps.

3.2 Field test

We operated the ADAS on the Dragon-I monitor system. Figure 7 shows the reconstruction effect report. The power splitter divided the detector output into two signals: the green one, which was sent to the ADAS through a short cable; and the red one, which was transmitted through an 85-m cable, with its reconstructed waveform being shown in blue. Analysis results showed great consistency between the reconstructed signal and the original one, with flat-topped average amplitude error of $<1.6\%$ and pulse width error of <2 ns.

Figure 8 is a screenshot of the ADAS software during the field test, reflecting the $V-t$ transients of eight types of

detected signals with a time base of 50 ns. Among all of the sampled signals, the fastest signal rising edge was 7 ns (see the enlarged section), suggesting that the system is competent in precise signal acquisition with a signal rising edge less than 10 ns.

4 Conclusion

We have developed the extensible high-speed ADAS. Owing to the calibration of the AFE and TDC-based trigger modules, the ENOB of the plug-in is greater than 7.05 bits and the RMS of the trigger accuracy is better than 107 ps. The data acquisition, control, and trigger algorithms are realized in the FPGAs, by which real-time data acquisition is guaranteed. During long-term operation of the Dragon-I accelerator, performance of the ADAS indicates that it has achieved the anticipated goals of high integration, high automation, and high reliability in data acquisition. The ADAS has potential applications on other large physical experiment facilities, without changing the circuit structure.

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