



Comparative analysis of PWM techniques for 15-level cross-connected H bridge inverter

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Abstract

The total harmonic distortion of the voltage plays an important role in selecting filter components. Multilevel inverters are one of the solutions for reducing total harmonic distortion and filter components. This paper discusses about third harmonic PWM controlled three-phase 15-level cross-H bridge multilevel inverter fed induction motor. The total harmonic distortion and losses of switches are calculated for third harmonic PWM, and the same are compared with a single pulse PWM controlled 3-Ø 15-level cross-H bridge multilevel inverter fed induction motor. The simulation of the third harmonic PWM and single pulse PWM fed 3-Ø 15-level cross-H bridge multilevel inverter fed induction motor is performed in MATLAB/SIMULINK environment.

Keywords Multilevel inverter · THD · Switch loss · PWM

List of symbols

L_V	Number of levels of output voltage
S_N	Number of power switches
V_{DCN}	Number of DC voltage sources
N_S	Number of switches conducting
V_{CE}	Voltage across IGBT
V_f	Voltage across diode
F	Fundamental frequency
E_{S_on}	Turn-on energy loss
E_{S_off}	Turn-off energy loss
$P_{cond.IGBT}$	Conduction losses of IGBT
$P_{cond.diode}$	Conduction losses of diode
P_{cond}	Loss due to conduction
$P_{sw\ IGBT}$	Loss due to switching

THI	Third harmonic injection
NPC	Neutral point clamped
mW	Milli Watt

Abbreviations

THD	Total harmonic distortion
MLI	Multilevel inverter
PWM	Pulse width modulation

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Introduction

The need for power is increasing day-by-day and fossil fuels are reducing, and environmental impact is more due to fossil fuels, so the research is focused on renewable energy sources. The major drawback of renewable energy is power generation that is not done at constant voltage and frequency so power electronic converters are required to convert to the required voltage and frequency. But with power electronic converters, harmonics are introduced. To minimize the harmonics multilevel inverters are one of the options to minimize the harmonics in converting power from DC to AC at the required voltage and frequency.

Multilevel inverters [MLIs] play an important role in converting the power from DC to AC. MLIs share the inverter operating voltage among the switches so low rating switches can be used to convert high power/voltage, which reduces the cost and size of the inverter. As the level of output voltage increases, the total harmonic distortion [THD] will reduce at low frequencies, which tends to reduce the cost and size of filters [1, 2].

The classical topologies of MLIs are neutral point clamped [3], flying capacitor [4], and Cascaded H-Bridge multilevel inverters [5]. The major issue with these conventional topologies is, as the number of levels in the output increases the

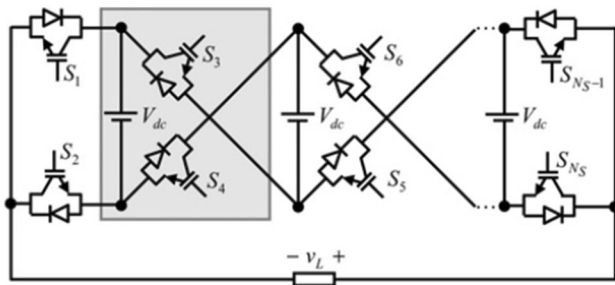


Fig. 1 Single-phase 15-level cross-H bridge MLI topology

number of switches also increased, this leads to the complexity in implementation of hardware circuits and switching patterns increases [6–10]. Based on these topologies, many topologies are developed, but in these topologies, some of the switches must withstand the total operating voltage of the inverter [11–14] (Fig. 1).

Cross-H bridge

The connection diagram for cross-H bridge inverter is shown in Fig. 2 having separate DC voltage sources, and switches are connected in a cross manner. This structure can be applied to any number of phases and any number of voltage levels by switching the proper switches required level of output voltage is obtained [15]. The stress on the switches S_1, S_2, S_{n-1} and S_n is V_{DC} , and it is $2V_{dc}$ for remaining switches and the total stress on the switches is equal to $2 * (V_L - 1) * V_{dc}$, where V_L is the level of output voltage.

Advantages of cross-H bridge:

- The number of power electronic switches required is less, and the number of switches conduct is less, so the losses and control circuit complexity are reduced.
- The total standing voltage is equal to CHB MLI.

Disadvantages of cross-H bridge:

- Structure is not modular
- Some switches have voltage rating more than Vdc (i.e., $2*Vdc$).

Mathematical analysis

Following relations are obtained from the proposed model

$$S_N = L_V + 1 \tag{1}$$

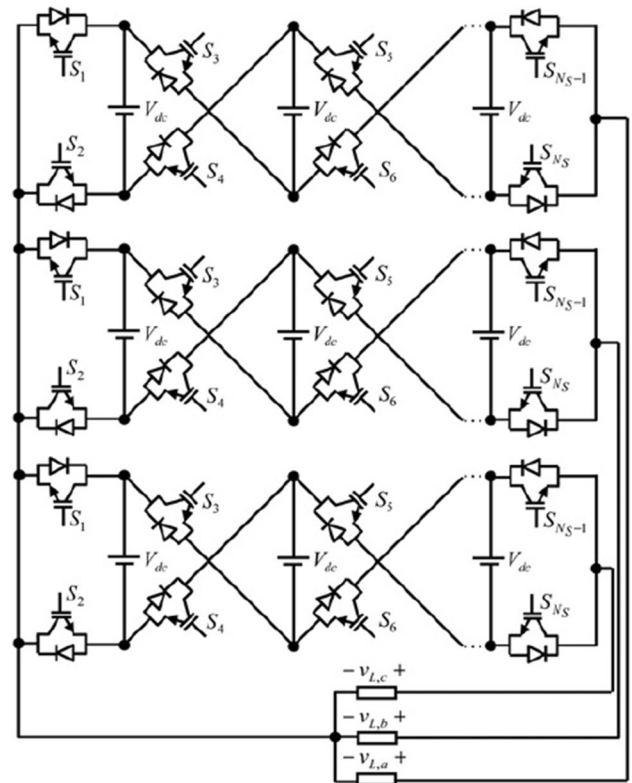


Fig. 2 Three-phase 15-level cross-H bridge MLI topology

$$L_V = 2 * V_{DCN} + 1 \tag{2}$$

$$S_N = 2(V_{DCN} + 1) \tag{3}$$

$$N_S = \frac{L_V + 1}{2} \tag{4}$$

These equations are used to calculate the number of switches required and the total number of output voltage levels that can be generated.

Table 1 Switch losses (total) versus O/P voltage levels

MLI type	Total switch losses (mW) for 15-level o/p voltage	
	1-phase	3-phase
Third harmonic PWM controlled cross-H-bridge	73.96	221.88
Single pulse PWM controlled cross-H-bridge	104.71	314.1

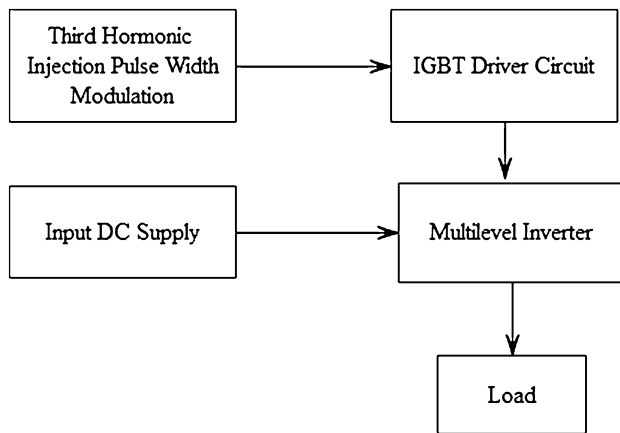


Fig. 3 Block diagram of 15-level cross-H bridge multilevel inverter fed a load using third harmonic PWM technique

Switch losses

Power electronic switches contain two major losses: one is due to conduction (P_{cond}), and another one is due to switching ($P_{sw\ IGBT}$) [16–19]; the IGBT switches are considered in this paper.

The average conduction losses of IGBT ($P_{cond.IGBT}$) and diode ($P_{cond.diode}$) are given as follows:

$$P_{cond.IGBT} = \int_{t_{con}} P(t)dt = \frac{1}{T} \int_0^T V_{ce}(t) * i_{ce}(t)dt \tag{5}$$

$$P_{cond.diode} = \frac{1}{T} \int_0^T V_f(t) * i_d(t)dt \tag{6}$$

The total conduction losses of the proposed inverter for one cycle

$$P_{cond} = (P_{cond.IGBT} + P_{cond.diode}) * N_s \tag{7}$$

The switching losses are present during ON and OFF the power electronic switches. The switching losses of IGBT ($P_{sw\ IGBT}$) are given as follows:

$$P_{swIGBT} = (E_{swon} + E_{swoff}) * f \tag{8}$$

$$E_{s_on} = \int_{ton} V_{ce}(t) * i_{ce}(t)dt \tag{9}$$

Fig. 4 a Generation of third harmonic waveform. **b** Third harmonic pulse width modulation for 15-level cross-H bridge inverter

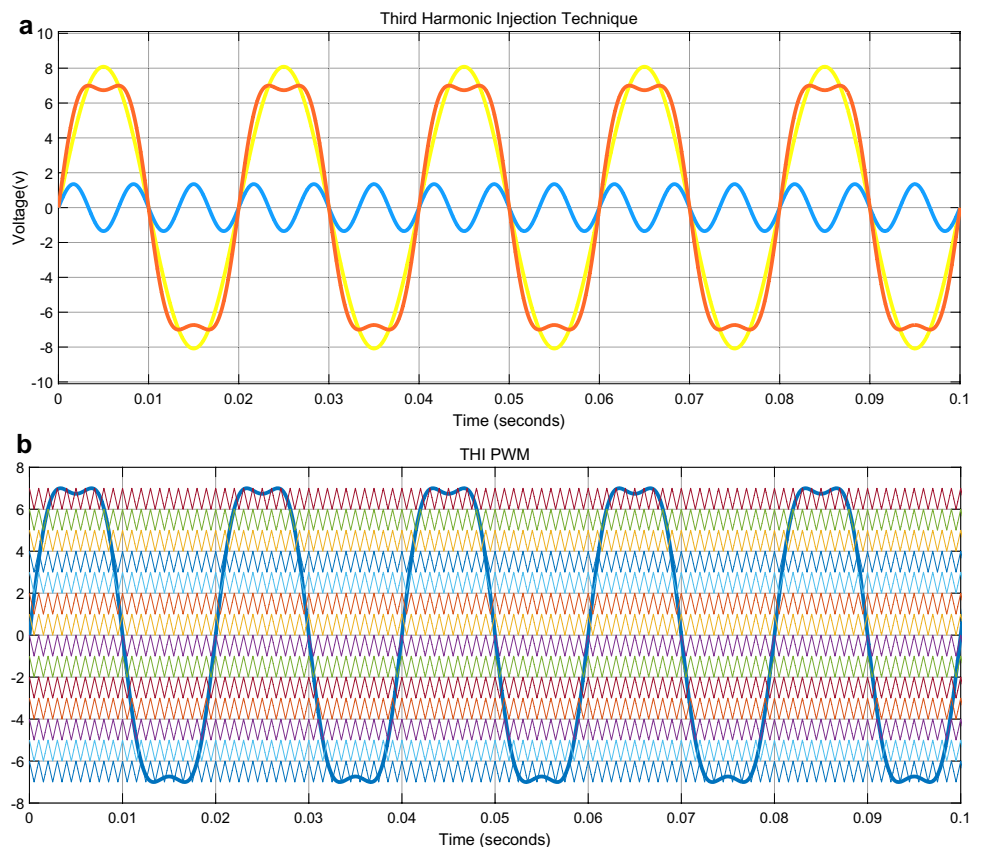


Table 2 Switching pattern of cross-H-bridge 15-level MLI

S. no.	O/P voltage	Switches ON	S. no.	O/P voltage	Switches ON
1	7 V _{DC}	S ₂ S ₃ S ₆ S ₇ S ₁₀ S ₁₁ S ₁₄ S ₁₅	9	-7 V _{DC}	S ₁ S ₄ S ₅ S ₈ S ₉ S ₁₂ S ₁₃ S ₁₆
2	6 V _{DC}	S ₁ S ₃ S ₆ S ₇ S ₁₀ S ₁₁ S ₁₄ S ₁₅ S ₂ S ₃ S ₆ S ₇ S ₁₀ S ₁₁ S ₁₄ S ₁₆	10	-6 V _{DC}	S ₁ S ₄ S ₅ S ₈ S ₉ S ₁₂ S ₁₃ S ₁₅ S ₂ S ₄ S ₅ S ₈ S ₉ S ₁₂ S ₁₃ S ₁₆
3	5 V _{DC}	S ₁ S ₃ S ₆ S ₇ S ₁₀ S ₁₁ S ₁₄ S ₁₆ S ₂ S ₃ S ₆ S ₇ S ₁₀ S ₁₁ S ₁₃ S ₁₅ S ₂ S ₄ S ₆ S ₇ S ₁₀ S ₁₁ S ₁₄ S ₁₅	11	-5 V _{DC}	S ₁ S ₄ S ₅ S ₈ S ₉ S ₁₂ S ₁₄ S ₁₆ S ₁ S ₃ S ₅ S ₈ S ₉ S ₁₂ S ₁₃ S ₁₆ S ₂ S ₄ S ₅ S ₈ S ₉ S ₁₂ S ₁₃ S ₁₅
4	4 V _{DC}	S ₁ S ₃ S ₆ S ₇ S ₁₀ S ₁₁ S ₁₃ S ₁₅ S ₁ S ₃ S ₆ S ₇ S ₁₀ S ₁₁ S ₁₄ S ₁₅ S ₂ S ₃ S ₆ S ₇ S ₁₀ S ₁₂ S ₁₄ S ₁₆ S ₂ S ₄ S ₆ S ₇ S ₁₀ S ₁₁ S ₁₄ S ₁₆	12	-4 V _{DC}	S ₁ S ₄ S ₅ S ₈ S ₉ S ₁₁ S ₁₃ S ₁₅ S ₁ S ₃ S ₅ S ₈ S ₉ S ₁₂ S ₁₃ S ₁₅ S ₂ S ₄ S ₅ S ₈ S ₉ S ₁₂ S ₁₄ S ₁₆ S ₂ S ₄ S ₆ S ₈ S ₉ S ₁₂ S ₁₃ S ₁₆
5	3 V _{DC}	S ₁ S ₃ S ₆ S ₇ S ₁₀ S ₁₂ S ₁₄ S ₁₆ S ₁ S ₃ S ₅ S ₇ S ₁₀ S ₁₁ S ₁₄ S ₁₆ S ₂ S ₃ S ₆ S ₇ S ₉ S ₁₁ S ₁₃ S ₁₅ S ₂ S ₄ S ₆ S ₇ S ₁₀ S ₁₁ S ₁₃ S ₁₅ S ₂ S ₄ S ₆ S ₈ S ₁₀ S ₁₁ S ₁₄ S ₁₅	13	-3 V _{DC}	S ₁ S ₃ S ₅ S ₈ S ₁₀ S ₁₂ S ₁₄ S ₁₆ S ₁ S ₃ S ₅ S ₈ S ₉ S ₁₂ S ₁₄ S ₁₆ S ₁ S ₃ S ₅ S ₇ S ₉ S ₁₂ S ₁₃ S ₁₆ S ₂ S ₄ S ₅ S ₈ S ₉ S ₁₁ S ₁₃ S ₁₅ S ₂ S ₄ S ₆ S ₈ S ₉ S ₁₂ S ₁₃ S ₁₅
6	2 V _{DC}	S ₁ S ₃ S ₆ S ₇ S ₉ S ₁₁ S ₁₃ S ₁₅ S ₁ S ₃ S ₅ S ₇ S ₁₀ S ₁₁ S ₁₃ S ₁₅ S ₁ S ₃ S ₅ S ₇ S ₉ S ₁₁ S ₁₄ S ₁₅ S ₂ S ₃ S ₆ S ₈ S ₁₀ S ₁₂ S ₁₄ S ₁₆ S ₂ S ₄ S ₆ S ₇ S ₁₀ S ₁₂ S ₁₄ S ₁₆ S ₂ S ₄ S ₆ S ₈ S ₁₀ S ₁₁ S ₁₄ S ₁₆	14	-2 V _{DC}	S ₁ S ₄ S ₅ S ₇ S ₉ S ₁₁ S ₁₃ S ₁₅ S ₁ S ₃ S ₅ S ₈ S ₉ S ₁₁ S ₁₃ S ₁₅ S ₁ S ₃ S ₅ S ₇ S ₉ S ₁₂ S ₁₃ S ₁₅ S ₂ S ₄ S ₅ S ₈ S ₁₀ S ₁₂ S ₁₄ S ₁₆ S ₂ S ₄ S ₆ S ₈ S ₉ S ₁₂ S ₁₄ S ₁₆ S ₂ S ₄ S ₆ S ₈ S ₁₀ S ₁₂ S ₁₃ S ₁₆
7	V _{DC}	S ₁ S ₃ S ₆ S ₈ S ₁₀ S ₁₂ S ₁₄ S ₁₆ S ₁ S ₃ S ₅ S ₇ S ₁₀ S ₁₂ S ₁₄ S ₁₆ S ₁ S ₃ S ₅ S ₇ S ₉ S ₁₁ S ₁₄ S ₁₆ S ₂ S ₃ S ₅ S ₇ S ₉ S ₁₁ S ₁₃ S ₁₅ S ₂ S ₄ S ₆ S ₇ S ₉ S ₁₁ S ₁₃ S ₁₅ S ₂ S ₄ S ₆ S ₈ S ₁₀ S ₁₂ S ₁₃ S ₁₅ S ₂ S ₄ S ₆ S ₈ S ₁₀ S ₁₂ S ₁₄ S ₁₅	15	-V _{DC}	S ₁ S ₄ S ₆ S ₈ S ₁₀ S ₁₂ S ₁₄ S ₁₆ S ₁ S ₃ S ₅ S ₈ S ₁₀ S ₁₂ S ₁₄ S ₁₆ S ₁ S ₃ S ₅ S ₇ S ₉ S ₁₂ S ₁₄ S ₁₆ S ₁ S ₃ S ₅ S ₇ S ₉ S ₁₁ S ₁₃ S ₁₆ S ₂ S ₄ S ₅ S ₇ S ₉ S ₁₁ S ₁₃ S ₁₅ S ₂ S ₄ S ₆ S ₈ S ₉ S ₁₁ S ₁₃ S ₁₅ S ₂ S ₄ S ₆ S ₈ S ₁₀ S ₁₂ S ₁₃ S ₁₅
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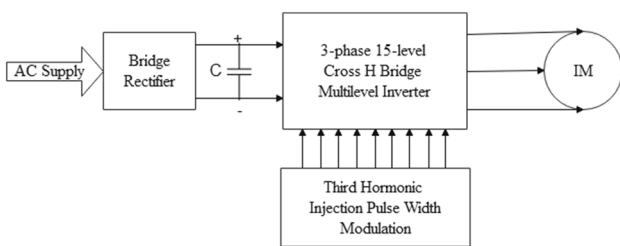


Fig. 5 Three-phase 15-level cross-H bridge MLI fed IM block diagram

$$E_{s_off} = \int_{toff} V_{ce}(t) * i_{ce}(t)dt \tag{10}$$

Table 1 represents the comparison of losses of converter for various switching techniques. The losses are in mW scale. Total switch loss in three-phase system has been reduced in third harmonic PWM control by 29.40% when the same converter is fed with single pulse PWM technique. Similarly, in single-phase system, the total losses are also reduced by 29.40%. When looking into switching loss third

Fig. 6 Single-phase 15-level cross-H-bridge MLI topology

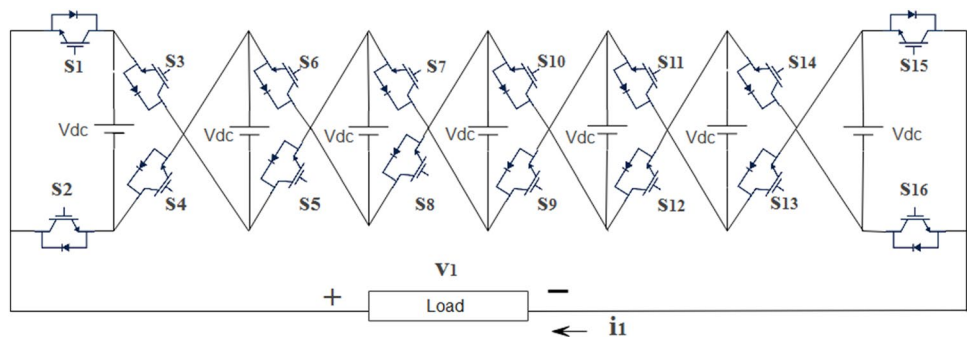


Fig. 7 Three-phase output voltages (THI PWM)

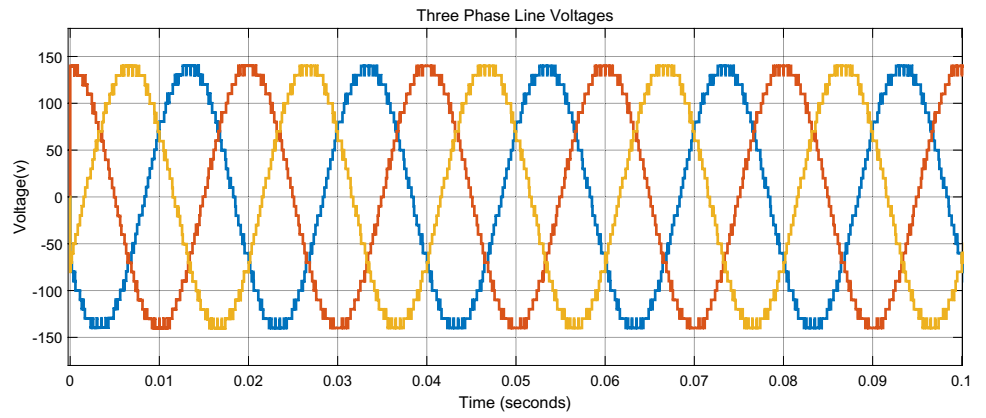


Fig. 8 Stator phase current of 3-Ø induction motor (THI PWM)

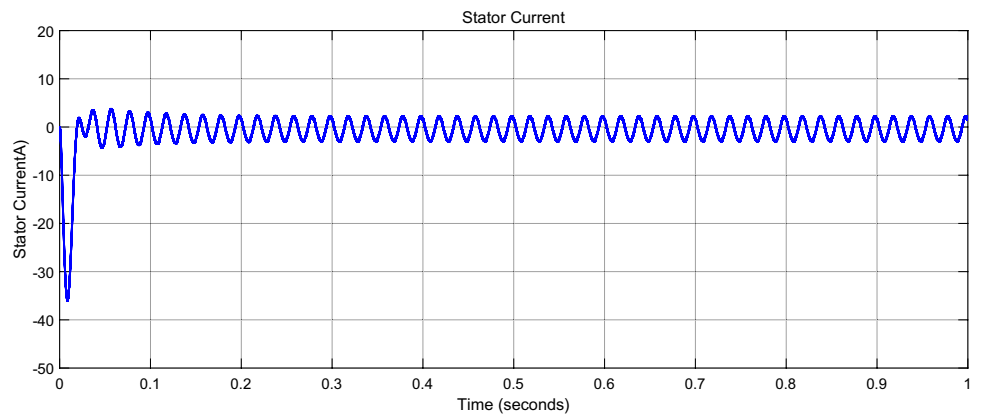


Fig. 9 Speed response of induction motor (THI PWM)

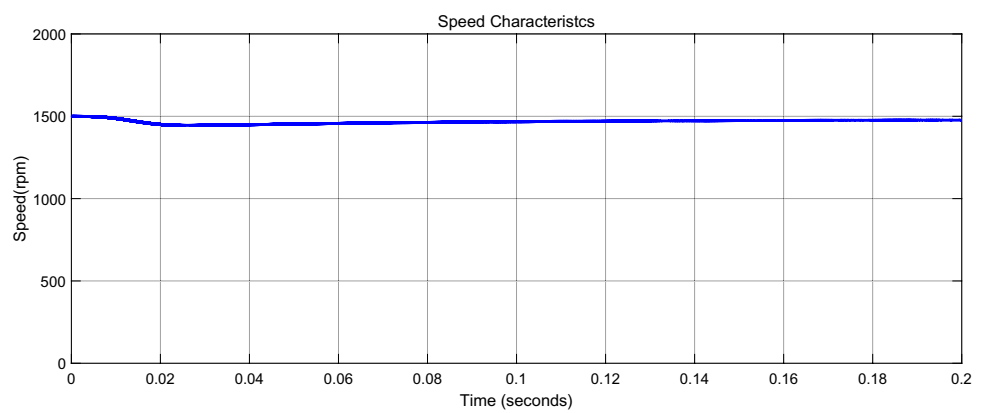
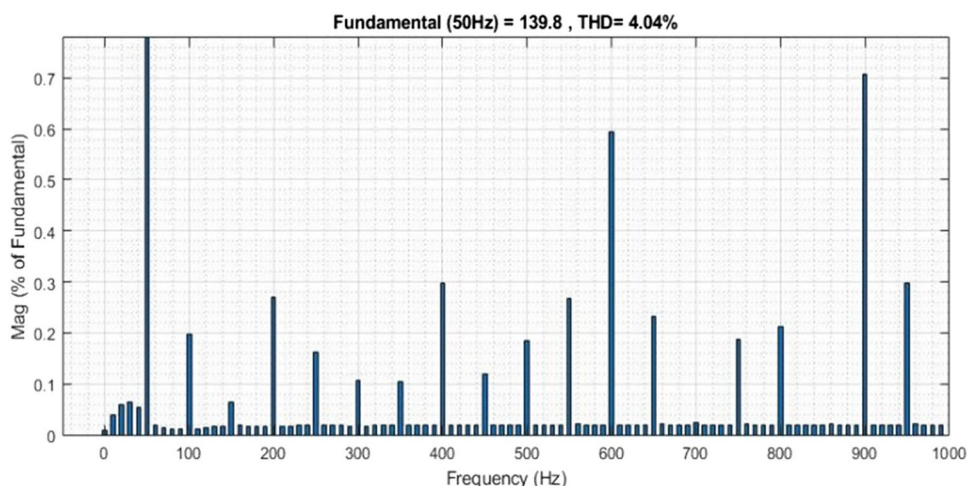


Fig. 10 THD of third harmonic PWM controlled 15-level cross-H-bridge MLI



harmonic PWM control is having less loss when compared with single pulse PWM.

Third harmonic PWM

For a three-phase load with a floating-point neutral point, the third harmonic voltage is absent from the phase voltages and line to line. Therefore, there is no distortion in the phase voltages. We might improve the sufficiency of the yield voltage waveform by adding a third consonant sign to a low-recurrence sinusoidal reference signal [20–24] (Figs. 3, 4; Table 2).

Results

The simulation of third harmonic PWM controlled 3- \emptyset 15-level cross-H bridge multilevel inverter is done. The block diagram of third harmonic PWM controlled 3- \emptyset 15-level cross-H bridge multilevel inverter and circuit representation of 15-level cross-H bridge is represented in Figs. 5 and 6, respectively. The switch IGBT (FGA15N120ANTD) is considered for simulation and for calculating the losses of switches. Voltage, current, and speed analysis are discussed for third harmonic PWM and single pulse PWM [25] controlled 3- \emptyset 15-level cross-H bridge multilevel inverter fed induction motor drive.

Third harmonic PWM controlled 3- \emptyset 15-level cross-H Bridge fed IM

Figure 7 represents three-phase simulated output voltages of third harmonic PWM controlled 15-level cross-H-bridge

multilevel inverter with the peak output voltage of 140v peak to peak. Similarly, the simulated phase current of 3- \emptyset IM is shown in Fig. 8. Figure 9 represents the speed response of the motor; the current and the speed are oscillated initially and settled to 1480 RPM at 0.19 s. Figure 10 shows the total harmonic distortion of sinusoidal PWM controlled 15-level cross-H-bridge MLI. The value of THD is recorded as 4.04%. Figure 10 shows the switching pulses of all sixteen switches (Fig. 11).

Single Pulse PWM controlled 3- \emptyset 15-level cross-H Bridge fed IM

Figure 12 indicates the 3- \emptyset output voltages with 140 V peak. Figures 13 and 14 represent the 3- \emptyset induction motor stator current of one of the phases and speed. From Figs. 13 and 14, it can be observed that the settling time of stator current and speed is 0.22 s. Figure 15 shows the total harmonic distortion, which is recorded as 6.64%. From above wave forms, THD with third harmonic PWM is reduced by 39% and settling time of current and speed is reduced by 13% when compared with single pulse PWM. Comparison of stator current, speed and torque characteristics are shown in Figs. 16, 17 and 18, respectively.

Conclusion

In this paper, simulation of third harmonic PWM controlled 3- \emptyset 15-level cross-H bridge and single pulse PWM controlled 3- \emptyset 15-level cross-H bridge is done. THD,

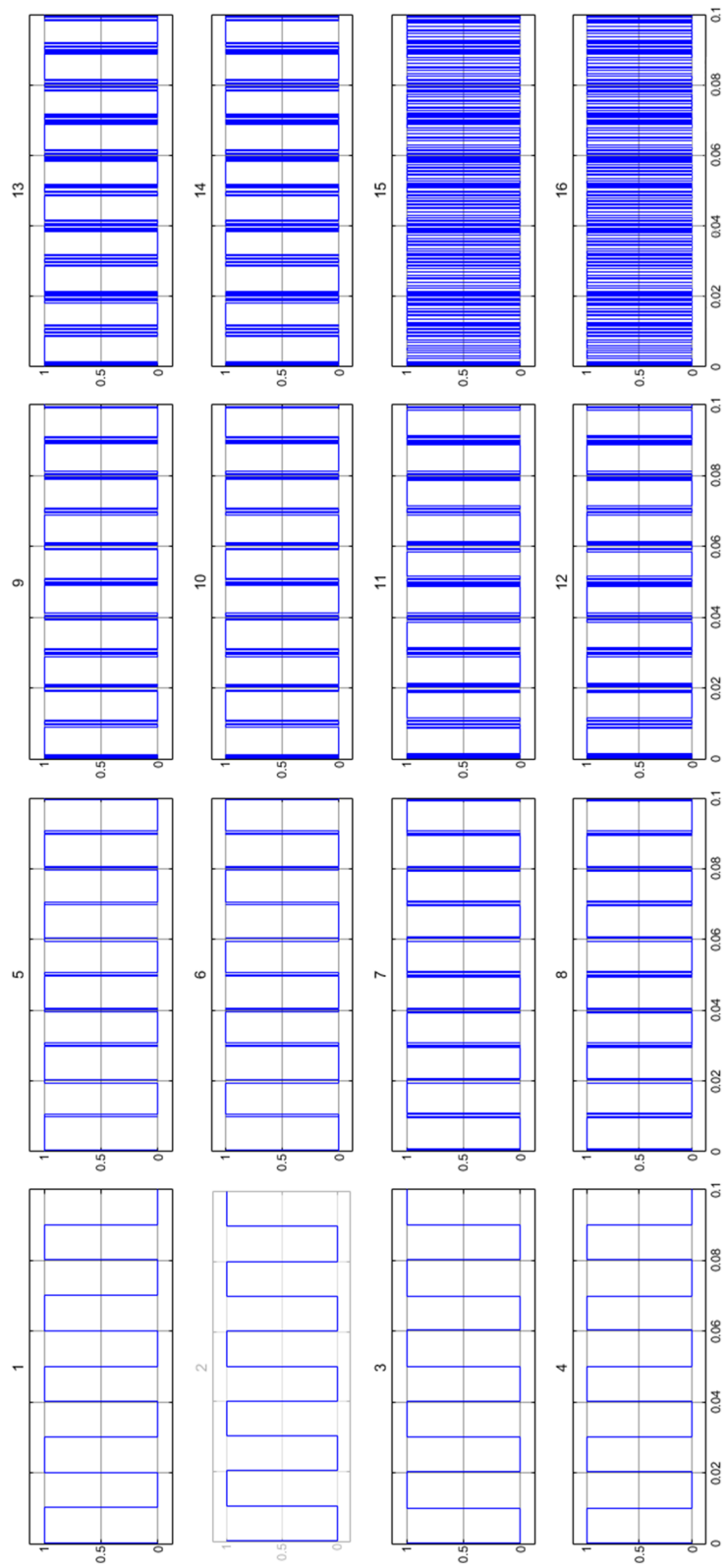


Fig. 11 Pulses given to 16 switches in THI-PWM

Fig. 12 Three-phase output voltages (single pulse PWM)

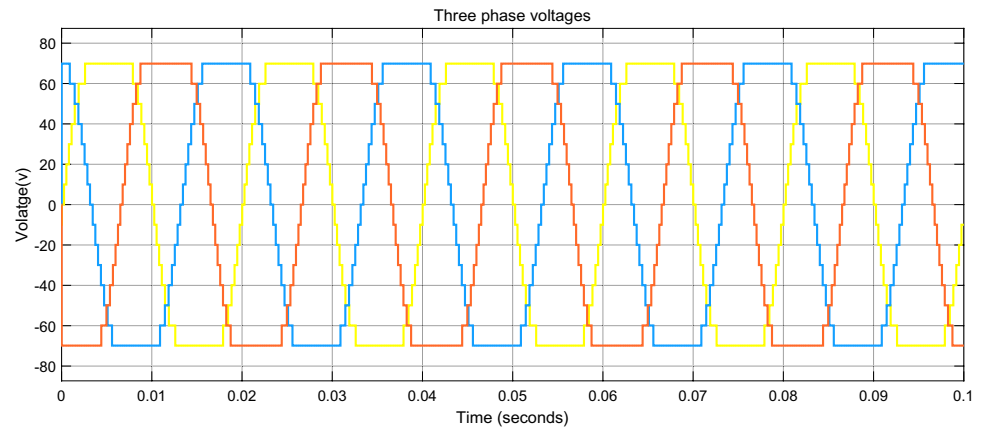


Fig. 13 Stator phase current of three-phase induction motor (single pulse PWM)

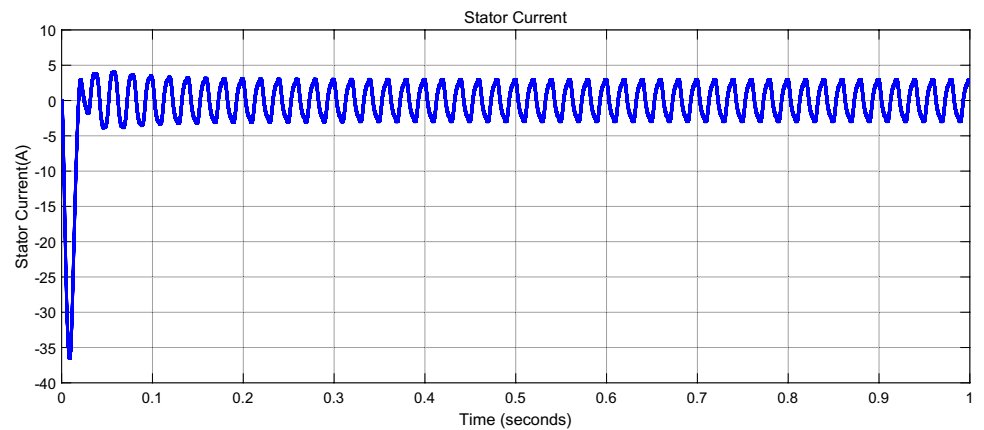
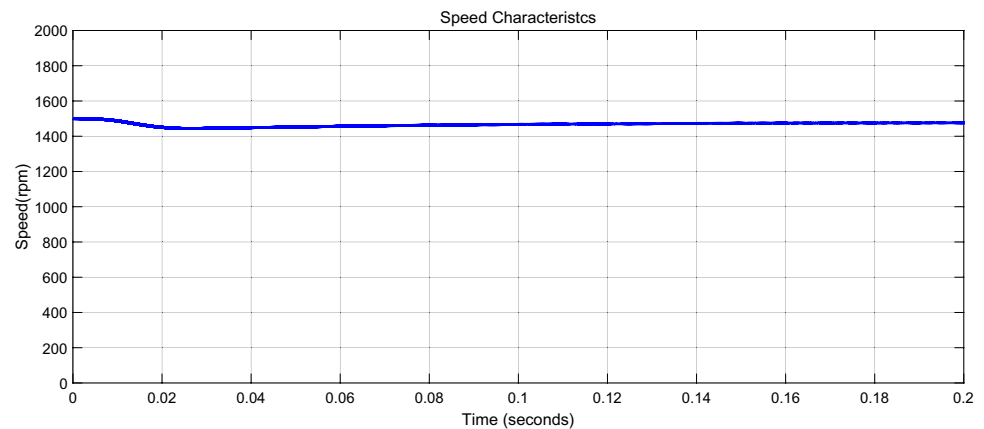


Fig. 14 Speed response of induction motor (single pulse PWM)



current, and speed are analyzed with both and PWM techniques. From results obtained, it is found that third harmonic PWM THD is reduced by 39% and settling time of speed and current waveforms is reduced by 13% and total

losses of switches are also reduced when compared with single pulse PWM. When compared both the PWM techniques, third harmonic PWM technique is more reliable than single pulse PWM technique.

Fig. 15 THD of single PWM controlled 15-level cross-H-bridge MLI

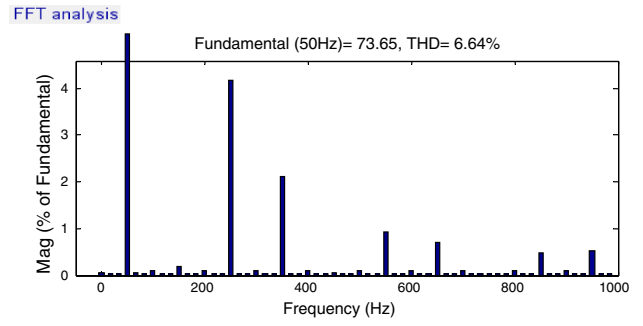


Fig. 16 Stator current comparison with THI and single pulse PWM

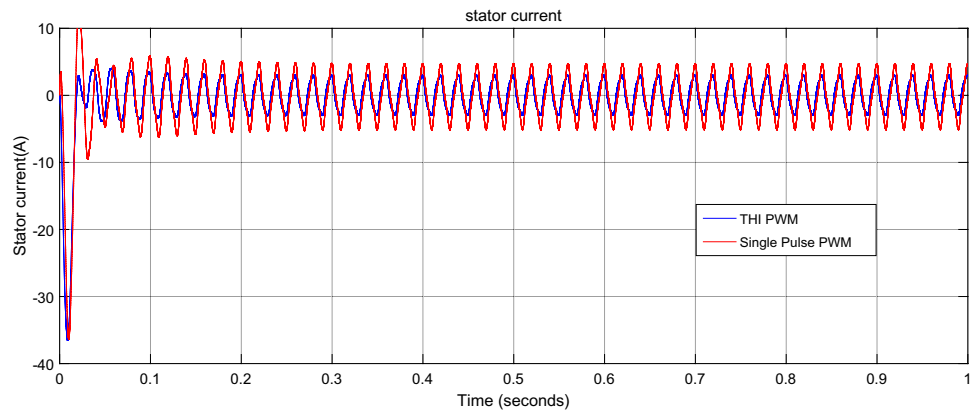


Fig. 17 Speed characteristics comparison with THI and single pulse PWM

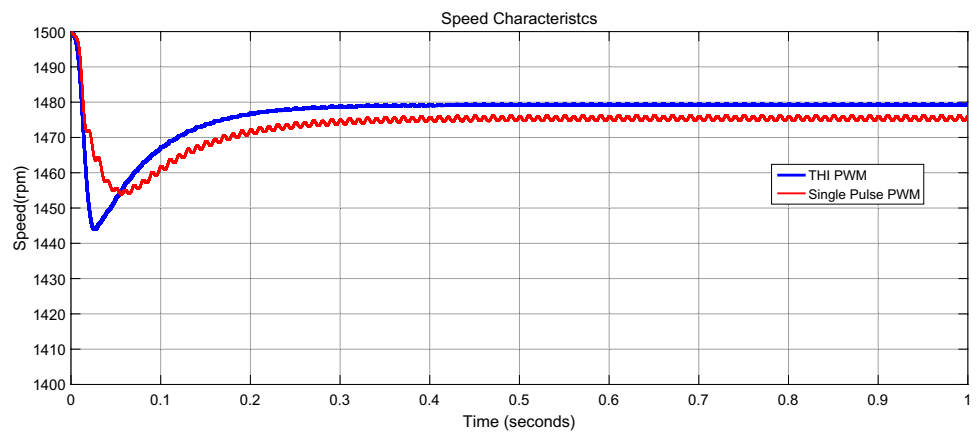
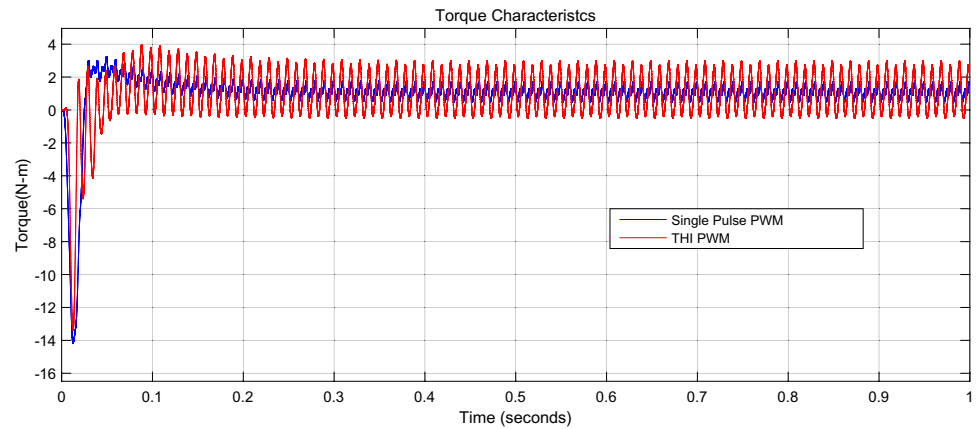


Fig. 18 Torque characteristics comparison with THI and single pulse PWM



Declarations

Conflict of interest The authors declare that they have no conflict of interest.

References

- Bana PR, Panda KP, Naayagi RT, Siano P, Panda G (2019) Recently developed reduced switch multilevel inverter for renewable energy integration and drives application: topologies, comprehensive analysis and comparative evaluation. *IEEE Access* 7:54888–54909
- Gupta KK, Ranjan A, Bhatnagar P, Sahu LK, Jain S (2016) Multilevel inverter topologies with reduced device count: a review. *IEEE Trans Power Electron* 31(1):135–151
- Rodriguez J, Bernet S, Steimer P, Lizama I (2010) A survey on neutral point clamped inverters. *IEEE Trans Ind Electron* 57(7):2219–2230
- Abhilash T, Annamalai K, Tirumala SV (2019) A seven-level VSI with a front-end cascaded three-level inverter and flying-capacitor-fed H-bridge. *IEEE Trans Ind Appl* 55(6):6073–6088
- Pamujula M, Ohja A, Kulkarni RD, Swarnkar P (2020) Cascaded ‘H’ bridge based multilevel inverter topologies: a review. In: 2020 International Conference for Emerging Technology (INCET), Bangalore, India
- Babaei E, Hosseinzadeh MA, Sarbanzadeh M, Cecati C (2016) A new basic unit for cascaded multilevel inverters with reduced number of power electronic devices. In: 2016 7th Power Electronics and Drive Systems Technologies Conference (PEDSTC), Tehran, Iran
- Babaei E, Laali S, Bayat Z (2015) A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches. *IEEE Trans Ind Electron* 62(2):922–929
- Srinivas Rao MJ, Srinivasa Varma P, Suresh Kumar T (2018) Novel switching design structure for three phase 21-level multilevel inverter fed BLDC drive application. *Int J Power Electron Drive Syst* 9(3), 1202–1213. ISSN: 2088-8694
- Ghat B, Shukla A, Mathew EC (2017) A new hybrid modular multilevel converter with increased output voltage levels. In: 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, pp 1634–1641
- Shuvo S, Hossain E, Islam T, Akib A, Padmanaban S, Khan MZR (2019) Design and hardware implementation considerations of modified multilevel cascaded H-bridge inverter for photovoltaic system. *IEEE Access* 7:16504–16524
- Chadli H, Jebrouni Z, Chadli S, Tahani A, Aziz A (2017) Design and implementation of a novel five-level inverter topology. In: 2017 International Conference on Wireless Technologies, Embedded and Intelligent Systems (WITS), Fez, Morocco, pp 1–6
- Chulan MA, Yatim AHM (2014) Design and implementation of a new H-bridge multilevel inverter for 7-level symmetric with less number of switches. In: 2014 IEEE International Conference on Power and Energy (PECon), Kuching, Malaysia, pp 348–353
- Neysabouri Y, Farhadi-Kangarlu M (2020) An improved fault tolerant technique based on zero-sequence voltage injection for symmetric cascaded H-bridge inverter. In: 2020 28th Iranian Conference on Electrical Engineering (ICEE), Tabriz, Iran
- Raj N, Anand A, Riyas A, Jagadanand G, George S (2016) A novel open-transistor fault detection method in symmetric cascaded H-bridge multilevel inverter. In: 2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Trivandrum, pp 1–6
- Kangarlu MF, Babaei E (2013) Cross-switched multilevel inverter: an innovative topology. *IET Power Electron* 6(4):642–651
- Shirahama H, Muto T (2018) A novel power loss calculation method for power converters by transforming switching-loss into impulse-waveforms. In: 2018 21st International Conference on Electrical Machines and Systems (ICEMS), Jeju, Korea (South)
- Wei K, Zhang C, Gong X, Kang T (2017) The IGBT losses analysis and calculation of inverter for two-seat electric aircraft application. *Energy Procedia* 105:2623–2628
- Alamri B, Darwish M (2015) Power loss investigation in HVDC for cascaded H-bridge multilevel inverters (CHB-MLI). In: 2015 IEEE Eindhoven PowerTech, PowerTech 2015, vol 2, no 6, pp 230–238
- Tomar PS, Sandeep N, Verma AK, Srivastava M (2020) Analysis, design, and implementation of an improved gate driver for high switching frequency EV application. *IET Power Electron* 13(9):1797–1806. <https://doi.org/10.1049/iet-pel.2019.1275>
- Albatran S, Allabadi AS, Khalailah ARA, Fu Y (2021) Improving the performance of a two-level voltage source inverter in the over-modulation region using adaptive optimal third harmonic injection pulsewidth modulation schemes. *IEEE Trans Power Electron* 36(1):1092–1103
- Albatran S, Khalailah ARA, Allabadi AS (2020) Minimizing total harmonic distortion of a two-level voltage source inverter using optimal third harmonic injection. *IEEE Trans Power Electron* 35(3):3287–3297

22. Tan B, Gu Z, Shen K, Ding X (2019) Third harmonic injection SPWM method based on alternating carrier polarity to suppress the common mode voltage. *IEEE Access* 7:9805–9816
23. Morais LMF, Donoso-Garcia PF, Seleme SI, Cortizo PC (2007) Acoustic resonance avoidance in high pressure sodium lamps via third harmonic injection in a PWM inverter-based electronic ballast. *IEEE Trans Power Electron* 22(3):912–918
24. Hava AM, Kerkman RJ et al (1998) Carrier-based PWM-VSI over modulation strategies: analysis, comparison and design. *IEEE Trans Power Electron* 13(4):674–689
25. Rao JS, Tummala SK, Kuthuri NR (2020) Comparative investigation of 15 level and 17 level cascaded h-bridge mli with cross-H-bridge mli fed permanent magnet synchronous motor. *Indones J Electr Eng Comput Sci* 21(2):723–734

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