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RESEARCH PAPER

VDCC-Based Memcapacitor/Meminductor Emulator and Its Application in Adaptive Learning Circuit

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Abstract
In this paper, floating memcapacitor and meminductor emulators have been proposed using voltage differencing current conveyors, memristor and grounded capacitor. Meminductor emulator has been easily obtained from memcapacitor emulator and vice versa by interchanging the positions of memristor and capacitor. The proposed designs of memcapacitor and meminductor emulators are very simple as compared to most of the designs available in the literature. Proposed emulators perform satisfactorily for a wide range of frequency and also satisfy the non-volatility test. The performance of proposed memcapacitor and meminductor emulators has been verified by embedding the memristor emulator circuit and the SPICE model of memristor. The performance of proposed emulators is found to be satisfactory in both the cases. The proposed designs have been simulated by LTspice tool using 0.18 μm CMOS technology parameters. Adaptive learning circuits have also been designed using proposed memcapacitor and meminductor emulators that fully verify the workability of the design.

Keywords VDCC · Memcapacitor · Meminductor · Emulator · Mem-element · Adaptive learning circuit

1 Introduction

Mem-elements are getting phenomenal attention from researchers due to their unique features and wide range of applications especially in neural networks, nonlinear circuits and dense non-volatile memories. Mem-elements are now considered as basic elements of electrical circuits in addition to the well-known elements, namely resistors, capacitors and inductors. The first mem-element is memristor that relates the charge with flux, whereas other two mem-elements are memcapacitor and meminductor that relate charge with voltage, and flux with current, respectively. The three basic elements resistors, capacitors and inductors are well known for a long time, while the first mem-element, namely memristor, came into picture in 1971 with Prof. Chua's prediction (Chua 1971). It remained a hypothetical element until the possibility of physical realization of memristor that was reported in 2008 (Strukov et al. 2008). After 2008, it became an interesting topic of research that motivated engineers to work upon these elements. A lot of research is going on to explore the possibilities of its physical realization and usage in multiple areas of electrical and electronics engineering. Researchers at HP Lab suggested the physical realization of TiO_2-based memristor, but it is still not commercially available in the market. To fulfil the gap and to develop the different applications using memristors, researchers have suggested memristor emulator circuits in many research papers (Kim et al. 2012; Yesil et al. 2014; Sanchez-Lopez and Carrasco-Aguilar 2015; Sanchez-Lopez and Aguila-Cuapio 2017; Sozen and Cam 2016; Ranjan et al. 2017; Kanyal et al. 2018; Yadav et al. 2020a, b; Gupta et al. 2020). After the sufficient work done in the realization of memristor emulators, researchers are now trying to mimic the properties of two other mem-elements, namely memcapacitors and mem-inductors. There are two approaches to design memcapacitor and meminductor emulators. In the first approach, properties of memcapacitor and meminductor are mimicked

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with the help of memristor and some active/passive components. In the second approach, the active inductor circuits available in literature are converted into meminductors in view of making an arrangement which realizes the inductor with memory. Memcapacitor and meminductor emulators were realized first in 2010 using memristor, operational amplifier, resistor and capacitor (Pershin and Ventra 2010). Meminductor emulator has been obtained from memcapacitor emulator by interchanging the positions of capacitor and memristor. Subsequently, a mutator circuit has been reported to transform the memristor into memcapacitor. To serve the purpose of transformation, the mutator circuit has been realized using two AD844 and one resistor. In order to mimic the behaviour of memcapacitor, memristor is terminated at port 2 of the mutator while measuring the input impedance of the circuit at port 1 (Biolek and Biolkova 2010). Floating memcapacitor and meminductor emulators are realized using two single-output or double-output current conveyors, memristor and two passive components (Pershin and Ventra 2011). Thereafter, memristor-less memcapacitor emulator has been reported using multiplier, four op-amps, resistors, capacitors and current-controlled current source (Fouda and Radwan 2012). Next, light-dependent resistor-based memristor model has been utilized to design a memcapacitor emulator in which five op-amps, few resistors and a capacitor are used (Wang et al. 2012). A mutator-based expandable memcapacitor emulator has been reported in which the mutator is designed using two CFOAs, resistor and capacitor. Memristor emulator circuit has been used to terminate the output port of the mutator. Parallel, series and parallel-series combinations of memristor emulators have been connected to the mutator circuit in order to get the respective combinations of memcapacitor emulators (Sah et al. 2013). A floating memcapacitor emulator circuit has been reported using four current-conveyors, memristor emulator, few resistors and capacitor. Memristor emulator has been realized using two op-amps, few resistors, a capacitor and a multiplier (Yu et al. 2013). Next, meminductor and memcapacitor emulators have been reported using memristor emulator, two AD844s, one resistor and a capacitor. Memristor emulator utilized in the designs of meminductor and memcapacitor has been realized using two operational amplifiers, two AD844s, few resistors and capacitors (Y D-Sheng et al. 2014). A floating memristor-less meminductor emulator has been realized using four current-conveyors, resistors, capacitors and a buffer (Liang et al. 2014). A charge-controlled meminductor emulator has been reported using three operational amplifiers, multiplier, few MOSFETs, inductor and capacitor (Sah et al. 2014a). Memristor-less current and voltage-controlled meminductor emulator has been reported using three current-conveyors, multiplier, adder, few resistors and capacitors (Fouda and Radwan 2014). A mutator-based meminductor emulator has been reported using two current conveyors, three operational amplifiers, multiplier, buffer, current sources, few resistors and capacitors (Sah et al. 2014b). Another mutator-based meminductor emulator has been reported using current conveyor, op-amps, buffer, few resistors and capacitor. Memristor emulator has been designed using op-amps, buffer, multiplier, current sources, resistor and capacitor (Sah et al. 2014c). A universal mutator has been reported in which memristor, memcapacitor and meminductor have been obtained using three off-the-shelf active devices, few resistors and a capacitor (Yu et al. 2014). A floating memcapacitor emulator has been realized using an instrumentation amplifier, binary capacitor, switches and resistors (Biolek et al. 2016). A meminductor emulator has been reported using a gyrator that uses two op-amps, memristor, four resistors and a capacitor (Wang 2016). A mutator circuit has been reported using four AD844, one op-amp, four resistors and a capacitor that is capable of emulating memristor, memcapacitor and meminductor (Yu et al. 2019). A universal grounded and floating emulator for memristor, memcapacitor and meminductor has been reported using five CCIIs, one analog multiplier, one op-amp, few resistors and capacitors (Zhao et al. 2019). A meminductor emulator has been reported in which Antoniou's inductance simulation circuit has been modified (Romero et al. 2020). A mutator circuit for memcapacitor and meminductor emulators has been designed using current backward transconductance amplifier, memristor and a capacitor (Taskiran et al. 2020). A universal mutator has been realized using four AD844s, one varactor diode, four resistors and one capacitor (Zheng et al. 2019). Meminductor emulators using two operational amplifiers, one memristor, three resistors and one capacitor have been reported in Singh and Rai (2021). Another meminductor emulator based on Riordan gyrator has been realized using three operational amplifiers, eight resistors, one capacitor and one LED coupled with photoresist (Romero et al. 2021). Recently, a meminductor emulator using two CCIIs, three capacitors and one resistor has been reported in Yesil and Babacan (2020).

It has been observed in the literature survey of mem-element emulators that most of the circuits reported so far in the literature are very complex. In many emulator circuits, analog multipliers have been used. This paper reports a very simple circuit of memcapacitor and meminductor emulator which uses only one active block, namely voltage differencing current conveyor, memristor and a capacitor. The memristor emulator circuit and SPICE model of memristor both have been utilized to check the workability

of the design of memcapacitor and meminductor emulators. The performance of proposed memcapacitor and meminductor emulators has also been verified by designing adaptive learning circuits.

The paper is organized in eight sections including introduction. In Sect. 2, the mem-elements and their inter-relations have been reviewed. The symbolic notation, characteristics and circuit diagram of VDCC are presented in Sect. 3. The proposed designs of memcapacitor and meminductor emulators are discussed in Sect. 4. Simulation results and their discussions are given in Sect. 5. Section 6 covers the performance comparison of proposed emulators with other emulators available in the literature. Adaptive learning circuits using proposed memcapacitor and meminductor emulators are presented in Sect. 7. Concluding remarks are given in Sect. 8.

2 Basic Review of Mem-elements

Mem-elements refer to the family of elements comprising memristor, memcapacitor and meminductor. The memristor was postulated as the two terminal missing circuit elements by Chua (1971). Memristive system shows nonlinear relationship between flux $\phi(t)$ and charge $q(t)$. Therefore, memristance (M_R) is defined by the following relation

$$d\phi = M_R dq \tag{1}$$

which can be rewritten as

$$V(t) = M_R I(t) \tag{2}$$

where $V(t)$ and $I(t)$ represent the voltage and current of the memristive system. The pinch hysteresis loop between $V(t)$ and $I(t)$ is plotted to determine the system's memristive behaviour. The memcapacitive and meminductive systems are defined by the variables σ and ρ, where ρ is the time integral of the flux and σ is the time integral of the charge as given in Eqs. (3) and (4):

$$\rho(t) = \int_{-\infty}^{t} \varphi(t)\mathrm{d}t \tag{3}$$

$$\sigma(t) = \int_{-\infty}^{t} q(t)\mathrm{d}t \tag{4}$$

Thus, the unique memory property pertaining to the memristive systems can now be easily implied in the capacitive and inductive systems making them memcapacitive and meminductive in nature. Memcapacitive systems are generally defined by the relation as

$$\mathrm{d}\sigma = M_c \mathrm{d}\phi \tag{5}$$

where M_C is the memcapacitance of the system. Redefining above equation we get

$$q(t) = M_c V(t) \tag{6}$$

where $q(t)$ and $V(t)$ are the charge and its corresponding voltage of the memcapacitive system, respectively. The pinched hysteresis loop in memcapacitive system is plotted between $q(t)$ and $V(t)$. Similarly, a meminductive system is characterized by the following relation

$$\mathrm{d}\rho = M_L \mathrm{d}q \tag{7}$$

where M_L is the meminductance of the system. Equation (7) can be rewritten as:

$$\phi(t) = M_L I(t) \tag{8}$$

where $\phi(t)$ and $I(t)$ are the induced flux and its corresponding current in the meminductive system, respectively. The pinched hysteresis loop for the meminductive system is observed between $\phi(t)$ and $I(t)$.

3 Voltage Differencing Current Conveyor (VDCC) and Its Properties

The voltage differencing current conveyor (VDCC) is a six terminal block out of which two terminals P and N are input terminals, Z and X are intermediate terminals and W_P and W_N are output terminals. It combines the advantages of both voltage differencing unit and current conveyor. The impedances of all terminals are very high except "X" terminal. The input currents Ip and In are zero as given in Eq. (9). Two voltages (Vp and Vn) are applied to the input terminals P and N, current Iz is obtained at intermediate terminal "Z" as given in Eq. (10). An impedance is connected to "Z" terminal to obtain the voltage Vz that is copied to "X" terminal of VDCC as given in Eq. (11). Current Ix of "X" terminal is conveyed to two output terminals "W_P" and "W_N" as given in Eq. (12). The symbolic notation and circuit diagram of VDCC are given in Figs. 1

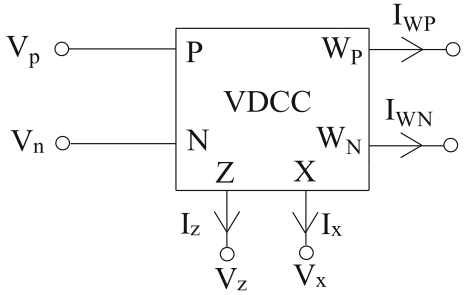

Fig. 1 Symbolic notation of VDCC

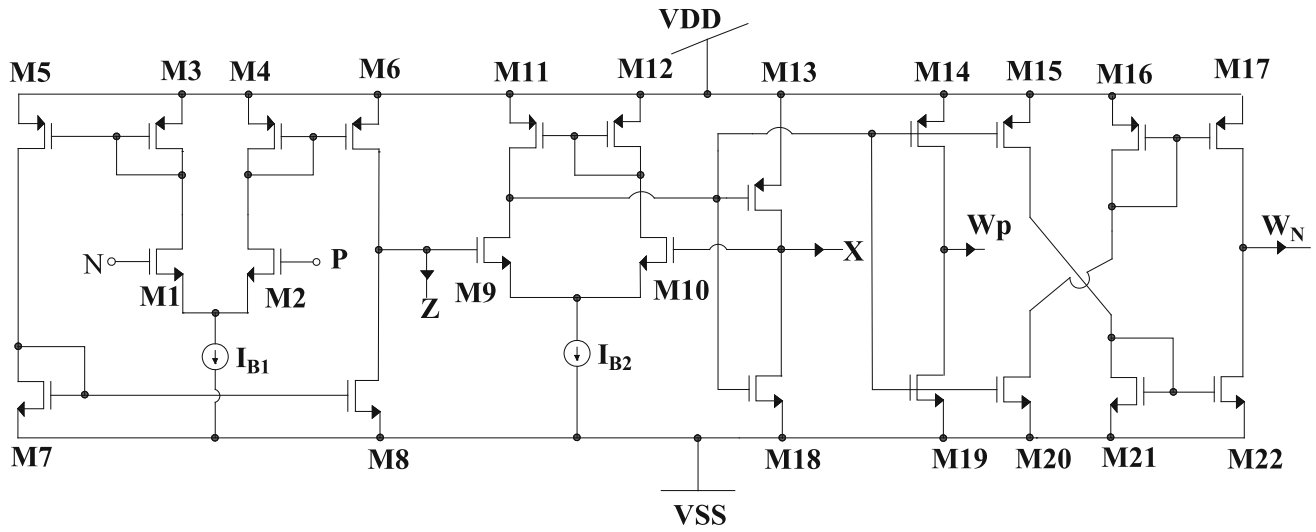

Fig. 2 Circuit diagram of VDCC (Kacar et al. 2014)

and 2. The transconductance of VDCC is controlled by the bias current I_{B1} as given in Eq. (13).

$$I_P = I_N = 0 \tag{9}$$

$$I_Z = G_m(V_P - V_N) \tag{10}$$

$$V_X = V_Z \tag{11}$$

$$I_{WP} = I_X\,, \qquad I_{WN} = -I_X \tag{12}$$

$$G_m = \sqrt{\mu_n . C_{ox} . \frac{W}{L} I_{B1}} \tag{13}$$

4 Proposed Floating Memcapacitor/ Meminductor Emulator

The proposed floating memcapacitor/meminductor emulator circuit using single voltage differencing current conveyor, a memristor and a grounded capacitor is shown in Fig. 3. The emulator of Fig. 3 has been designed on the principle of mutator in which terminals "a" and "c" are connected to terminals "b" and "d", respectively, to realize memcapacitor emulator, whereas terminals "a" and "c" are connected to terminals "d" and "b", respectively, to realize meminductor emulator. This proves the universality of our design. The VDCC-based memristor emulator shown in Fig. 4 is utilized in the design of proposed memcapacitor and meminductor emulators.

4.1 Analysis of the Proposed Memcapacitor

Figure 3 represents the proposed memcapacitor emulator circuit when terminals "*a*" and "*c*" are connected to terminals "*b*" and "*d*" respectively. The routine analysis of the circuit yields the following equation:

$$V_Z = V_X = G_m V_{in}(t).M_R \tag{14}$$

where V_{in} (t) = V_{in1} (t) – V_{in2} (t).

The voltage V_X can also be written as:

$$V_X = \frac{1}{C_1}\int I_X(t)\mathrm{d}t \tag{15}$$

The input current I_{in1} can easily be obtained as:

$$I_{in1} = -I_{WN} = I_X \tag{16}$$

From Eqs. (14), (15) and (16), we get

$$G_m V_{in}(t) M_R = \frac{1}{C_1}\int I_{in1}(t)\mathrm{d}t = \frac{1}{C_1}(q_{in}(t)) \tag{17}$$

that leads to the value of charge q_{in} (t) as

$$q_{in}(t) = G_m C_1 M_R V_{in}(t) \tag{18}$$

Comparing Eq. (18) with Eq. (6), the value of memcapacitance (M_C) is deduced as

$$M_C = G_m C_1 M_R \tag{19}$$

Equation (19) is further analysed using SPICE model of HP memristor (Biolek et al. 2009). The memristance of the HP memristor is given as

$$M_R = [R_{ON}x(t) + R_{OFF}(1 - x(t))] \tag{20}$$

where R_{OFF} and R_{ON} are the equivalent resistances of the HP memristor when it is undoped and doped, respectively, the state variable $x(t)$ is represented by $\frac{W(t)}{D}$, $W(t)$ is the state variable for the length of doped T_iO_2, D is the total T_iO_2 length in HP memristor.

After substituting the value of M_R from Eq. (20) to Eq. (19), we get

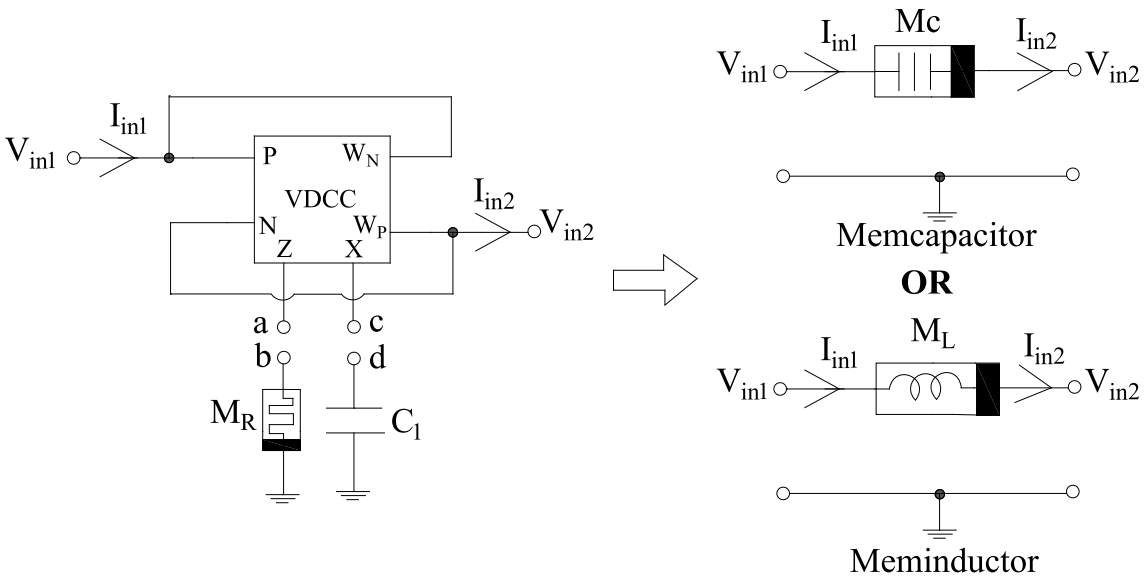

Fig. 3 Proposed memcapacitor and meminductor emulators

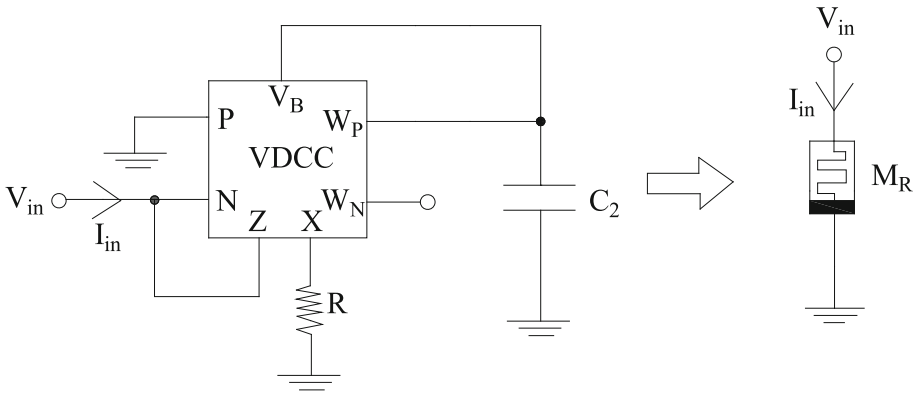

Fig. 4 VDCC-based memristor emulator used in Fig. 3 (Yesil et al. 2019)

$$M_C = G_m C_1 R_{\mathrm{OFF}} + G_m C_1 (R_{\mathrm{ON}} - R_{\mathrm{OFF}}) x(t) \quad (21)$$
$$\leftarrow \text{Fixed} \rightarrow \leftarrow \text{Variable} \rightarrow$$

It is inferred from Eq. (21) that the memcapacitance of proposed memcapacitor emulator designed using HP memristor comprised two parts, namely fixed and variable. The fixed part depends on the transconductance of the VDCC. It also depends on the values of capacitor and off-resistance (R_{OFF}) of the memristor used in proposed memcapacitor emulator. The variable part depends on both internal state $x(t)$ and on the values of on-resistance and off-resistance (R_{ON} and R_{OFF}) of HP memristor. It also depends on the value of capacitor used in the design. When VDCC-based memristor emulator circuit (Fig. 4) is embedded in place of memristor (M_R) used in the proposed memcapacitor emulator circuit of Fig. 3, the value of memristor (M_R) is obtained as given in Eq. (22)

$$M_R = \frac{1}{g_m} = [K(V_B - V_{ss} - V_{th})]^{-1} \quad (22)$$

where $K = \mu_n C_{ox} \frac{W}{L}$, $V_B = \frac{\phi_1}{RC_2}$ and φ_1 is the flux of VDCC-based memristor emulator.

Replacing the value of M_R from Eq. (22) to Eq. (19), we obtain

$$M_C = G_m C_1 [K(V_B - V_{ss} - V_{th})]^{-1} \quad (23)$$

Substituting the value of $V_B = \frac{\phi_1}{RC_2}$ and rearranging Eq. (23) results in

$$M_C = \frac{G_m R C_1 C_2}{K\phi_1} \left[1 - \frac{RC_2(V_{ss} + V_{th})}{\phi_1}\right]^{-1} \quad (24)$$

From Eq. (24), it is clear that memcapacitance of the proposed memcapacitor emulator depends on the flux (Φ_1) and the values of resistor (R) and capacitor (C_2) used in the memristor emulator. It also depends on value of the capacitor (C_1) used in the proposed memcapacitor emulator and on various technology parameters.

4.2 Analysis of the Proposed Meminductor

The meminductor emulator circuit (Fig. 3) is realized when terminals "a" and "c" are connected to terminals "d" and "b", respectively. The routine analysis of meminductor emulator shown in Fig. 3 yields the following equations:

$$V_Z = \frac{1}{C_1}\int I_Z(t)\mathrm{d}t \tag{25}$$

$$V_Z = \frac{1}{C_1}\int G_m V_{in}(t)\mathrm{d}t \tag{26}$$

$$V_Z = \frac{G_m}{C_1}\phi_{in}(\mathrm{t}) \tag{27}$$

The voltage V_z can also be represented as:

$$V_Z = V_X = I_X(t)M_R \tag{28}$$

With the help of Eqs. (27) and (28), the value of flux ϕ_{in} can be represented as:

$$\phi_{\mathrm{in}}(t) = \frac{C_1 M_R}{G_m} I_X(t) \tag{29}$$

Rewriting Eq. (29), we get:

$$\phi_{\mathrm{in}}(t) = \frac{C_1 M_R}{G_m} I_{\mathrm{in}}(t) \tag{30}$$

Comparing Eq. (30) with Eq. (8), the meminductance (M_L) is deduced as:

$$M_L = \frac{C_1 M_R}{G_m} \tag{31}$$

Equation (31) is further analysed using SPICE model (Biolek window) of HP memristor.

Substituting the value of memristor M_R from Eq. (20) into Eq. (31), we get

$$M_L = \underbrace{\frac{C_1 R_{\mathrm{OFF}}}{G_m}}_{\leftarrow \text{ Fixed } \rightarrow} + \underbrace{\frac{C_1(R_{\mathrm{ON}} - R_{\mathrm{OFF}})x(t)}{G_m}}_{\leftarrow \text{ Variable } \rightarrow} \tag{32}$$

It is deduced from Eq. (32) that the meminductance of proposed meminductor emulator designed using HP memristor is comprised of two parts, namely fixed and variable. The fixed part depends on the values of capacitor (C_1) and off-resistance of memristor (R_{OFF}). The variable part depends on internal state $x(t)$ as well as on-resistance and off-resistance (R_{ON} and R_{OFF}) of HP memristor. When VDCC-based memristor emulator circuit (Fig. 4) is embedded in place of memristor (M_R) used in the proposed meminductor emulator circuit of Fig. 3, the value of memristor (M_R) is obtained as given in Eq. (22).

Replacing the value of memristor (M_R) from Eq. (22) into Eq. (31), we get

$$M_L = \frac{C_1[K(V_B - V_{ss} - V_{th})]^{-1}}{G_m} \tag{33}$$

Substituting $V_B = \frac{\Phi_1}{RC_2}$ and rearranging the terms result in the value of meminductance as:

$$M_L = \frac{RC_1C_2}{G_m K\phi_1}\left[1 - \frac{RC_2(V_{ss} + V_{th})}{\phi_1}\right]^{-1} \tag{34}$$

It can be concluded from Eq. (34) that the meminductance of proposed meminductor emulator depends on the values of flux (Φ_1), resistor (R) and the value of capacitor (C_2) used in the memristor emulator. It also depends on the value of the capacitor (C_1) used in the proposed meminductor emulator.

5 Simulation Results and Discussions

The proposed floating memcapacitor/meminductor emulator circuit is simulated using LTspice tool with TSMC 180 nm CMOS technology parameters. The supply voltage is chosen as ± 0.9 V. The value of resistor (R) shown in Fig. 4 is chosen as 2 kΩ. The aspect ratios of MOSFETs used in the design of VDCC are given in Table 1.

5.1 Simulation Results of Proposed Memcapacitor Emulator

The proposed memcapacitor emulator shown in Fig. 3 is simulated employing both the SPICE model of HP memristor (Biolek window) and the VDCC-based memristor emulator shown in Fig. 4. The plots depicting transient response and the pinched hysteresis loop for the proposed memcapacitor emulator using SPICE model of HP memristor (Biolek window) are shown in Fig. 5a, b. Pinched hysteresis loop is obtained between voltages V_X and V_{in} that indirectly plots the curves between charge (q) and voltage (V). These responses are obtained for the input sinusoidal voltage having amplitude of 100 mV and frequency of 0.6 Hz. The value of capacitor C_1 is chosen as 50 pF. Figure 6a depicts the pinched hysteresis curves at

Table 1 Aspect ratios of MOSFETs

MOSFETs	W (μm)	L (μm)
M1–M4	3.6	1.8
M5–M6	7.2	1.8
M7–M8	2.4	1.8
M9–M10	3.06	0.72
M11–M12	9	0.72
M13–M17	14.4	0.72
M18–M22	0.72	0.72

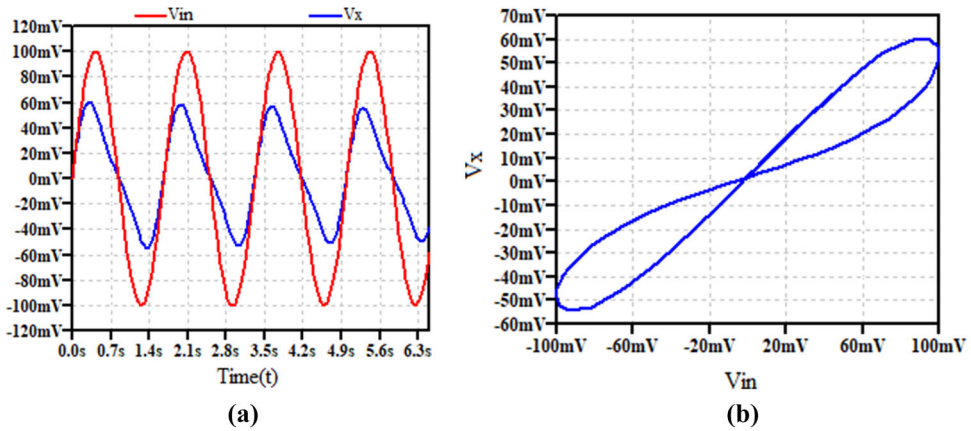

Fig. 5 **a** Transient analysis of proposed memcapacitor emulator and **b** pinched hysteresis loop between voltages V_x and V_{in}

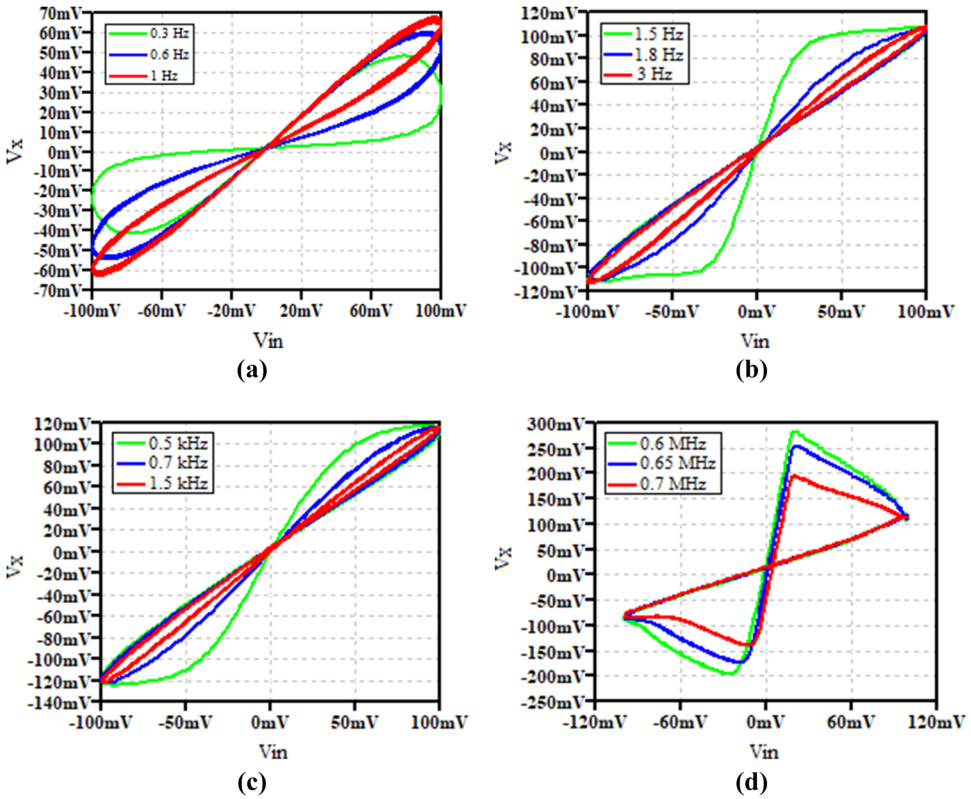

Fig. 6 Pinched hysteresis loops of memcapacitor emulator using **a** SPICE model of HP memristor, **b–d** VDCC-based memristor emulator

different frequencies when simulated using SPICE model of HP memristor. Pinched hysteresis loops of memcapacitor emulator have also been obtained using VDCC-based memristor emulator for different frequencies extending from hertz to several hundreds of kilohertz range as shown in Fig. 6b–d. These loops have been obtained by appropriately scaling the values of capacitors C_1 and C_2. The pinched hysteresis loops of Fig. 6b are obtained when the values of capacitors C_1 and C_2 are selected as 10 μF and 18 μF, respectively. Pinched hysteresis loops of Fig. 6c are obtained for the values of capacitors $C_1 = 20$ nF and $C_2 = 85$ nF. Similarly, the pinch hysteresis loops shown in Fig. 6d are obtained when values of capacitors C_1 and C_2 are chosen as 50 pF and 18 pF, respectively Therefore, it can be concluded that proposed memcapacitor emulator works satisfactorily for low to high frequency range. It is observed from Figs. 6a–d that the pinched hysteresis loop shrinks when frequency is increased.

The non-volatility property of the proposed memcapacitor emulator is verified by applying the pulse input (V_{in}) of 20 mV amplitude and 0.55 Hz frequency to the memcapacitor circuit designed using the SPICE model of HP memristor. The memory retaining property is shown in Fig. 7 by plotting the voltage (V_X) at X terminal of memcapacitor emulator as it is the value corresponding to the charge (q_{in}). It can be observed from Fig. 7 that during

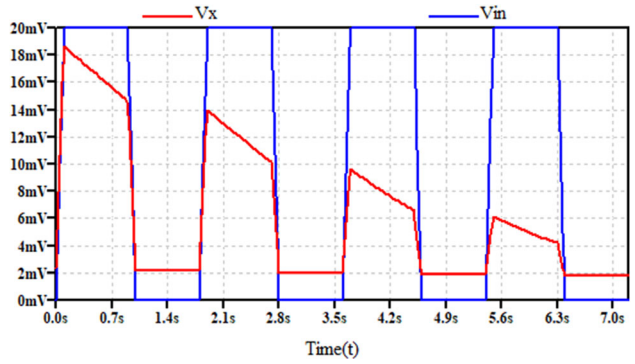

Fig. 7 Non-volatility test of the proposed memcapacitor emulator

"on" period of the input pulse the voltage (V_X) decreases from the value 18 mV to 15 mV, while for the "off" period, it retains the same voltage 15 mV and starts decreasing it for the "on" period of next cycle of the input pulse. The same effect can be observed for the four cycles of the input pulse. Thus, the proposed memcapacitor emulator verifies the non-volatility property.

5.2 Simulation Results of Proposed Meminductor Emulator

The proposed meminductor emulator shown in Fig. 3 has been simulated employing both the SPICE model of HP memristor (Biolek window) and the VDCC-based memristor emulator shown in Fig. 4. The transient response and the pinched hysteresis loop for the proposed meminductor emulator using SPICE model of HP memristor are shown in Fig. 8a, b. These responses have been obtained by applying the input current signal of 25 μA amplitude and 0.6 Hz frequency, and the value of capacitor C_1 is chosen as 20 pF. The simulations of the proposed meminductor emulator designed using VDCC-based memristor are done by applying input sinusoidal voltage having amplitude of 100 mV. It can be deduced from Eq. (27) that flux (Φ_{in}) is proportional to voltage (V_Z) at Z terminal of the meminductor emulator. Thus, for the ease of plotting, pinched hysteresis loop is plotted between voltage (V_Z) and current (I_{in}) of the proposed meminductor emulator.

The pinched hysteresis loops for different frequencies obtained by using the SPICE model of HP memristor are shown in Fig. 9a. Pinched hysteresis loops for different frequencies ranging from hertz to several hundreds of kilohertz are also plotted for the meminductor emulator using VDCC-based memristor. These loops are plotted by appropriately adjusting the values of capacitors C_1 and C_2. The pinched hysteresis loops of Fig. 9b are obtained when the values of capacitors C_1 and C_2 are selected as 10 μF and 40 μF, respectively. Pinched hysteresis loops of Fig. 9c are obtained for the values of capacitors C_1 = 10 nF and C_2 = 40 nF. Similarly, the pinch hysteresis loops shown in Fig. 9d are obtained when values of capacitors C_1 and C_2 are chosen as 10 pF and 50 pF, respectively Therefore, it can be concluded that proposed meminductor emulator works satisfactorily for low to high frequency range. It is observed from Fig. 9a–d that the pinched hysteresis loop shrinks when frequency is increased.

The non-volatility property of the proposed meminductor emulator is verified by applying the current pulse input (I_{in}) of amplitude 5 μA and frequency of 0.55 Hz to the meminductor emulator designed using SPICE model of HP memristor. The memory retaining property is shown in Fig. 10 by plotting the voltage (V_Z) at Z-terminal of meminductor emulator as it is the value corresponding to the charge (Φ_{in}). It can be observed from Fig. 10 that during "on" period of the input pulse the voltage V_Z decreases from 16 to 12 mV, while it retains the value of voltage V_Z for the "off" period. When the next input pulse arrives, the voltage V_Z starts decreasing again for the "on" period of input pulse and retained its value for the "off" period of input pulse. The non-volatility property is shown in Fig. 10 for four cycles of the input pulses. Therefore, proposed meminductor emulator verifies the property of non-volatility.

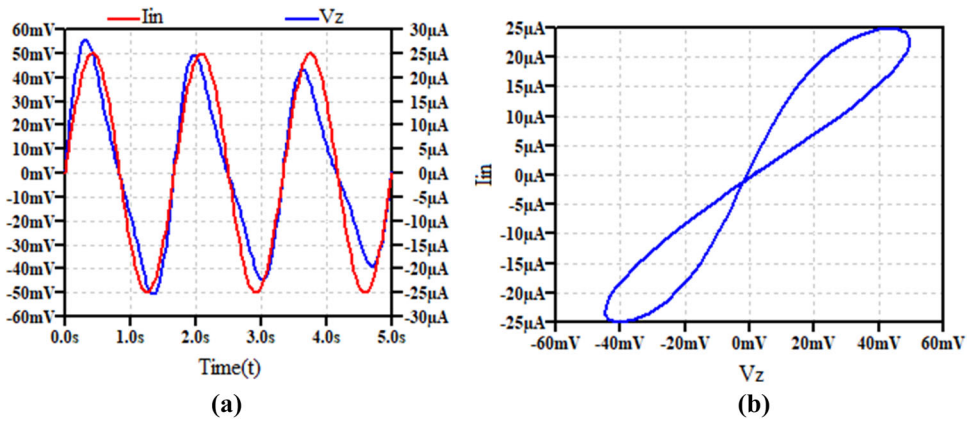

Fig. 8 **a** Transient analysis of proposed meminductor emulator. **b** Pinched hysteresis loop between voltage (V_z) and current (I_{in})

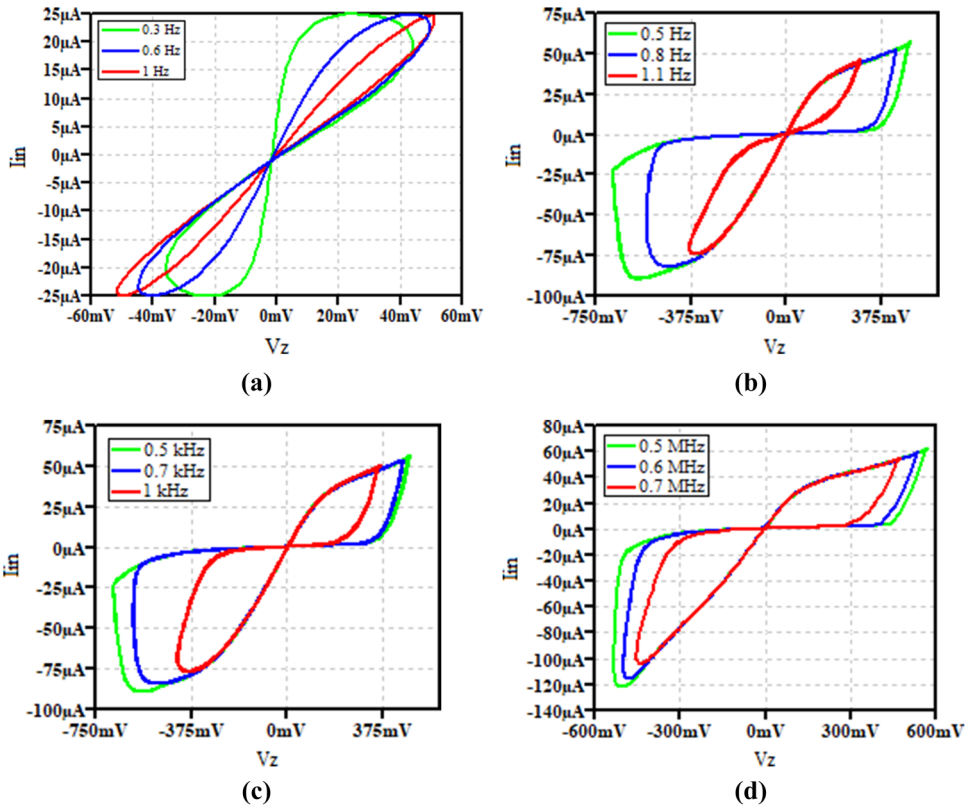

Fig. 9 Pinched hysteresis loops of meminductor emulator using **a** SPICE-based memristor emulator, **b–d** VDCC-based memristor emulator

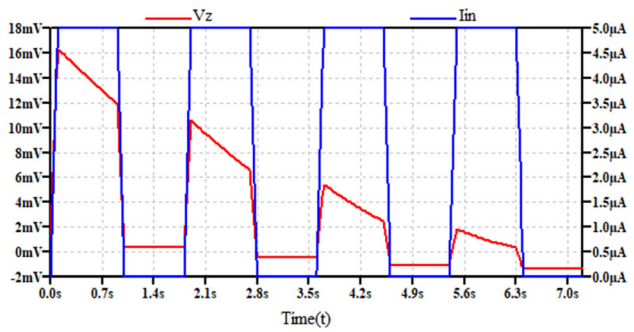

Fig. 10 Non-volatility test of the proposed meminductor emulator

6 Comparison of Proposed Emulators with Other Reported Emulators in the Literature

The proposed memcapacitor and meminductor emulators have been compared with other reported memcapacitor/meminductor emulators in the literature. The comparison is done on the basis of number of active and passive components, range of frequency, floating/grounded configurations of emulators and types of realizations. The following conclusions have been drawn on the basis of Table 2.

1. The proposed emulators use only one active block and two passive components, whereas other emulators reported in references (Biolek and Biolkova 2010; Pershin and Ventra 2011; Fouda and Radwan 2012, 2014; Wang et al. 2012; Sah et al. 2013, 2014a, b, c; Yu et al. 2013, 2019; Sheng et al. 2014; Liang et al. 2014; Yu et al. 2014; Biolek et al. 2016; Wang 2016; Zhao et al. 2019; Romero et al. 2020, 2021; Zheng et al. 2019; Singh and Rai 2021; Yesil and Babacan 2020) use large number of active and passive components.
2. Proposed circuits realize both memcapacitor and meminductor emulators, whereas emulators reported in references (Biolek and Biolkova 2010; Fouda and Radwan 2012, 2014; Wang et al. 2012; Sah et al. 2013, 2014a, b, c; Yu et al. 2013; Liang et al. 2014; Biolek et al. 2016; Wang 2016; Romero et al. 2020, 2021; Singh and Rai 2021; Yesil and Babacan 2020) realize either memcapacitor or meminductor emulator.
3. Proposed emulators are floating type, whereas reported emulators in references (Pershin and Ventra 2010; Biolek and Biolkova 2010; Fouda and Radwan 2012, 2014; Wang et al. 2012; Sah et al. 2014a, b; Wang 2016; Romero et al. 2020; Singh and Rai 2021) realize only grounded configuration.
4. Pinched hysteresis loop of proposed emulators is maintained up to 700 kHz, whereas emulators reported

Table 2 Comparison of proposed emulators with existing emulators

Ref	No. of blocks	No. of passive elements	Range of Freq	Floating/grounded (F/G)	Meminductor/ memcapacitor
Pershin and Di Ventra (2010)	1 op-amp	3 ($1M_R$, 1C, 1R)	8 Hz	G	Both
Biolek and Biolkova (2010)	2 AD844	3 ($1M_R$,1C,1R)	1 Hz	G	Memcapacitor
Pershin and Di Ventra (2011)	4 CCIIs	3 ($1M_R$,1C,1R)	–	F	Both
Fouda and Radwan (2012)	4 op-amp, 1 multiplier, 1 current source	4 (2R, 2C)	10 Hz	G	Memcapacitor
Wang et al. (2012)	3 op-amp, 2 AD 844, 1 diode	16 (13R, 2C, 1 LDR)	10 Hz	G	Memcapacitor
Sah et al. (2013)	2 CFOAs	3 ($1M_R$, 1R, 1C)	900 Hz	F	Memcapacitor
Yu et al. (2013)	4 AD844s	4 ($1M_R$, 2R, 1C)	86.6 Hz	F	Memcapacitor
Yu et al. (2014a)	2 CCII, 2 op-amp, 3 multiplier	2 (1R,1C)	24.1 Hz	F	Both
Liang et al. (2014)	2 CCII, 3 op-amp, 1 multiplier	9 (7R,2C)	28.3 Hz	F	Meminductor
Sah et al. (2014a)	3op-amp,1 multiplier, 1 Voltage differentiator	3 (2C,2R,1L)	300 Hz	G	Meminductor
Fouda and Radwan (2014)	3 CCII + , 1 multiplier, 1 adder	5 (3R, 2C)	10 Hz	G	Meminductor
Sah et al. (2014b)	4 op-amp, 2 CCII,1Multiplier	9 (2C,7R)	800 Hz	G	Meminductor
Sah et al. (2014c)	3 op-amp, 1 CCII +	5 ($1M_R$, 3R, 1C)	400 Hz	F	Meminductor
Yu et al. (2014a)	3 Trans-impedance op-amps	5 (2C,2R,1MC)	21.1 Hz	F	Both
Biolek et al. (2016)	1 Instrumentation amplifier, 3 op-amp,	9 (5R, 4C)	1 kHz	F	Memcapacitor
Wang (2016)	2 op-amp	7 ($2M_R$,1C,4R)	–	G	Meminductor
Yu et al. (2019)	4 CCII,1op-amp	8 (6R,1C,1VrD)	22 kHz	F	Both
Zhao et al. (2019)	5 CCIIs, 1 voltage buffer	2 (1R, 2C)	5 kHz	F	Both
Romero et al. (2020)	5 op-amp	9 (6R, 3C)	10 kHz	G	Meminductor
Zheng et al. (2019)	4 AD844s, 1 op-amp	8 (4R, 3C, 1VrD)	180 kHz	F	Both
Singh and Rai (2021)	2 op-amp	5 (1 M_R, 3R, 1C)	2 MHz	G	Meminductor
Romero et al. (2021)	3 op-amp	10 (8R, 1C, 1LED coupled with photoresist)	10 kHz	F	Meminductor
Yesil and Babacan (2020)	2 CCII or 1 CCII and 1 OTA, 1 Multiplier	4 (1R, 3C) or 3C	2 kHz	F	Meminductor
Proposed work	1 VDCC	2 (1 M_R, 1C)	700 kHz	F	Both

in references (Pershin and Ventra 2010,2011; Biolek and Biolkova 2010; Fouda and Radwan 2012, 2014; Wang et al. 2012; Sah et al. 2013, 2014a, b, c; Yu et al. 2013; Y D-Sheng et al. 2014; Liang et al. 2014; Yu et al. 2014) form pinched hysteresis loop in the frequency range of Hz only. The emulators reported in references (Biolek et al. 2016; Yu et al. 2019; Zhao et al. 2019; Romero et al. 2020, 2021; Zheng et al. 2019; Yesil and Babacan 2020) provide pinched hysteresis loops in kHz range but varies only from 1 to 180 kHz.

7 Application of Proposed Memcapacitor and Meminductor Emulators in Adaptive Learning Circuit

Mem-elements are widely being used in various fields and applications. One of the popular applications is adaptive neuromorphic circuits and neural networks (Pershin et al. 2009; Pershin and Ventrai 2010; Wang et al. 2013; Erokhin 2020; Sangwan and Hersam 2020; Alexander et al. 2021). In this section, adaptive learning

circuit using proposed memcapacitor and meminductor emulators is realized as shown in Fig. 11a, b. This model of the neuromorphic adaptive learning circuit is derived from the behavioural response of the amoeba (a unicellular organism) (Pershin et al. 2009; Wang et al. 2013). Amoeba generally reacts to changes in its environmental conditions like temperature and humidity by slowing down its locomotive speed. In this process, it memories past events and nearly predicts the timing of future events having periodicity with the past ones (Wang et al. 2013). The adaptive learning circuits shown in Figs. 11a, b are the electronic analogous model of the amoeba's behavioural response. Input voltage (V_{in}) shown in Fig. 12a corresponds to the temperature changes in amoeba's environment, and output voltages (V_{out1} and V_{out2}) correspond to variation in the locomotive speed of the amoeba in response to temperature changes. The values of meminductor and memcapacitor element change with respect to variation in the values of the input signal across them. This finally results in the tuning of the designed adaptive learning circuit with that of input voltage (temperature variation) frequency. Component values for the adaptive learning circuit as shown in Fig. 11a are $R = 1\ \Omega$, $L = 1\ \mu H$, and its memcapacitor is having component values of $C_1 = 1$ nF with Biolek window-based SPICE model of HP memristor. In Fig. 11b, the values of the components are $R = 1\ \Omega$, $C = 0.1$ pF and its meminductor is having component values of $C_1 = 300$ pF with HP memristor based on the Biolek window SPICE model. Figure 12b, c shows the simulation results for the circuits shown in Fig. 11a, b, respectively. From Fig. 12b, c, it is observed that at each point of the temperature drop the corresponding output locomotive speed also drops. With periodic drop in input voltage (temperature drop), the locomotive speed, i.e. V_{out1} and V_{out2}, drops further as compared to its previous drop value. This verifies the adaptive learning process. From these adaptive learning circuit realization, our proposed circuits qualify for the neuromorphic applications.

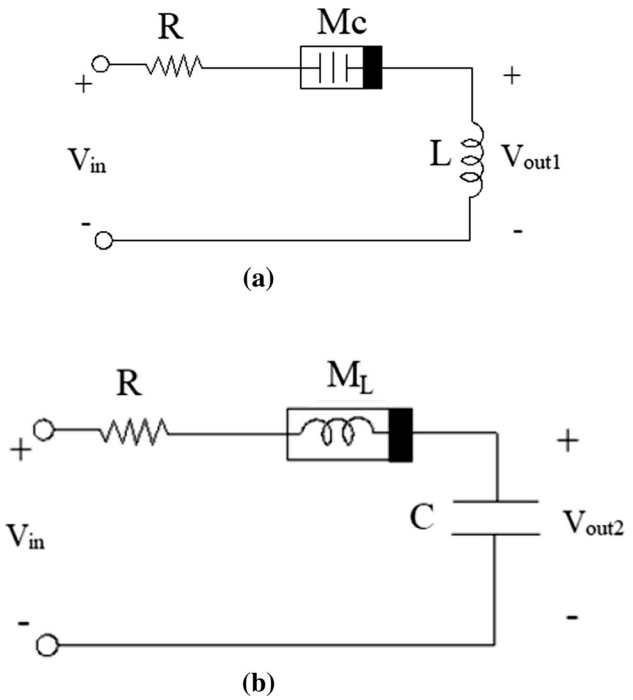

Fig. 11 Adaptive learning circuits using **a** proposed memcapacitor and **b** proposed meminductor

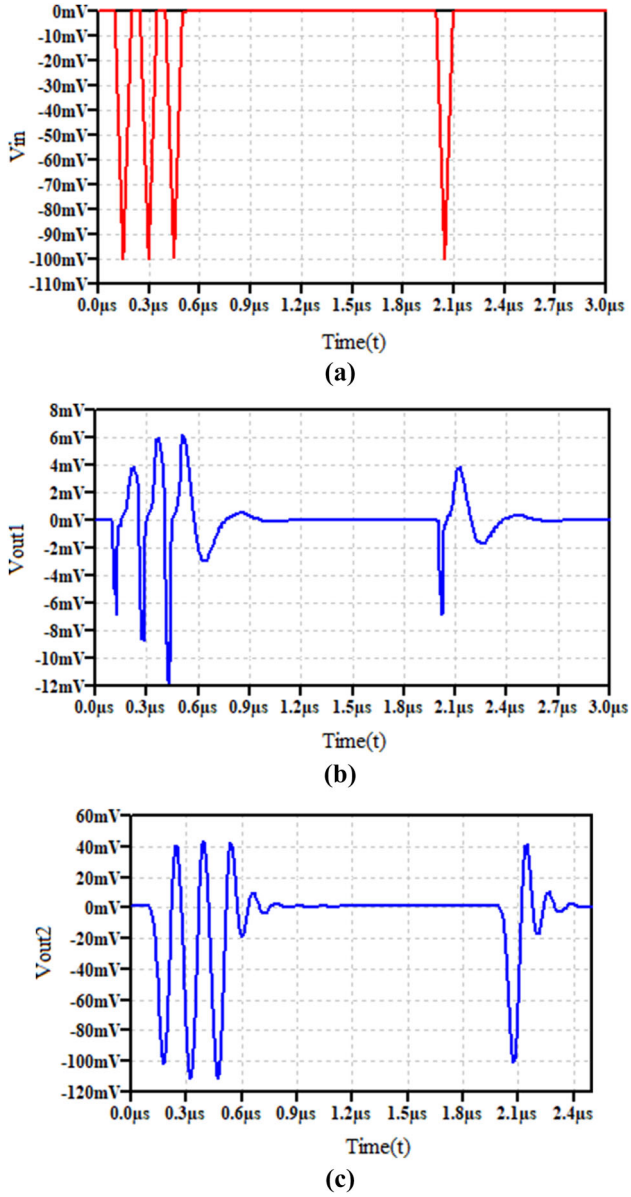

Fig. 12 **a** Applied input voltage pulse (V_{in}). **b** Obtained output response (V_{out1}). **c** Obtained output response (V_{out2})

8 Conclusion

In this work, memcapacitor and meminductor emulators have been proposed using voltage differencing current conveyor, memristor and a capacitor. The proposed emulators have been designed using both SPICE model of memristor and VDCC-based memristor emulators. The obtained pinched hysteresis loops indicate the workability of the proposed design for a wide range of frequencies. The performance of proposed emulators has been verified by designing an adaptive learning circuit. The output responses of the adaptive learning circuits using memcapacitor and meminductor emulators verify their performance. The proposed memcapacitor and meminductor emulators have been compared with existing memcapacitor and meminductor emulators in the literature. It is concluded that the proposed design is very simple over most of the designs available in the literature.

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