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RESEARCH PAPER

An Interleaved High Step-Up DC–DC Converter with Low Voltage Stress

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Abstract
The present paper proposes a kind of interleaved high step-up converter without the coupled inductor. The converter consists of two basic boost converters and two voltage multiplier cells. The proposed converter has a lower input current rippled by means of the interleaving method. The voltage stress of the switches remains at a low level. The theoretical analysis and operation intervals of the proposed high step-up converter are presented. The voltage gain of the converter is higher than that of the similar converters. The converter is simulated in the OrCAD software. In this converter, the inductors operate in a continuous flow mode CCM. In this topology, the input voltage is 40 V, which is converted to the output 400 V with a power of 200 W and a frequency of 100 kHz. The voltage stress of the switches is 120 V, which is much lower than the output 400 V. Finally, the experimental results are presented to validate the effectiveness of the proposed converter.

Keywords Step-up converter · Interleaved · Voltage stress · High voltage gain · Low current ripple

1 Introduction

The importance of renewable energy sources has been increased recently due to their benefits, such as the lack of limitations and environmental pollution, as well as their high reliability. Sunlight is known as a clean and free renewable energy source (Shimizu et al. 2003). Photovoltaic (PV) cells are utilized to convert solar energy into electrical energy (Scarpa et al. 2009). Since the voltage level generated by the PV cells is small, the DC–DC voltage converters can be used to boost it to the desired level (Salary et al. 2017). Accordingly, the voltage level required by the inverter input to convert the DC voltage to AC voltage can be attained (Figueres et al. 2009).

The DC voltage generated by the PV module is usually enhanced by a DC–DC converter to reach the desired level. Since most electric consumers need AC voltage, the amplified DC voltage is converted to the AC voltage by an inverter. (Figueres et al. 2009; Chen et al. 2018; Liu and Xhang 2019).

Various types of boost converters are employed to increase the voltage level. The conventional boost converter can produce a gain no more than 5 (Lopez et al. 2006). Moreover, it leads to hard switching, which increases converter losses at high frequencies. On the other hand, due to high stress in the diode voltage and the converter switch, the elements that are at reasonable prices have poor quality. In this regard, the conductive and reverse recovery losses of the diodes are also problematic. This requires us to employ optimal interleaved boost converters. These converters are generally divided into several categories. The first one is the conventional interleaved boost converter, which contains a series of auxiliary circuits added to each phase consisting of an active key, a capacitor, and an inductor. The main switches are naturally switched on at zero current, and the output diodes' reverse voltage problem is reduced due to the performance of the discontinuous flow mode (DCM). The auxiliary commutation circuits provide a transient zero current mode when the main switch is off. However, the variable frequency control is obligatory for this converter, which makes it difficult to design a filter to reduce electromagnetic

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interference (Jemei et al. 2008). The second category is the interleaved boost converter coupled with an inductor. In these converters, the output diodes' reverse voltage problem is reduced. In addition, the coupled inductor's leakage inductor leads to zero current switching (ZCS)of the switches. These switches are switched off rigorously. The circuit current ripple in negatively coupled inductors is high because the circuit operates in a discontinuous mode, and the switching loss is low due to zero switching operation in all switching intervals (Todorovic et al. 2008). The third category is a three-layer boost converter, which can reduce the voltage stress of semiconductor devices by half, which makes it more suitable for high output voltage applications compared with conventional two-layer boost converters. Switching losses and the noise induced by electromagnetic interference (EMI) can be reduced by low voltage stress. The activated switches work well in hard switching and increase the resonance inductor of the voltage stress (Hwu and Yau 2009). The last category contains new DC–DC boost converters with a coupled inductor and multiplier circuits. In this converter, a high voltage gain with appropriate duty factor and low voltage stress in power switches are provided. Furthermore, the stored energy in the inductively coupled inductor's leakage inductor can be returned to the converter output. The steady-state voltage of the two switches is lower than the output voltage. However, the voltage uplift is observed in the switches when they are switched off (Chang et al. 2017; Franceschini et al. 2008). The interleaved high step-up converters based on diode–capacitor multiplier are presented in Zhou et al. (2014) and Yang et al. (2009). These papers propose transformerless converters to achieve high voltage gain without an extremely high duty ratio. The main drawback of these converters is high voltage stress of the switches and diodes.

The remainder of this study is organized as follows. Section 2 introduces an interleaved boost converter to increase the voltage gain without using coupled inductors. Besides, an enhanced arrangement of the boost converter elements and its auxiliary components are offered to increase the gain and reduce the voltage stress while the input current ripple of the converter is kept low. Also, the operation intervals are demonstrated. Section 3 contains the design of considerations and the formula in detail. In Sect. 4, the results in the OrCAD software are utilized to simulate and evaluate the performance of the proposed converter. Section 5includes the experimental results obtained from an implemented laboratory system. They are also provided to validate the accuracy of this converter. Finally, Sect. 6 offers the conclusion of this study.

2 The Proposed Converter and Its Operating Intervals

2.1 CCM Operation

In this section, a new high-gain converter is introduced. Figure 1 shows the circuit of the proposed high-gain interleaved converter. In this converter, the inductor L_1, switch S_1, diode D_3, and capacitor C_{o1} belong to one of the boost converters, while inductor L_2, switch S_2, diode D_6, and capacitor C_{o2} belong to the other one. As a result, diodes D_1 and D_2, capacitors C_1 and C_2, and inductor L_{a1} form the switching capacitor circuit that increases the employed voltage for one of these converters. On the other hand, diodes D_3, D_4, capacitors C_3, and C_4, and inductor L_{a2} form the switching capacitor circuit that increases the employed voltage for the other one. In the proposed converter, the switches are switched according to the desired patterns. In this study, these patterns are considered as two pulses with the same duty factor and 180° phase shift; therefore, the input current ripple and the size of input filter can be effectively reduced (Chen and Lin 2015). Unlike the other switched capacitor-based high-gain interleaved boost converters, there is no limitation on the duty factor in the proposed converter. Moreover, the converter works correctly for all the task coefficients larger or smaller than 0.5.

The converter's operation is divided into six steps, which are adopted successively in each switching cycle. Figure 2 shows the current and voltage curves of the critical components in the proposed converter.

2.1.1 Interval 1: t_0–t_1

In this step, both switches of the proposed converter are switched on. The voltage is equal to the input voltage of the two-terminal inductors L_1 and L_2, where their current linearly increases. The C_2 capacitor charges the capacitor C_1 through C_2-D_2-L_{a1}-C_1-S_1. The C_4 capacitor also charges the capacitor C_3 through C_4-S_2-C_3-L_{a2}-D_5. In this step, the load's current is also determined by C_{o2}-V_{in}-C_{o1}-R_o. This situation ends with switching the switch S_1off. Now, the converter enters the next step. The equivalent circuit of this interval is presented in the Appendix section. The current equations for the inductors L_1, L_2, L_{a1}, and $L_{a2}$are given as:

$$I_{L1}(t) = I_{L1}(t_0) + \frac{V_{in}}{L_1}.(t - t_0) \quad (1)$$

$$I_{L2}(t) = I_{L2}(t_0) + \frac{V_{in}}{L_2} \cdot (t - t_0) \quad (2)$$

$$I_{La1}(t) = I_{La1}(t_0) + \frac{V_{C2} - V_{C1}}{L_{a1}} \cdot (t - t_0) \quad (3)$$

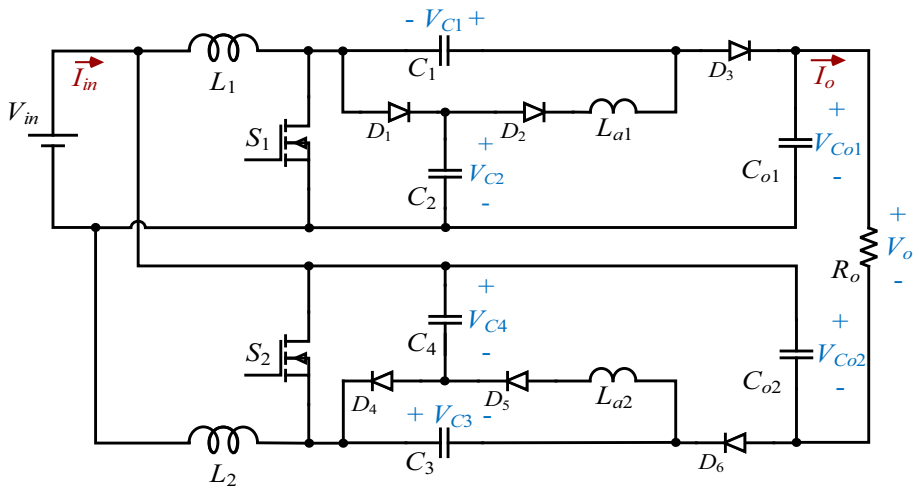


Fig. 1 The circuit of the proposed high-gain interleaved DC–DC converter

$$I_{\mathrm{La2}}(t) = I_{\mathrm{La2}}(t_0) + \frac{V_{C4} - V_{C3}}{L_{\mathrm{a2}}}.(t - t_0) \tag{4}$$

The process duration could be considered as $(D - 0.5)T_{\mathrm{sw}}$.

2.1.2 Interval 2: t_1–t_2

At t_1, the switch S_1 switches off. Afterward, the inductor L_1 switches the diodes D_1 and D_3 on, charges the capacitor C_2 through V_{in}-L_1-D_1-C_2, and charges the capacitor C_{o1} through V_{in}–L_1–C_1–D_3–C_{o1}. The voltage of the capacitor C_1 called VC_1 is adjusted at the two terminals of the inductor L_{a1} through C_1-L_{a1}-D_2-D_1. Accordingly, the currents of inductor L_{a1} and diode D_2 linearly decrease with a steep slope until they tend to zero. This leads to switching off the diode D_2 under ZCS conditions. The current of the inductor L_1 decreases slowly with a slight slope. The same conditions are true for another circuit branch. In this case, the following current equations could be written:

$$I_{L1}(t) = I_{L1}(t_1) - \frac{V_{C2} - V_{\mathrm{in}}}{L_1} \cdot (t - t_1) \tag{5}$$

$$I_{L2}(t) = I_{L2}(t_1) + \frac{V_{\mathrm{in}}}{L_2} \cdot (t - t_1) \tag{6}$$

$$I_{\mathrm{La1}}(t) = I_{\mathrm{La1}}(t_1) - \frac{V_{C1}}{L_{a1}} \cdot (t - t_1) \tag{7}$$

$$I_{\mathrm{La2}}(t) = I_{\mathrm{La2}}(t_1) + \frac{V_{C4} - V_{C3}}{L_{a2}} \cdot (t - t_1) \tag{8}$$

2.1.3 Interval 3: t_2–t_3

At t_2, diode D_2 is switched off, and the converter enters the third stage of its operation. As shown in Fig. 3, in this stage, the switches S_1 and S_2 are off and on, respectively. A part of the inductor current L_1 charges the capacitor C_2 through diode D_1, while another part charges the output capacitor through diode D_3. The operation of another branch is also similar. Now, the current of inductor L_1 linearly decreases with slow slope, while the current of inductor L_2 increases. In this case, the current equations are given as the following (consider that the duration process is $(1 - D)T_{\mathrm{sw}}$):

$$\begin{aligned} I_{L1}(t) &= I_{L1}(t_2) - \frac{V_{C2} - V_{\mathrm{in}}}{L_1} \cdot (t - t_2) \\ &= I_{L1}(t_2) - \frac{V_{Co1} - V_{in} - V_{C1}}{L_1} \cdot (t - t_2) \end{aligned} \tag{9}$$

$$I_{L2}(t) = I_{L2}(t_2) + \frac{V_{\mathrm{in}}}{L_2} \cdot (t - t_2) \tag{10}$$

$$I_{\mathrm{La2}}(t) = I_{\mathrm{La2}}(t_2) + \frac{V_{C4} - V_{C3}}{L_{a2}} \cdot (t - t_2) \tag{11}$$

2.1.4 Interval 4: t_3–t_4

At t_3, S_1 is switched on, and the converter enters this step. As shown in Figs. 3, 4, and 5, the converter operation is similar to the first step. This means that the input voltage is placed at the two terminals of the inductor L_1, which increases the current linearly with a slow slope. Moreover, the voltage shift of the capacitors C_2 and C_1 is placed at the two terminals of the inductor L_{a1} and leads to an increase in the inductor current with another slow slope. In this case, the essential current equations are given as follows. The converter remains in this state until S_2 is switched off. The duration of this process is considered as $(1 - D)\cdot T_{\mathrm{sw}}$.

$$I_{L1}(t) = I_{L1}(t_3) + \frac{V_{\mathrm{in}}}{L_1}.(t - t_3) \tag{12}$$

$$I_{L2}(t) = I_{L2}(t_3) + \frac{V_{\mathrm{in}}}{L_2}.(t - t_3) \tag{13}$$

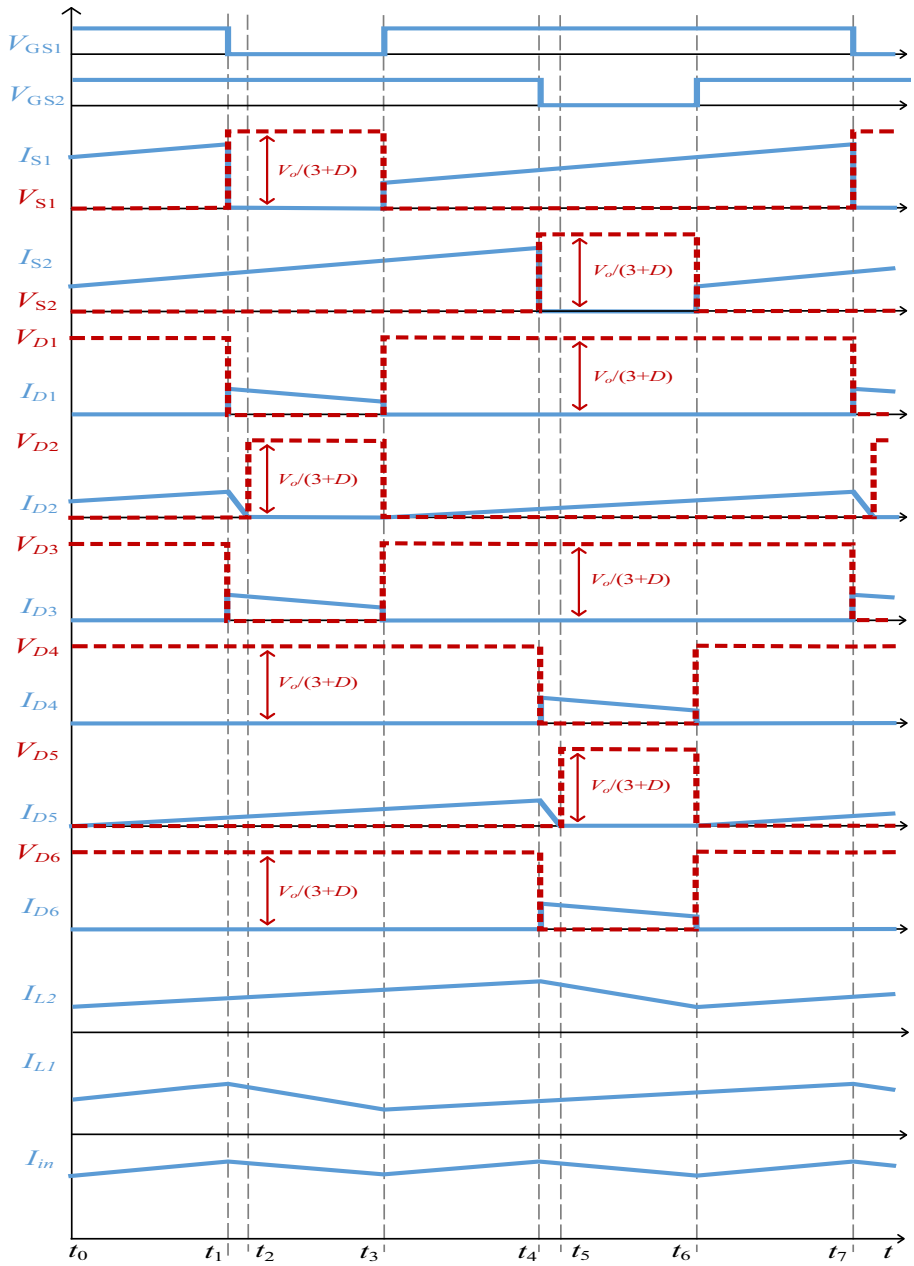


Fig. 2 The current and voltage curves of the key components in the proposed converter

$$I_{\mathrm{La1}}(t) = \frac{V_{C2} - V_{C1}}{L_{a1}} \cdot (t - t_3) \tag{14}$$

$$I_{\mathrm{La2}}(t) = I_{\mathrm{La2}}(t_3) + \frac{V_{C4} - V_{C3}}{L_{\mathrm{a2}}} \cdot (t - t_3) \tag{15}$$

2.1.5 Interval 5: t_4–t_5

At t_4, the switch S_2 in the converter is switched off, and the converter enters this step. In this case, inductor L_2 charges the capacitors C_4 and C_{o2} through the diodes D_4 and D_6, respectively. Since diodes D_4 and D_5 are switched on, the voltage of the capacitor C_3 is positioned at two terminals of the inductor L_{a2}. This reduces its current by a steep slope. This phase lasts for a short time. In this case, the operation of the upper branch of the converter is similar to the corresponding one in the previous step. The important equations for the convertor elements are presented as follows:

$$I_{L1}(t) = I_{L1}(t_4) + \frac{V_{\mathrm{in}}}{L_1} \cdot (t - t_4) \tag{16}$$

$$I_{L2}(t) = I_{L2}(t_4) - \frac{V_{C4} - V_{\mathrm{in}}}{L_2} \cdot (t - t_4) \tag{17}$$

$$I_{L_{\mathrm{a1}}}(t) = I_{L_{\mathrm{a1}}}(t_4) + \frac{V_{C2} - V_{C1}}{L_{\mathrm{a1}}} \cdot (t - t_4) \tag{18}$$

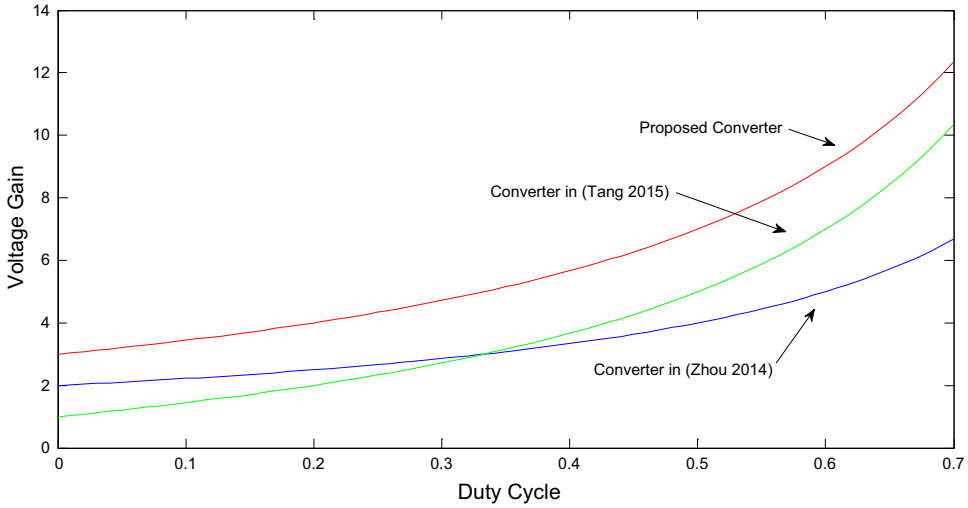


Fig. 3 The comparison of the voltage gain of the proposed converter with other converters

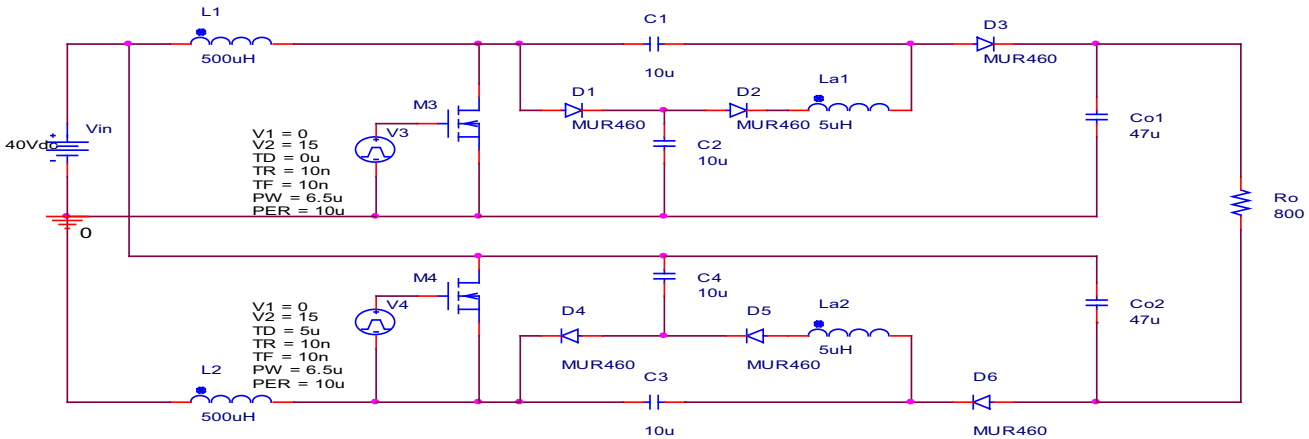


Fig. 4 Scheme of the experimental sample for the proposed converter in OrCAD software

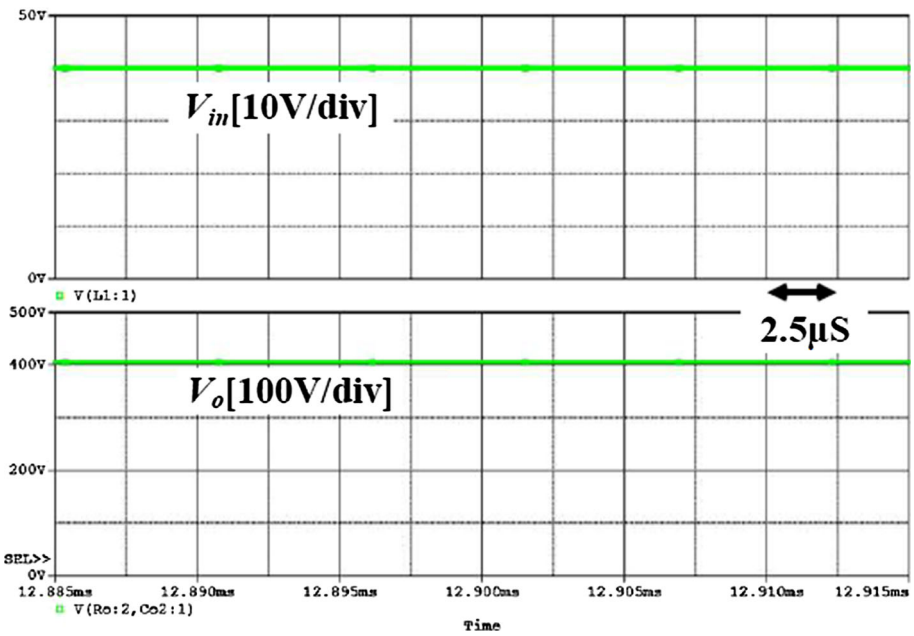


Fig. 5 Input and output voltage waveforms in the simulated converter

$$I_{L_{a2}}(t) = I_{L_{a2}}(t_4) - \frac{V_{C3}}{L_{a2}} \cdot (t - t_4) \tag{19}$$

2.1.6 Interval 6: t_5–t_6

This stage of the converter operation begins when diode D_5 is switched off. In this phase of the converter operation in the upper branch, switch S_1 is on, and the current of the inductor L_1 increases linearly on the path V_{in}–L_1–S_1. The current of the inductor L_{a1} also linearly increases on the path C_2–D_2–L_{a1}–C_1–S_1. Thus, the capacitor C_1 will be charged. In the lower branch, a part of the inductor L_2 charges the capacitor C_4 through V_{in}–C_4–D_4–L_2, while another part charges the output capacitor through V_{in}–C_{o2}–D_6–C_3–L_2. The current of the inductor L_2 decreases linearly with a slow slope. The main equations for the convertor elements are given as:

$$I_{L1}(t) = I_{L1}(t_5) + \frac{V_{in}}{L_1} \cdot (t - t_5) \tag{20}$$

$$I_{L2}(t) = I_{L2}(t_5) - \frac{V_{C4} - V_{in}}{L_2} \cdot (t - t_5) \tag{21}$$

$$I_{L_{a1}}(t) = I_{L_{a1}}(t_5) + \frac{V_{C2} - V_{C1}}{L_{a1}} \cdot (t - t_5) \tag{22}$$

Upon the completion of Step 6, the converter accomplishes a full switching cycle, and the mentioned six steps are repeated, subsequently.

2.2 Boundary Operation Between CCM and DCM

If the proposed converter is operated in boundary condition, the minimum value of the inductor currents at CCM condition reaches zero. For inductor L_2, the minimum value of current is:

$$\begin{aligned}(i_{L_2})_{min} &= (i_{L_2})_{av} - \frac{\Delta i_{L_2}}{2} = \frac{I_{in}}{2} - \frac{\Delta i_{L_2}}{2} \\ &= \frac{(3+D)I_o}{2(1+D)} - \frac{V_{in}D}{2f(L_2)_{min}} = 0.\end{aligned} \tag{23}$$

Therefore, the minimum value of inductor that the converter is operated in CCM condition is given as:

$$(L_2)_{min} = (L_1)_{min} = \frac{D(1-D)V_{in}}{(3+D)I_o f}. \tag{24}$$

2.3 DCM Operation

In this condition, the inductor current i_{L2} is increased in interval 0 to DT and decreased in interval DT to D_1T. This current reached zero at $(D + D_1)T$. The average value of i_{L2} is computed as:

$$(i_{L_2})_{av} = \frac{(D+D_1)\Delta i_{L_2}}{2} = \frac{(D+D_1)V_{in}D}{2fL_2} = \frac{I_{in}}{2} = \frac{V_o^2}{2RV_{in}}. \tag{25}$$

Therefore, D_1 is derived as follows:

$$D_1 = \frac{L_2 V_o^2 f}{R V_{in}^2 D} - D. \tag{26}$$

By using the volt-second balance principle on L_{a2}, the following equation can be obtained:

$$V_o = \frac{2 + 2D + D_1}{D_1} \tag{27}$$

Substituting (26) into (27), the voltage gain is derived as:

$$\frac{V_o}{V_{in}} = \frac{3}{2} + \sqrt{1 + \frac{4D^2R}{fL_2}}. \tag{28}$$

3 Design Considerations

The voltage values of the capacitors C_1, C_2, C_3, C_4, C_{o1}, and C_{o2} are obtained from the volt-sec balance equations for the inductors L_1 and L_2. The voltage equations for these capacitors are given as follows:

Voltage gain of the DC–DC converter

$$V_{C1} = V_{C2} = V_{C3} = V_{C4} = \frac{V_{in}}{1-D} \tag{29}$$

$$V_{Co1} = V_{Co2} = \frac{2.V_{in}}{1-D}. \tag{30}$$

By applying the KVL law in the cycle V_{in}–V_{Co1}–V_o–V_{Co2}, the following equation could be obtained:

$$V_0 = V_{Co1} + V_{Co2} - V_{in}. \tag{31}$$

Replacing V_{Co1} and V_{Co2} from (30) in (31), and simplifying it, gives

$$G = \frac{V_o}{V_{in}} = \frac{3+D}{1-D}. \tag{32}$$

Considering the converter operation values at the concerned intervals in the previous section and the capacitor voltage equations, the following relations for the voltage stresses across each of the switches could be obtained:

$$\overline{V_{S1}} = \overline{V_{S2}} = \frac{V_{in}}{1-D} = \frac{V_o}{3+D}. \tag{33}$$

The voltage stresses across each of the diodes are also calculated as:

$$\overline{V_{D1}} = \overline{V_{D2}} = \overline{V_{D3}} = \overline{V_{D4}} = \frac{V_{in}}{1-D} = \frac{V_o}{3+D}. \tag{34}$$

Figure 3 shows the comparison of the voltage gain of the proposed converter with other converters. As shown in this figure, the converter's voltage gain is higher than that of the similar converters (Table 1).

The converter's switches and diodes are selected in accordance with the converter's power level and their voltage stress equations. The converter's inductors for the concerned current ripples could be calculated from the following equation:

$$L_1 = L_2 = \frac{V_{in}.D.T_{sw}}{\Delta I_L}. \tag{35}$$

To obtain the design equations of the converter's capacitors, the input power equation is considered as:

$$P_{in} = P_o. \tag{36}$$

Given the gain equation of the converter, the following equation could be employed to replace the input voltage in the above equation.

$$P_{\text{in}} = V_{\text{in}} \cdot I_{\text{inavg}}. \tag{37}$$

Thus, we have:

$$I_{inavg} = \frac{(3+D).P_o}{(1-D).V_o}. \tag{38}$$

The average current in each inductor is equal to the corresponding one in the others. Or

$$I_{L1avg} = I_{L2avg} = \frac{I_{inavg}}{2}. \tag{39}$$

When the switch S_1 is off within a period of $(1-D)T_{\text{sw}}$, an average current of $I_{\text{inavg}}/2$ passes through the capacitor C_2. According to the capacitor's voltage load equation, the capacitor C_2 for the voltage variation of ΔVC_2 over the given interval could be calculated as:

$$C_2 = \frac{I_{\text{inavg}} \cdot (1-D) \cdot T_{sw}}{(3+D) \cdot \Delta V_{C2}}. \tag{40}$$

Similarly, the design equations of the capacitors C_1, C_3, and C_4 are given as:

$$C_1 = \frac{I_{\text{inavg}} \cdot (1-D) \cdot T_{\text{sw}}}{(3+D) \cdot \Delta V_{C1}} \tag{41}$$

$$C_3 = \frac{I_{\text{inavg}} \cdot (1-D) \cdot T_{\text{sw}}}{(3+D) \cdot \Delta V_{C3}} \tag{42}$$

$$C_4 = \frac{I_{\text{inavg}} \cdot (1-D) \cdot T_{\text{sw}}}{(3+D) \cdot \Delta V_{\text{Co1}}}. \tag{43}$$

The output capacitors C_{o1} and C_{o2} in a switching cycle must supply the output load current over the period $(\text{D}) \cdot T_{\text{sw}}$. Since the output capacitors are in series, each capacitor value for a voltage variation of ΔV_{o} over a given interval could be obtained as:

$$C_{o1} = C_{o2} = 2 \cdot \frac{P_{\text{o}} \cdot (D) \cdot T_{\text{sw}}}{V_{\text{o}} \cdot \Delta V_{\text{Co}}}. \tag{44}$$

To design the inductors L_{a1} and L_{a2}, it should be noted that when the switch S_1 is on, an approximate voltage of $00.5(\Delta \text{VC}_1 + \Delta \text{VC}_2)$ is created at the two terminals of the inductor L_{a1} that increases the current. If the inductor's increased current value is considered as ΔIL_{a1}, the inductor's value could be calculated as:

$$L_{\text{a1}} = \frac{\Delta V_{C1} + \Delta V_{C2}) \cdot D \cdot T}{2.\Delta I_{L_{\text{a1}}}}. \tag{45}$$

According to the above equation, an appropriate inductor value could be obtained by considering a small current variation in the inductor to prevent a significant increase in the switch stress. It is worth noting that the inductor value is generally in micro-Henry and small due to the small voltage applied to this inductor. Hence, this

Table 1 Comparison of the proposed and boost converters with other similar converters

	Boost converter	Converter in Zhou et al. (2014)	Converter in Yang et al. (2009)	Converter in Tang and Fu (2015)	Converter in Ganesan and Prabhakar (2014)	Proposed converter
Gain	$\frac{1}{1-D}$	$\frac{2}{1-D}$	$\frac{2}{1-D}$	$\frac{1+3D}{1-D}$	$\frac{2}{1-D}$	$\frac{3+D}{1-D}$
Voltage stress of switches	V_{o}	$\frac{V_{\text{o}}}{2}$	$\frac{V_{\text{o}}}{2}$	$\frac{V_{\text{o}}+V_{\text{in}}}{2}$	$\frac{V_O}{1-D}$	$\frac{V_O+V_{in}}{2}$
Voltage stress of diodes	V_{o}	Two $\frac{V_{\text{o}}}{2}$ diodes and two V_{o} diodes	Two $\frac{V_{\text{o}}}{2}$ diodes and two V_{o} diodes	Three V_{in} diodes and four $\frac{V_O-V_{in}}{4}$ diodes	$\frac{V_O}{1-D}$	$\frac{V_{\text{o}}}{3+D}$
Number of capacitors	1	4	2	1	2	6
Number of diodes	1	4	2	7	2	4
Number of inductors	1	2	2	4	2	4

inductor could not significantly increase the circuit volume. The value of the inductor L_{a2} is determined similar to that mentioned for the inductor L_{a1}.

4 Simulation Result

To evaluate the efficiency of the proposed converter and verify its accuracy, it is simulated with the OrCAD software. The converter is designed and simulated for 40 V input voltage, 400 V output voltage, 200 W power level, and 100 kHz frequency. The size and type of the selected components are reported in Table 2. Figure 4 illustrates the scheme of the proposed converter in the OrCAD software.

Figure 5 shows the input and output voltages obtained from the simulation. As shown in Fig. 5, the proposed converter is well managed to convert the 40 V input voltage to the 400 V output voltage. Figure 6 presents the waveforms of the inductors L_1 and L_2 and the input current I_{in}. Accordingly, the inductors L_1 and L_2 operate in a continuous conduction mode (CCM). Moreover, the input current ripple is considerably smaller than the corresponding ones obtained for inductors L_1 and L_2.

Table 2 The size and type of the selected components

Parameter	Description
Switching frequency	100 kHz
Switches	640 IRF
Diodes	460 MUR
Input inductors	500 Hμ
inductors L_{a1}, L_{a2}	5 Hμ
Capacitors C_1, C_2, C_3, and C_4	10 Fμ
C_{o1} and C_{o2} Capacitors	47 Fμ

5 Experimental Result

The experimental results of the proposed converter are presented in this section. It could be seen that the converter works appropriately in the simulator environment. Therefore, in order to evaluate the feasibility of the proposed converter, its laboratory sample is constructed. The elements similar to the simulated converter are utilized to construct the convertor. Moreover, a 200 W sample converter with 100 kHz switching frequency is prepared in the laboratory to convert the 40 V input voltage to the 400 V output voltage. Figure 7 shows the input and output voltages of the converter. Based on this figure, the converter is designed for about 67% duty factor. Thus, a high gain could be generated by the sample converter.

The current and voltage waveforms of switch S_1in the sample converters are shown in Fig. 8. As could be seen from Fig. 8, the switches' voltages are 120 V, which are considerably smaller than the 400 V output voltage. Furthermore, this figure illustrates that the switch voltage is limited when the switch is off, and there is no significant voltage fluctuation at its terminals. The voltage waveform and the current of the switch S_2 in the simulated converter are similar to the corresponding ones shown in Fig. 9, with

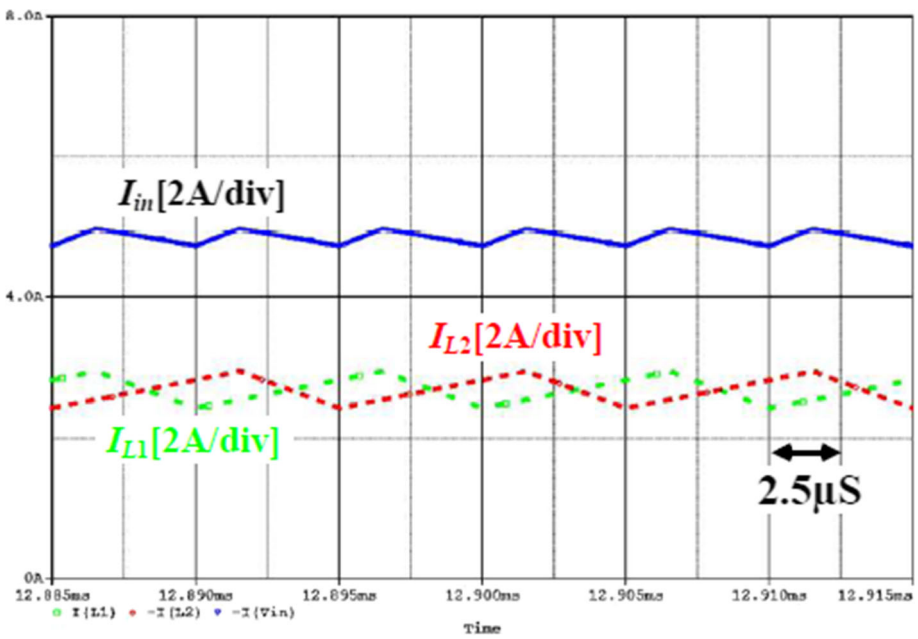


Fig. 6 Waveforms of IL_1, IL_2, and I_{in} in the simulated converter

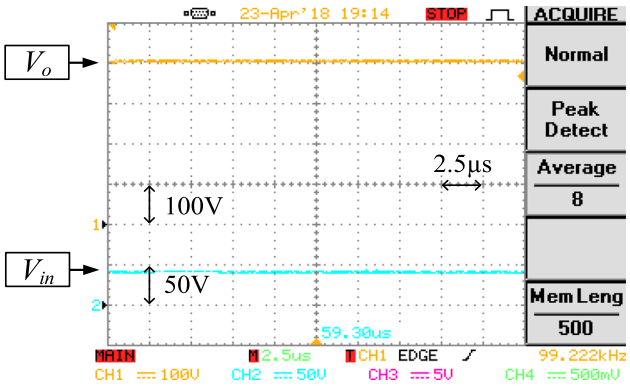


Fig. 7 Input and output voltage waveforms of the sample converter

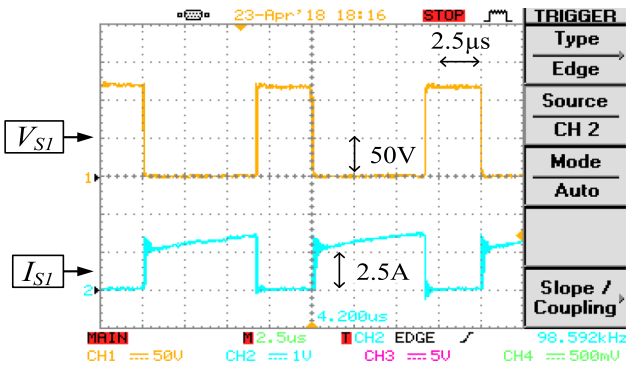


Fig. 8 Current and voltage waveforms in a switch of the sample converter

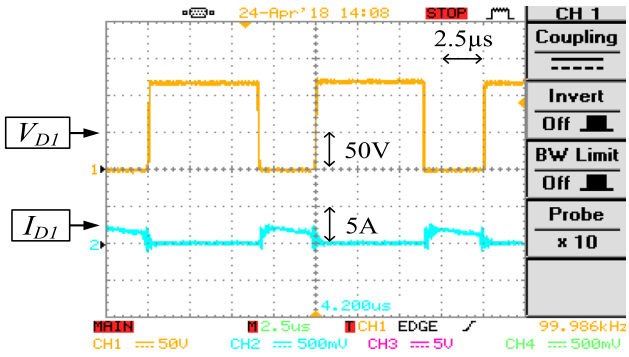


Fig. 9 Current and voltage waveforms in diode D_1 of the sample converter

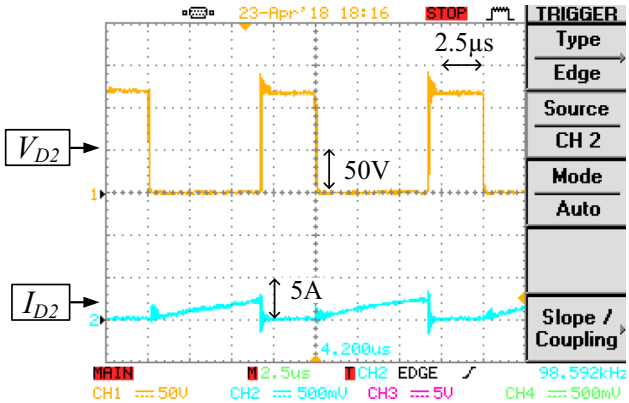


Fig. 10 Current and voltage waveforms in diode D_2 of the sample converter

only 180° phase shift. The voltage stress of switch S_2 is also 120 V.

Figures 10 and 11show the current and voltage waveforms of diodes D_2 and D_3 in the sample converter, respectively. Accordingly, it could be seen that the diodes' voltages stress is 120 V that is significantly smaller than the output voltage. In addition, the reverse recovery current in the diodes is negligible. This means that high-speed low-voltage diodes could be employed for these diodes to reduce the converter's losses.

The current and voltage waveforms of the diodes D_4 to D_6 are also shown in Figs. 9 and 10. The voltage stresses of these diodes are also about 120 V. Thus, high-speed low-voltage diodes are utilized.

The efficiency of the proposed converter in different loads is calculated in simulation. Figure 12 shows the comparison of efficiency between the proposed converter and converter in Zhou et al. (2014). As shown in this figure, the efficiency of the proposed converter is improved because the voltage stress of switches and diodes is very lower than converter in Zhou et al. (2014) and the conduction loss is reduced. In addition, the diodes of the

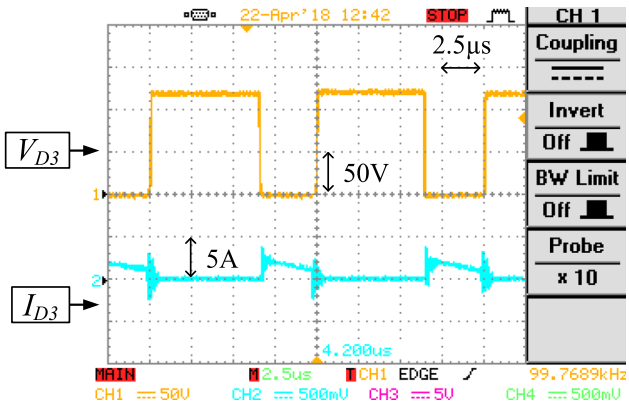


Fig. 11 Current and voltage waveforms in diode D_3 of the sample converter

proposed converter turn off under ZCS condition and the switching loss is reduced. Figure 13 shows the pie chart of component losses in the proposed converter for a 200(W) load. Figure 14 shows the image of implemented setup.

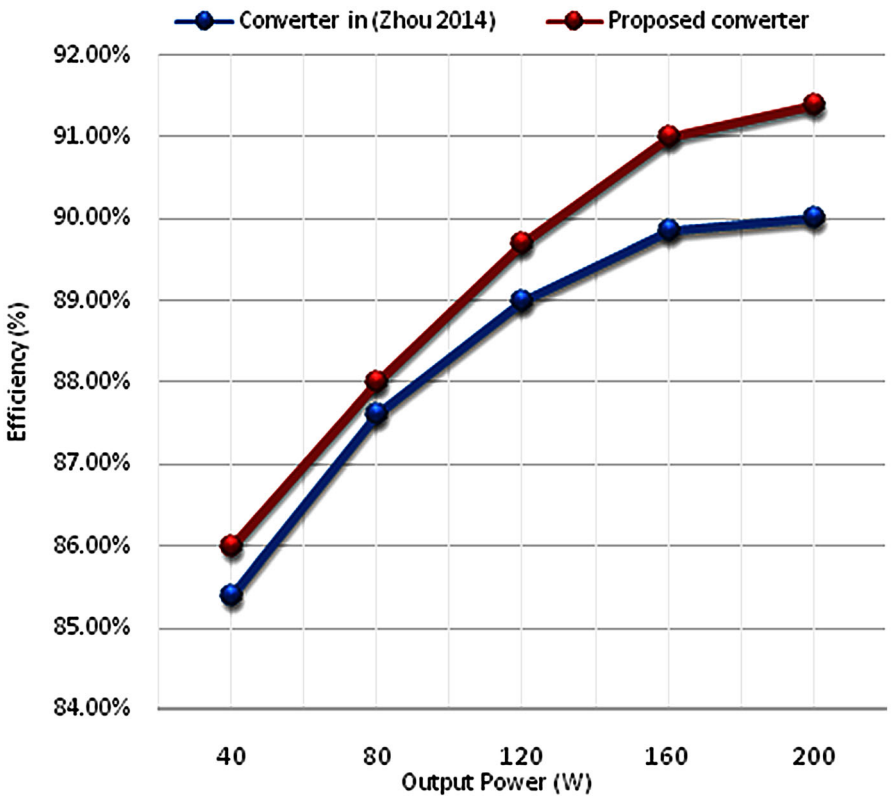


Fig. 12 Comparison of efficiency between the proposed converter and converter in Zhou et al. (2014)

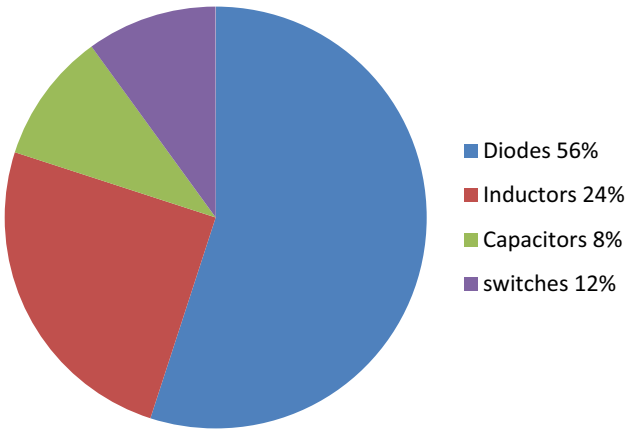


Fig. 13 The pie chart of component losses

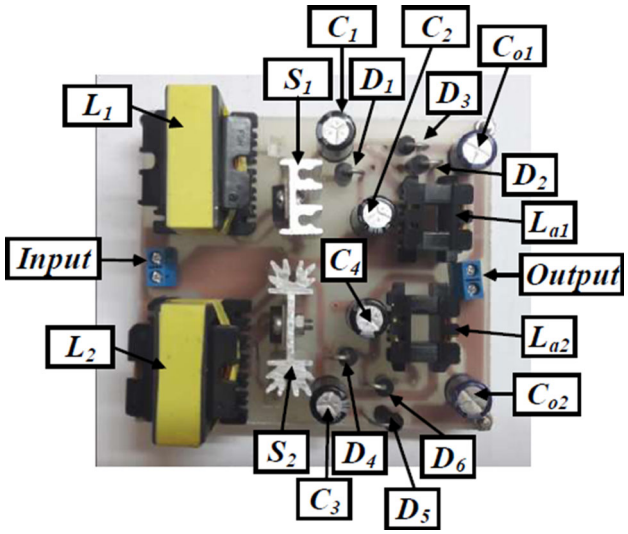
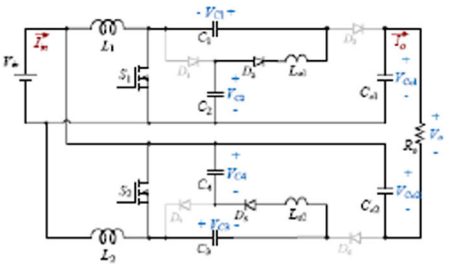


Fig. 14 The image of implemented setup

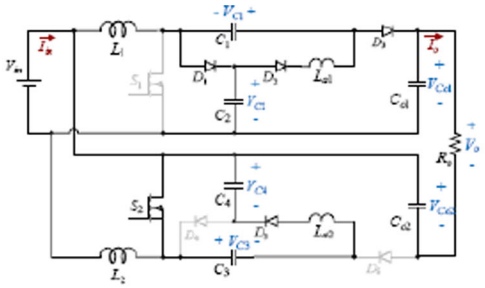
6 Conclusion

This paper introduced the proposed converter and describes its operation in detail. After describing its theoretical analysis, the simulation results and construction phases of the proposed converter are also provided. The efficiency of the proposed converter is improved by about 1.5% compared with the converter in Yang et al. (2009). Furthermore, the proposed converter can be implemented via elements with less voltage tolerance levels. Table 1 compares the proposed converter with the converters presented in Chang et al. (2017) and Zhou et al. (2014), which are interleaved boost converters with switched capacitors. According to the results, higher efficiency can be obtained with the converter proposed in this study. Based on the analysis, the simulation results, and the sample converter, the proposed converter can be employed in highly boosting applications with an average power level. Since the planar inductors are employed instead of the coupled inductors in the proposed converter, a superior power density can be attained.

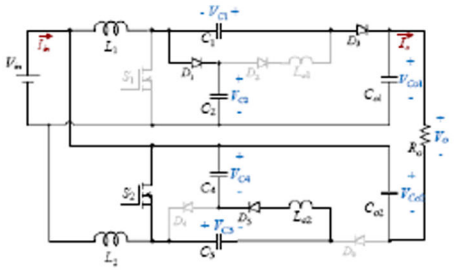
Appendix



Interval I



Interval II



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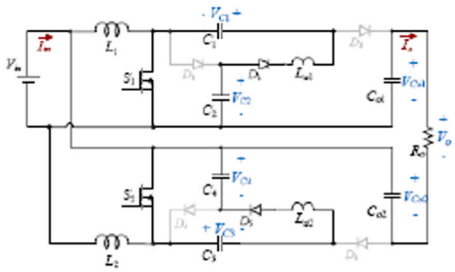
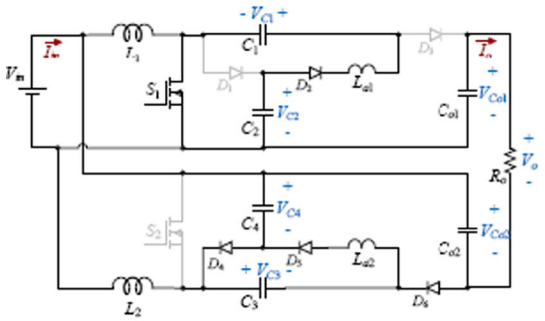
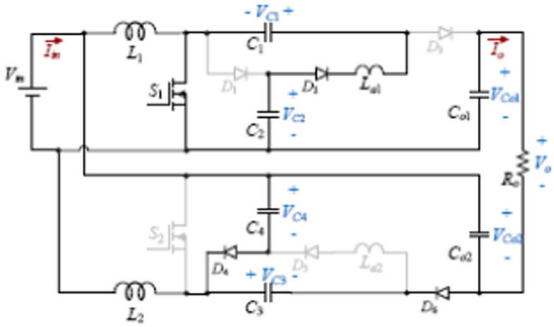


Interval IV



Interval V



Interval VI

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