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RESEARCH PAPER

Novel Memristor Emulators using Fully Balanced VDBA and Grounded Capacitor

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Abstract
In this paper, grounded and floating decremental/incremental memristor emulator circuits are realized using fully balanced voltage differencing buffered amplifier (FB-VDBA) and grounded capacitor. These proposed configurations are simpler in design as compared to most of the designs available in the literature. The pinched Hysteresis loops are maintained up to 1 MHz frequency. The decremental to incremental memristor emulator and vice versa can be easily attained by slightly modifying the circuits. Proposed designs of memristor emulator circuits are simulated using TSMC 0.18 μm CMOS process technology parameters of Mentor Graphics Eldo tool. The proposed decremental floating memristor emulator circuit has been embedded in the design of universal biquad filter to evaluate its performance.

Keywords Memristor · Emulator · VDBA · Filter · Fully balanced voltage differencing buffered amplifier

1 Introduction

Resistor, capacitor and inductor are the three well-known fundamental elements of electrical circuits. Each element offers a relation between any two of the four circuit variables namely voltage, current, charge and flux. Resistor provides relationship between voltage and current, whereas capacitor and inductor relate charge to voltage and flux to current, respectively. There was no element that can provide relationship between charge and flux. Professor Leon Chua postulated the fourth fundamental circuit element namely memristor (short for memory and resistor) that relates flux and charge (Chua 1971). Memristor offers unique properties that cannot be offered by any of the three fundamental elements or by combinations of these elements. Despite of its unique properties, researchers and engineers were not very interested to use memristor because of its unavailability in the market as off-the-shelf component. Researchers of Hewlett Packard lab published a paper announcing the physical realization of the memristor (Strukov et al. 2008). This paper has drawn significant attention of researchers and also motivated them to work upon memristors. Memristor is still not commercially available in the device form which opens a new area of research to design memristor emulator circuits. Researchers have recently started working on memristor emulator circuits and a lot of research is going on in this direction. Various emulator circuits which mimic the properties of memristors are being reported using modern active analog building blocks such as second-generation current conveyors (CCIIs), current feedback operational amplifiers (CFOAs), differential difference current conveyor (DDCC), operational transconductance amplifier (OTA), current conveyor transconductance amplifier (CCTA), differential voltage current conveyor transconductance amplifier (DVCCTA), current backward transconductance amplifier (CBTA), voltage differencing current conveyor (VDCC), voltage differencing transconductance amplifier (VDTA), current differencing buffered amplifier (CDBA), current differencing transconductance amplifier (CDTA) and, etc. A memristor emulator circuit was realized using four CCIIs, one multiplier and six passive components

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(Lopez et al. 2013). Another realization of floating memristor emulator circuit was reported in which four CCIIs, one op-amp, one multiplier, and eight passive components have been used (Yu et al. 2014). The incremental/decremental memristor emulator circuits using one active building block namely DDCC, three passive components and one additional multiplier have been realized in (Yesil et al. 2014). Different values of resistors and capacitors are given for different range of frequencies of operation of memristor emulator circuits. Afterward, memristor emulator circuit has been realized using three CCIIs, five passive components and one multiplier (Kumngern 2015). Another current-controlled memristor emulator circuit was reported using two CCIIs, three passive components and two transistors (Alharbi et al. 2015). Next, grounded memristor emulator circuit using two active building blocks namely CFOAs and OTA with five passive components was reported in (Abuelma'atti and Khalifa 2015). The reported memristor emulator was embedded in the design of multivibrator circuit to verify its performance. A grounded memristor emulator circuit was reported using two CCIIs, three passive components and one multiplier (Lopez et al. 2015). Subsequently, grounded memristor emulator circuit was reported using six OTAs, three passive components and one multiplier (Kumngern and Moungnoul 2015). A simple memristor emulator circuit was realized using single CCII, three passive components and one amplifier (Alharbi et al. 2015). The amplifier was used to obtain the nonlinear behavior for the formation of pinched Hysteresis loop. A floating memristor emulator circuit employing four CFOAs and five passive components was reported in (Abuelma'atti and Khalifa 2016) and was also used in the realization of FM demodulator. Next, memristor emulator circuit using seven active building blocks (four CCIIs and three OTAs) and six passive components was reported in which the transconductance is adjusted after changing the bias voltage of one of the OTA in order to change the memristance (Sozen and Cam 2016). Another floating memristor emulator circuit of high memristance value was reported in which the subthreshold region of operation was utilized to implement the tunable resistor (Babacan and Kacar 2017). A fractional-order memristor emulator circuit was designed using two CCIIs + , three passive components and one multiplier (Rashad et al. 2017). Next, the charge-controlled memristor emulator circuit was reported in Ranjan et al. (2017) that uses one CCTA and five passive components. Incremental and decremental memristor emulator circuits for high frequency were reported in which one DVCCTA and four passive components have been used (Ranjan et al. 2017). Afterward, another incremental/decremental memristor emulator circuits using a CBTA, three passive components and a multiplier were reported in (Ayten et al. 2017). The output terminals of CBTA have been interchanged to convert incremental memristor emulator circuit into decremental memristors emulator (Babacan et al. 2017). Memristor emulator circuits utilizing two CCIIs, four passive components and a multiplier have been reported in (Cam and Sedef 2017). Both, incremental and decremental memristor emulator circuits, were presented. A memristor emulator circuit was presented using VDTA, three passive components and a multiplier (Petrovic 2018). Floating memristor emulator circuit with hard-switching behavior was reported using multiple-output OTA and a capacitor in (Yesil 2019). A MOSFET-C-based grounded memristor emulator circuit was reported in which seven MOSFETs and one capacitor have been used (Yesil 2018). A memristor emulator circuit was reported in (Ranjan et al. 2018) employing four multiple-output OTAs, three resistors and a capacitor. Subsequently, high-frequency memristor emulator circuits have been reported using two OTAs and a capacitor (Kanyal et al. 2018). A VDCC-based memristor emulator circuit was realized in (Yesil et al. 2019) that uses one VDCC, two PMOS (used as a tunable resistor) and one capacitor. A memristor emulator circuit was reported in (Yesil et al. 2019) that utilizes VDTA and one MOS capacitor. A floating-gate MOSFET (FGMOS)-based memristor emulator circuit has been reported that uses three FGMOS and a capacitor (Vista and Ranjan 2019). Grounded and floating configurations of memristor emulator circuits using OTA, CDBA and grounded capacitor are reported in (Yadav et al. 2020). Recently, memristor emulator circuits using two active building blocks (CDTA and OTA) with a grounded capacitor are reported in (Gupta and Rai 2020).

Memristors are now being used in variety of applications such as adaptive filtering (Driscoll et al. 2010; Chew and Li 2012), computation of Boolean functions (Lehtonen et al. 2010), cellular neural networks (Itoh and Chua 2019), chaotic circuit (Muthuswamy and Chua 2010; Muthuswamy 2010; Ngouonkadi et al. 2014), computation of basic arithmetic operations (Merrikh-Bayat and Shouraki 2010), data storage neuromorphic applications (Kim et al. 2012), fractional-order circuits (Petras 2010), image processing (Hu et al. 2012), logic gate implementation (Borghetti et al. 2010; Kvatinsky et al. 2011), memristive neural networks (Pershin and Di Ventra 2010; Pérez-Carrasco et al. 2010), multilevel memory (Kim et al. 2010), non-volatile memory (Yang et al. 2008; Pickett et al. 2009; Robinett et al. 2010), phase shift oscillator (Talukdar et al. 2012; Talukdar et al. 2011), programmable analog circuits (Pershin and Di Ventra 2010; Shin et al. 2010), reactance-less oscillator (Zidan et al. 2014), temperature sensor (Wang et al. 2009), twin-T oscillator (Zhi-Jun and Yi-Cheng 2013), twin-T notch filter (Iu et al. 2011), variable gain amplifier (Wey and Jemison 2011), voltage controlled relaxation oscillator (Hussein and Fouda 2013; Anjanakumari et al. 2019), Wein

bridge oscillator (Talukdar et al. 2011) and Wheatstone bridge (Kim et al. 2015).

It has been observed that most of the designs of memristor emulator circuits reported in the literature use excess number of active and passive components and also use analog multiplier to obtain pinched Hysteresis loop of memristor. The range over which memristor emulator circuit works well is restricted to the frequency range of KHz in most of the designs. Therefore, objective of the paper is to design grounded and floating decremental/incremental memristor emulator circuits using less number of active and passive components that can perform satisfactorily in the frequency range of MHz. In this paper, memristor emulator circuits are proposed using one fully balanced VDBA and a grounded capacitor. Decremental memristor emulator circuits have easily been converted into incremental memristor emulator circuits and vice versa with slight modification in the circuit.

2 Fully Balanced Voltage Differencing Buffered Amplifier: Characteristics, Symbol and Circuit Diagram

The FB-VDBA is a six terminal block out of which two are input terminals, two are intermediate terminals and remaining two are output terminals as depicted in Fig. 1. Input voltages V_p and V_n are applied to terminals p and n. The transconductance amplifier converts these voltages into currents (I_{z+} and I_{z-}) at $z+$ and $z-$ terminals, respectively, as given in Eq. (1). The voltages V_{z+} and V_{z-} are obtained by connecting impedances Z_z to the $z+$ and $z-$ terminals of FB-VDBA as given in Eq. (2). The voltages V_{z+} and V_{z-} are copied by two inverted buffers to achieve two voltages V_{w-} and V_{w+} as given in Eq. (3). The transconductance (g_m) of conventional FB-VDBA is controlled by varying the bias current (I_B) as given in Eq. (4). The internal structure of voltage-tunable FB-VDBA as shown in Fig. 2 has been designed by replacing the bias current I_B of conventional FB-VDBA (Sotner et al. 2013) with structures of current mirror formed by MOSFETs

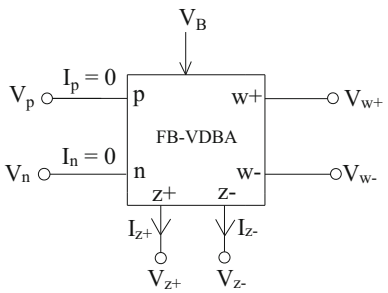

Fig. 1 Symbol of voltage-tunable FB-VDBA

M17-M19. The transconductance (G_m) of voltage-tunable FB-VDBA depends on voltage V_B as given in Eq. (5).

$$I_{z+} = g_m(V_p - V_n), I_{z-} = -g_m(V_p - V_n), \quad (1)$$

$$V_{z+} = I_{z+}.z_{z+}, V_{z-} = -I_{z-}.z_{z-} \quad (2)$$

$$V_{w-} = -V_{z+}, V_{w+} = -V_{z-} \quad (3)$$

$$g_m = \sqrt{2.\mu_n.C_{ox}.\frac{W}{L}}.\sqrt{I_B} \quad (4)$$

$$G_m = \frac{k}{\sqrt{2}}(V_B - V_{SS} - 2V_{th}) \quad (5)$$

where $k = \mu_n.C_{ox}$.

3 The Proposed Grounded and Floating Memristor Emulator Circuits

The realizations of grounded decremental/incremental and floating decremental/incremental memristor emulators are depicted in Fig. 3a, b, respectively. In Fig. 3a, when terminals "a" and "c" are connected to terminals "b" and "d", respectively, then, grounded decremental memristor emulator is obtained while grounded incremental configuration of memristor emulator is obtained from the same circuit when terminals "a" and "c" are connected to terminals "d" and "b", respectively. Similarly in Fig. 3b, floating decremental memristor emulator circuit is realized when terminals "a" and "c" are connected to terminals "b" and "d", respectively, while floating incremental memristor emulator circuit is obtained when terminals "a" and "c" are connected to terminals "d" and "b", respectively. In grounded decremental/incremental memristor emulator circuits, one of the input terminals of voltage-tunable FB-VDBA is kept at ground, whereas in the decremental/incremental floating memristor emulator circuits both terminals remain at different voltages (V_{in1} or V_{in2}). In all configurations of memristor emulator circuits, w−terminals are connected to V_B terminal. In floating memristor emulator circuits, one additional feedback path is provided between z_{2+} terminal to input terminal. The voltage V_{w-} follows the inverted voltage across capacitor (V_{z+} or V_{z1+}) connected to z_+ and z_{1+} terminals of voltage-tunable FB-VDBA in grounded and floating memristor emulator circuits, respectively. The voltage V_{w-} is connected to the bias voltage V_B which controls the input current (I_{in}). Therefore, voltage across capacitor (V_{z+} or V_{z1+}) controls the input current (I_{in}) and this current is used to control the voltage across capacitor. This process keeps repeating and forms a pinched hysteresis loop. The input current (I_{in}) gets affected by the last stored voltage across the capacitor. If the voltage across capacitor increases the current I_{in} in positive direction, the proposed configurations

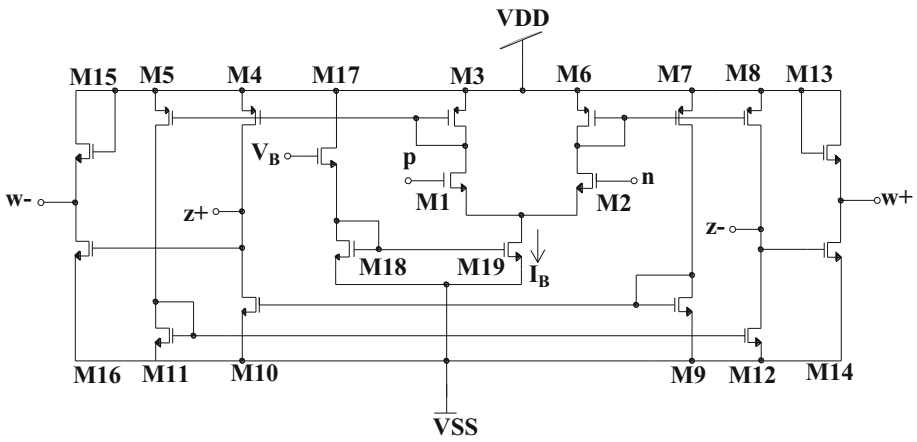

Fig. 2 Internal structure of voltage-tunable FB-VDBA

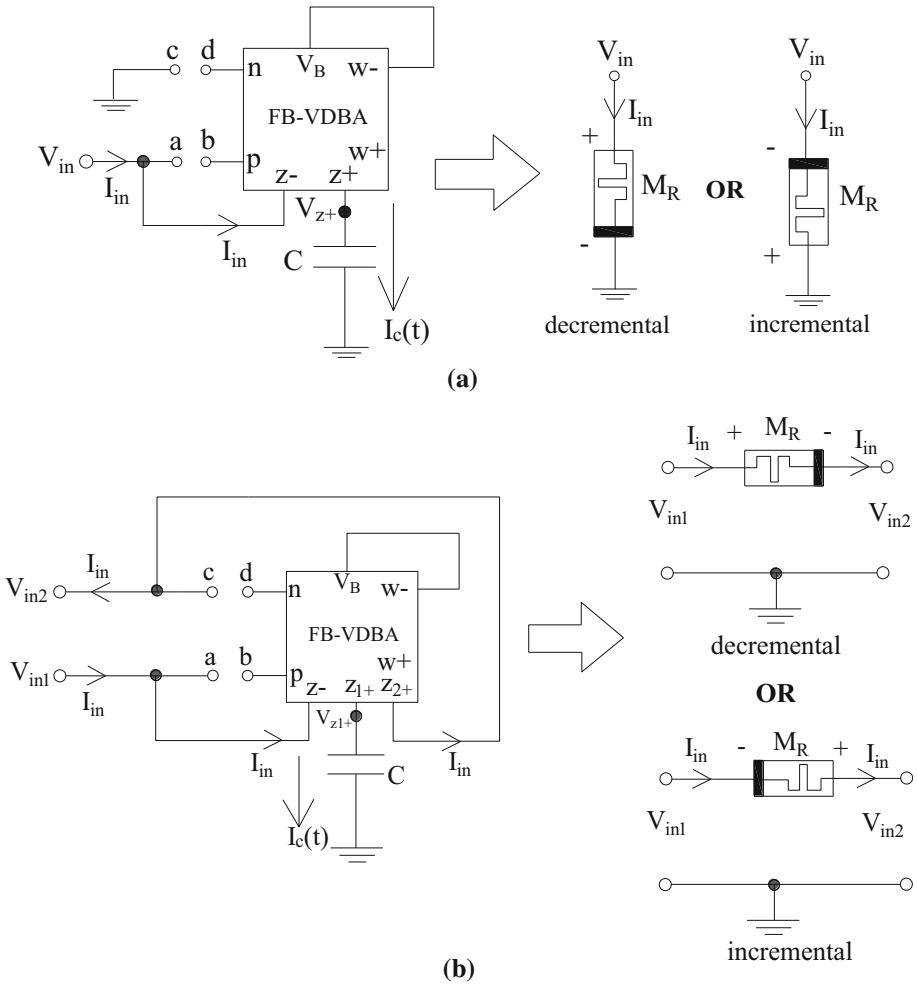

Fig. 3 Proposed decremental and incremental memristor emulators **a** grounded **b** floating

are called as incremental memristor emulator circuits, whereas if the voltage across capacitor increases the current (I_{in}) in negative direction, the proposed configurations are known as decremental memristors emulators.

The analysis of the circuit shown in Fig. 3a yields the equations as

$$I_{in} = I_{z-} = G_m V_{in} \tag{6}$$

$$I_c(t) = I_{z+} = G_m V_{in} \tag{7}$$

$$V_{w-} = -V_{z+} = V_B = -\frac{1}{C}\int I_c(t)\mathrm{d}t \tag{8}$$

With the help of Eqs. (7) and (8), we get

$$V_{w-} = V_B = -\frac{1}{C}\int G_m V_{in}(t)\mathrm{d}t = -\frac{G_m \varphi_{in}}{C} \tag{9}$$

where Φ_{in} is the total flux obtained in the proposed circuit of memristor emulator.

The flux (Φ_{in}) of proposed circuit of memristors emulator is given in Eq. (10).

$$\varphi_{in} = \int V_{in}(t)\mathrm{d}t \tag{10}$$

The transconductance (G_m) is obtained after solving Eqs. (5) and (9) as

$$G_m = -\frac{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})}{1 + \frac{k}{\sqrt{2}}\frac{\varphi_{in}}{C}} \tag{11}$$

The memristance M (Φ) is achieved after replacing the value of Eq. (11) into Eq. (6) as

$$M(\varphi) = \frac{V_{in}}{I_{in}} = \frac{1}{G_m} = -\frac{1}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})} - \frac{\varphi_{in}}{C(V_{ss} + 2V_{th})}$$
$$\leftarrow \text{Fixed part} \rightarrow \leftarrow \text{Variable part} \rightarrow \tag{12}$$

It is observed from Eq. (12) that the memristance has two parts fixed and variable. The variable part gets subtracted from the fixed part, and therefore, it represents the memristance of decremental grounded memristor emulator circuit. It depends on the amount of flux (ϕ_{in}) and value of capacitor. Similarly, the memristance of incremental memristor emulator circuit is represented by Eq. (13) in which variable part is added with the fixed part

$$M(\varphi) = \frac{V_{in}}{I_{in}} = \frac{1}{G_m} = -\frac{1}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})} + \frac{\varphi_{in}}{C(V_{ss} + 2V_{th})}$$
$$\leftarrow \text{Fixed part} \rightarrow \leftarrow \text{Variable part} \rightarrow \tag{13}$$

After applying sinusoidal signal $V_m \sin \omega t$ to the input terminal of grounded memristor emulator circuit, flux Φin is obtained as

$$\varphi_{in} = \frac{V_m}{\omega}\cos\left(\omega t - \frac{\pi}{2}\right) \tag{14}$$

where V_m is the amplitude of sinusoidal input signal and ω represents the frequency.

The value of flux Φin obtained from Eq. (14) is substituted into Eqs. (12) and (13) which leads to

$$M(\varphi) = \frac{V_{in}}{I_{in}} = -\frac{1}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})} \mp \frac{V_m \cos\left(\omega t - \frac{\pi}{2}\right)}{\omega C(V_{ss} + 2V_{th})}$$
$$\leftarrow \text{Fixed part} \rightarrow \leftarrow \text{Variable part} \rightarrow \tag{15}$$

From Eq. (15), it is clearly observed that the value of memreistance varies with change in amplitude and frequency for the applied signal of proposed decremental and incremental grounded memristor emulator circuits. It is also controlled by changing the value of capacitors. The derivation of memristance of floating decremental/incremental memristor emulator circuit remains same with only change in applied voltage ($V_{in1} - V_{in2}$) between input terminals of voltage-tunable FB-VDBA. The memristance M (Φ) of floating decremental/incremental memristor emulator circuits can be easily obtained directly from Eq. (15) and is given in Eq. (16).

$$M(\varphi) = \frac{V_{in2} - V_{in1}}{I_{in}} = \frac{1}{G_m} = -\frac{1}{\frac{k}{\sqrt{2}}(V_{ss} + 2V_{th})} \mp \frac{V_m \cos\left(\omega t - \frac{\pi}{2}\right)}{\omega C(V_{ss} + 2V_{th})}$$
$$\leftarrow \text{Fixed part} \rightarrow \leftarrow \text{Variable part} \rightarrow \tag{16}$$

The memristance of decremental and incremental floating memristor emulator circuits is also varied after changing the amplitude and frequency of applied sinusoidal signal.

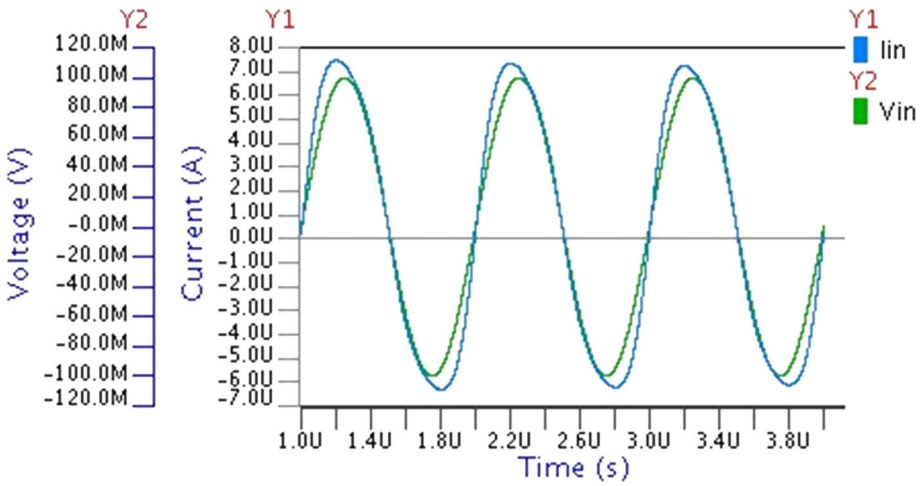

Fig. 4 Current–voltage response of decremental memristor emulator

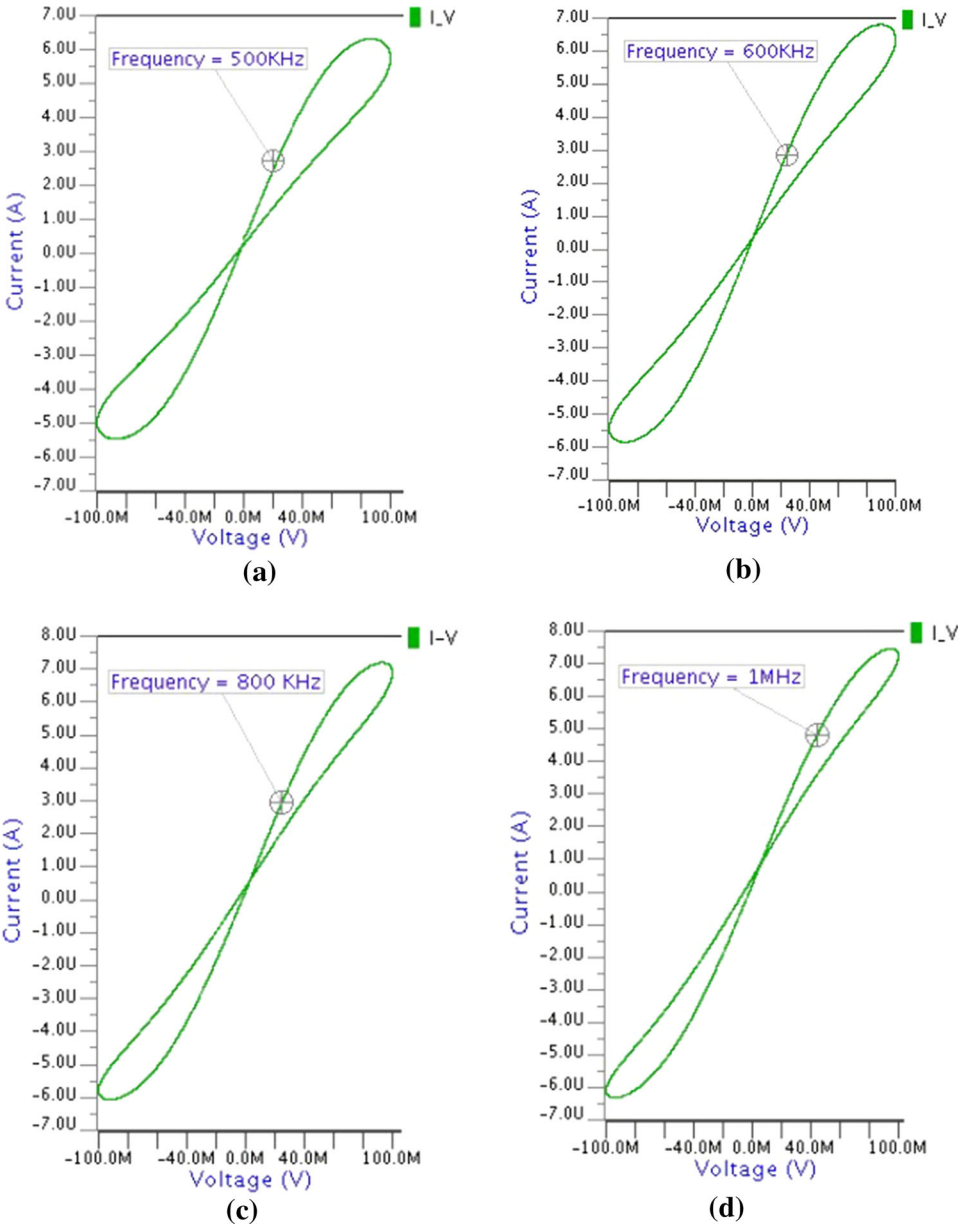

Fig. 5 Current–voltage pinched Hysteresis loops of grounded decremental emulator **a** 500 kHz **b** 600 kHz **c** 800 kHz **d** 1 MHz

4 Simulation Results and Discussions

The proposed decremental/incremental grounded and floating memristor emulator circuits are simulated using TSMC 0.18 µm CMOS process technology parameters of Mentor Graphics Eldo tool. The supply voltage is used as ± 0.9 V, whereas capacitor value is chosen as 40 pF. The aspect ratios of MOSFETs for the circuit diagram of voltage-tunable FB-VDBA are presented in Table 1.

Table 1 Aspect ratios (W/L) of MOSFETs for voltage-tunable FB-VDBA

MOSFETs	W(µm)	L(µm)
M1-M2	16	1
M3-M8	9	1
M9-M12	4	1
M13-M16	54	0.18
M17	15	0.18
M18-M19	14	0.18

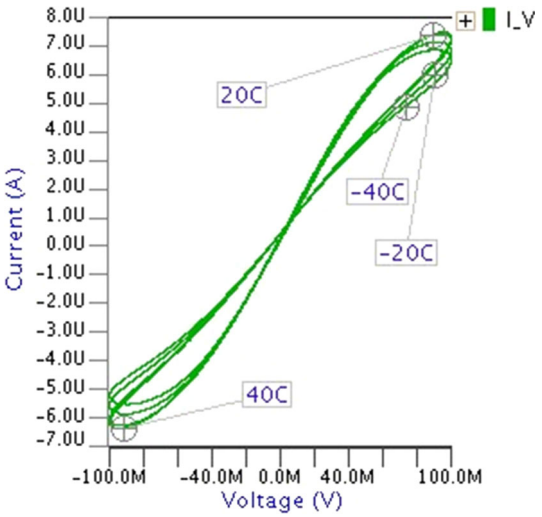

Fig. 6 Hysteresis loop for grounded decremental emulator at different temperatures

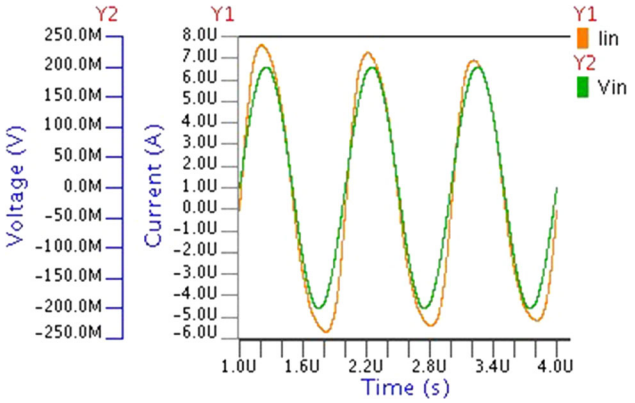

Fig. 7 Current–voltage response of decremental floating memristor emulator circuit

4.1 Decremental Grounded Memristor Emulator Circuit

The sinusoidal signal having amplitude of 100 mV and frequency of 1 MHz is applied to decremental emulator of Fig. 3. The current–voltage response with respect to time is shown in Fig. 4. To obtain the pinched Hysteresis loops, a periodic sinusoidal waveform (Vm = 100 mV) is applied to input terminal of decremental memristor emulator of Fig. 3. These loops are obtained for different frequencies of input sinusoidal signal as depicted in Fig. 5a–d. It is clearly observed that the decremental grounded memristor emulator circuit performs satisfactorily for the wide range of frequencies. It is also seen from Fig. 5a–d that the loops shrink for increase in frequency. The pinched loops of grounded decremental memristor emulator circuit are shown in Fig. 6 for variations in temperature. It is concluded from Fig. 6 that the Hysteresis loops shrink with increase in the temperature.

4.2 Decremental Floating Memristor Emulator Circuits

The sinusoidal signal having amplitude of 100 mV and frequency of 1 MHz is applied between terminals (V_{in1} and V_{in2}) of decremental memristor emulator of Fig. 4. Current–voltage response of proposed decremental floating memristor emulator circuit is shown in Fig. 7. The pinched loops of decremental floating memristor emulator circuit for different frequencies are shown in Fig. 8a–d. It is concluded from the figures that the pinched Hysteresis loop shrinks when frequency is increased within a suitable range. Figure 9 shows the pinched Hysteresis loops of decremental floating memristor emulator circuit when temperature is varied from − 40 to + 40 °C. It can be concluded from Fig. 9 that the Hysteresis loop of proposed decremental floating memristor emulator circuit is not deformed when temperature is varied from − 40 to +40 °C.

4.3 Behavior of Proposed Memristor Emulator Circuits at Lower Frequencies

The value of memristance depends on both the frequencies of operation and the values of capacitors used in the design of memristor emulator circuits as expressed in Eqs. (15) and (16). The memristance is inversely proportional to the product of angular frequency (ω) and the value of capacitor (C). To maintain the same Hysteresis loops (f = 1 MHz, C = 40 pF) for the lower frequencies, the values of capacitors are appropriately increased. The pinched Hysteresis loops of proposed grounded and floating decremental/incremental memristor emulator circuits are the same for frequencies of 10 Hz, 100 Hz, 1 kHz, 10 kHz and 100 kHz if the values of capacitors are chosen as 4μF, 0.4μF, 40 nF, 4 nF and 0.4 nF, respectively, as shown in Fig. 10a–d. In each case, the product of frequencies (f) and the values of capacitors (C) are the same as in the case of 1 MHz frequency with 40 pF capacitor. Thus, it is concluded that the proposed decremental/incremental memristor emulator circuits can work satisfactorily at lower frequencies with appropriate values of capacitors.

4.4 Monte Carlo Analysis of Proposed Memristor Emulator Circuits

The robustness of the proposed memristor emulator circuits has been checked by Monte Carlo analysis. Monte Carlo analysis is performed for 200 runs, and Gaussian random variations have been given for changing the device

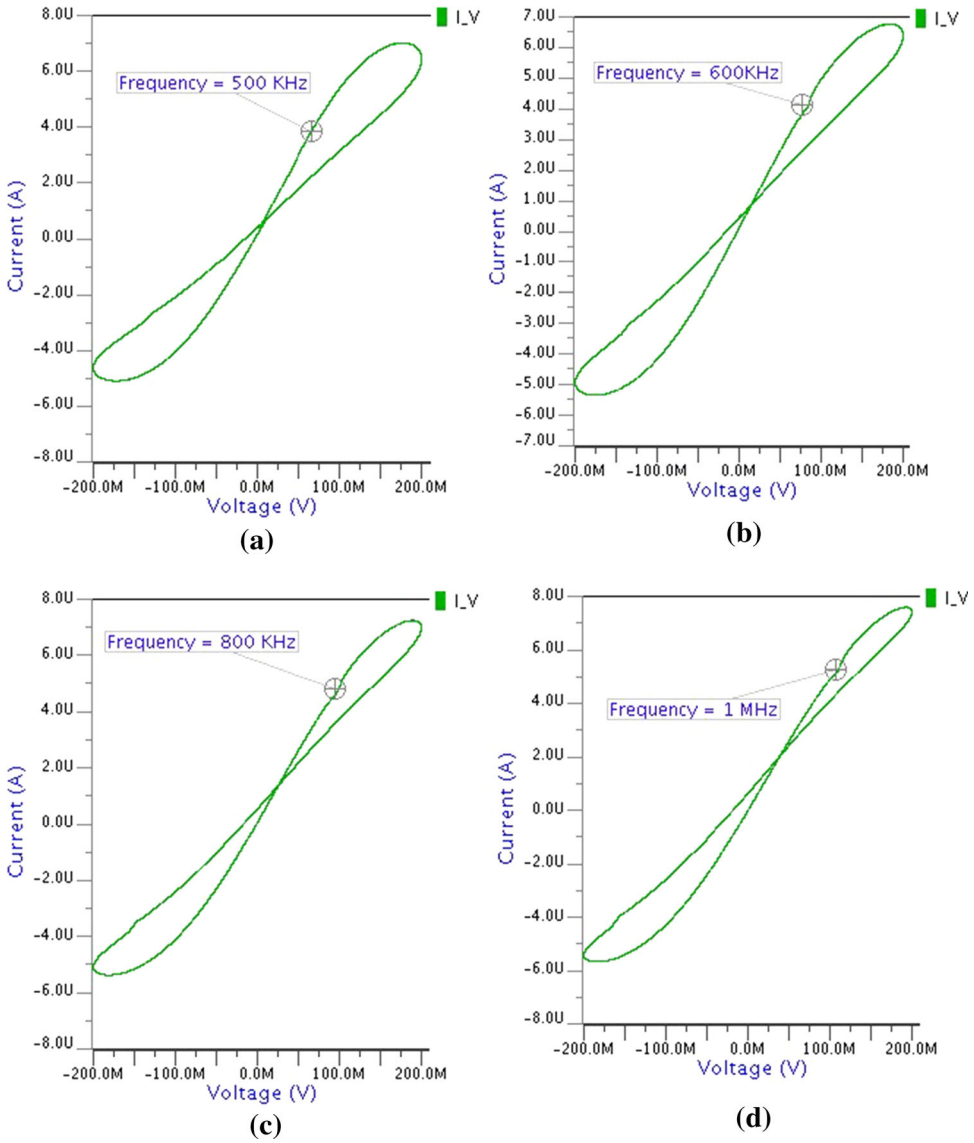

Fig. 8 Current–voltage pinched Hysteresis loops of proposed decremental floating memristor emulator **a** 500 kHz **b** 600 kHz **c** 800 kHz **d** 1 MHz

parameters such as threshold voltage, aspect ratios of MOSFETs and device parasitic capacitances. It is observed from Fig. 11 that the pinched Hysteresis curves of Monte Carlo analysis is conversed even after change in device parameters and therefore the designs of the proposed decremental and incremental memristor emulator circuits are robust.

4.5 Non-volatility Tests of Proposed Grounded Memristor Emulator Circuits

In order to verify the property of non-volatility, a voltage pulse of 1 MHz frequency has been applied to input terminals of proposed grounded decremental/incremental memristor emulator circuits. The obtained results of non-volatility tests are shown in Fig. 12a, b. It can be seen from Fig. 12a that memristance (M_R) decreases from 22 to 16 kΩ during "on" period of the first cycle of input pulse and it retains the value of memristance during "off" period. For the "on" period of second cycle, memristance decreases from 16 to 13 kΩ and retains its value of memristance during "off" period. In the next cycle, the process repeats in the same manner. Therefore, it is concluded that during "off" period of input pulse, memristor emulator circuit retains the previous value of memristance. Similarly, for the incremental grounded memristor emulator circuit, the memristance increases from 14 to 18 kΩ during "on" period of first cycle and holds its value of memristance during "off" period. During "on" period of second cycle, the value of memristance increases again from 18 to 22 kΩ and retains its value of memristance during "off" period Thus, it is concluded that proposed decremental and incremental memristor emulator circuits satisfy the property of non-volatility.

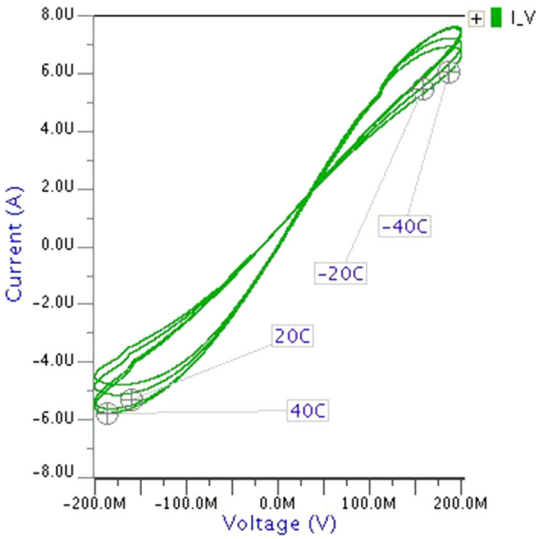

Fig. 9 Hysteresis loop for decremental floating memristor emulator circuit at different temperatures

5 Comparison of Proposed Memristor Emulator Circuits with Other Reported Memristor Emulator Circuits in the Literature

The proposed memristor emulator circuits have been compared with other memristor emulator circuits available in the literature as given in Table 2. The following advantages of proposed memristor emulator circuits have been observed.

(1) The memristor emulator circuits reported in (Lopez et al. 2013; Yu et al. 2014; Yesil et al. 2014; Kumngern 2015; Lopez et al. 2015; Kumngern and Moungnoul 2015; Alharbi et al. 2015; Ayten et al. 2017; Babacan et al. 2017; Cam and Sedef 2017; Petrovic 2018) use both analog multiplier as well as active and passive components that results in increased complexity, whereas the proposed memristor emulator only use single active and passive component that leads to simpler configurations.

(2) The frequency range over which memristor emulator works are in the range of hertz (Yu et al. 2014; Babacan and Kacar 2017; Cam and Sedef 2017) and kilohertz (Lopez et al. 2013; Kumngern 2015; Alharbi et al. 2015; Abuelma'atti and Khalifa 2015; Lopez et al. 2015; Kumngern and Moungnoul 2015; Alharbi et al. 2015; Abuelma'atti and Khalifa 2016; Sozen and Cam 2016; Babacan and Kacar 2017; Rashad et al. 2017; Ranjan et al. 2017; Ranjan et al. 2017; Ayten et al. 2017; Babacan et al. 2017; Ranjan et al. 2018; Kanyal et al. 2018), whereas proposed memristor emulator circuits work up to 1 MHz frequency.

(3) The reported memristor emulator circuits in (Lopez et al. 2013; Yu et al. 2014; Yesil et al. 2014; Kumngern 2015; Alharbi et al. 2015; Abuelma'atti and Khalifa 2015; Lopez et al. 2015; Kumngern and Moungnoul 2015; Alharbi et al. 2015; Abuelma'atti and Khalifa 2016; Sozen and Cam 2016; Rashad et al. 2017; Ranjan et al. 2017; Ayten et al. 2017; Babacan et al. 2017; Ranjan et al. 2018; Yadav et al. 2020; Gupta and Rai 2020) use excess number of passive components, whereas only one capacitor is used in proposed memristor emulators.

(4) Only grounded memristor emulator circuit was reported in (Alharbi et al. 2015; Abuelma'atti and Khalifa 2015; Lopez et al. 2015; Kumngern and Moungnoul 2015; Alharbi et al. 2015; Rashad et al. 2017; Ranjan et al. 2017; Ayten et al. 2017; Babacan et al. 2017; Ranjan et al. 2018), whereas both grounded and floating memristor emulator circuits are proposed in this paper.

(5) Memristor emulator circuits reported in (Lopez et al. 2013; Yu et al. 2014; Yesil et al. 2014; Kumngern 2015; Alharbi et al. 2015; Abuelma'atti and Khalifa 2015; Lopez et al. 2015; Kumngern and Moungnoul 2015; Alharbi et al. 2015; Abuelma'atti and Khalifa 2016; Sozen and Cam 2016; Rashad et al. 2017; Petrovic 2018; Ranjan et al. 2018) use resistor, whereas the proposed memristor emulator circuits are resistorless.

(6) Only one active building block is used in the realization of proposed memristor emulator circuits, whereas the memristor emulator circuits reported in (Lopez et al. 2013; Yu et al. 2014; Yesil et al. 2014; Kumngern 2015; Alharbi et al. 2015; Abuelma'atti and Khalifa 2015; Lopez et al. 2015; Kumngern and Moungnoul 2015; Alharbi et al. 2015; Abuelma'atti and Khalifa 2016; Sozen and Cam 2016; Babacan and Kacar 2017; Rashad et al. 2017; Babacan et al. 2017; Cam and Sedef 2017; Petrovic 2018; Yesil 2019; Ranjan et al. 2018; Kanyal et al. 2018) use more than one active building block.

Table 2 Comparison of proposed memristor emulators with existing memristor emulators in the literature

Reference	No. of components	No. of resistors and capacitors	Power supply (V)	Operating frequency	Floating (F) and grounded (G)
Lopez et al. (2013)	4 CCIIs, 1multiplier	5 and 1	±10	20 kHz	F
Yu et al. (2014)	4 CCIIs, 1op-Amp 1multiplier	10 and 1	±15	160 Hz	F
Yesil et al. (2014)	1DDCC, 1multiplier	2 and 1	±1.5	1 MHz	F
Kumngern (2015)	3ECCIIs, 1AD633	4 and 1	±10	5 kHz	F
Alharbi et al. (2015)	1 CCII, 2 diode-connected transistors	3 and 1	±12	10 kHz	G
Abuelma'atti and Khalifa (2015)	2CFOAs, 1OTA	3 and 2	±12	2 kHz	G
Lopez et al. (2015)	2CCIIs, 1multiplier	4 and 3	±10	270 kHz	G
Kumngern and Moungnoul (2015)	6OTA,1multiplier	2 and 1	±10	1.5 kHz	G
Alharbi et al. (2015)	1 CCII, 1AD633, 2 transistors PN3565, 1amplifier	5 and 1	±1	3 kHz	G
Abuelma'atti and Khalifa (2016)	4CFOAs, 2 diodes	5 and 4	±10	2.9 kHz	F
Sozen and Cam (2016)	4CCIIs, 3OTAs	5 and 1	±15	10 kHz	F
Babacan and Kacar (2017)	1OTA, 2PMOS	0 and 1	±1	30 Hz	F
Rashad et al. (2017)	2 CCIIs,1 multiplier, 1 fractional capacitor	0 and 3	±10	10 kHz	G
Ranjan et al. (2017)	1 CCTA	3 and 1	±1.5	10 MHz	Both
Ranjan et al. (2017)	1 DVCCTA	3 and 1	±1.25	1 MHz	G
Ayten et al. (2017)	1 CBTA, 1multiplier	2 and 1	±0.9	100 kHz	G
Babacan et al. (2017)	1 MO-OTA, 1multiplier	1 and 1	±5/1.2	10 kHz	G
Cam and Sedef (2017)	4 CCIIs, 1 multiplier	3 and 1	±10	120 Hz	F
Petrovic (2018)	1 VDTA, 1multiplier	2 and 1	±0.9	2 MHz	F
Yesil (2019)	1 MO-OTA	0 and 1	±0.9	1 MHz	F
Ranjan et al. (2018)	4 MO-OTA	3and 1	±2.5	500 kHz	G
Kanyal et al. (2018)	2 OTAs	0 and 1	±1.2	400 kHz/ 8 MHz	Both
Yadav et al. (2020)	1 CDBA, 1OTA	0 and 1	±0.9	1 MHz	Both
Gupta and Rai (2020)	1 CDTA, 1 OTA	0 and 1	±0.9	2 MHz	Both
Proposed work	**1 FB-VDBA**	**0 and 1**	**±0.9**	**1 MHz**	**Both**

6 Performance Analysis of Proposed Non-Ideal Decremental Grounded Memristor Emulator

In this section, non-ideal characteristics of FB-VDBA are presented first that is followed by the performance analysis of non-ideal grounded decremental memristor emulator circuit. In the non-ideal analysis, role of parasitic impedances become important because it affects the performance of the circuit over certain frequencies of operation.

6.1 Non-Ideal FB-VDBA

Non-ideal model of FB-VDBA (Khatib and Biolek 2013) including parasitic resistances and capacitances of different terminals is shown in Fig. 13. The parasitic resistances are represented by Rp, Rn, R_{z-}, R_{z+}, R_{w-} and R_{w+} at terminals p, n, z−, z + , w− and w +, respectively, whereas parasitic capacitances are shown by C_p, C_n, C_{z-} and C_{z+} at terminals p, n, z− and z + , respectively. Parasitic inductances are presented by Lw + and Lw- at terminals w + and w-, respectively. The parasitic resistances R_p, R_n, R_{z+} and R_{z-} appear in parallel with parasitic capacitances C_p, C_n, C_{z+} and C_{z-} at terminals p, n, z + and z−, respectively. The parasitic resistances R_{w+} and R_{w-} appear in series with parasitic inductances L_{w+} and L_{w-} at w + and w− terminals of FB-VDBA, respectively. In ideal case, transconductance (g_m) and gain (β) of FB-VDBA are assumed to be constant for all frequencies of operation whereas in the non-ideal case, transconductance (g_m) and

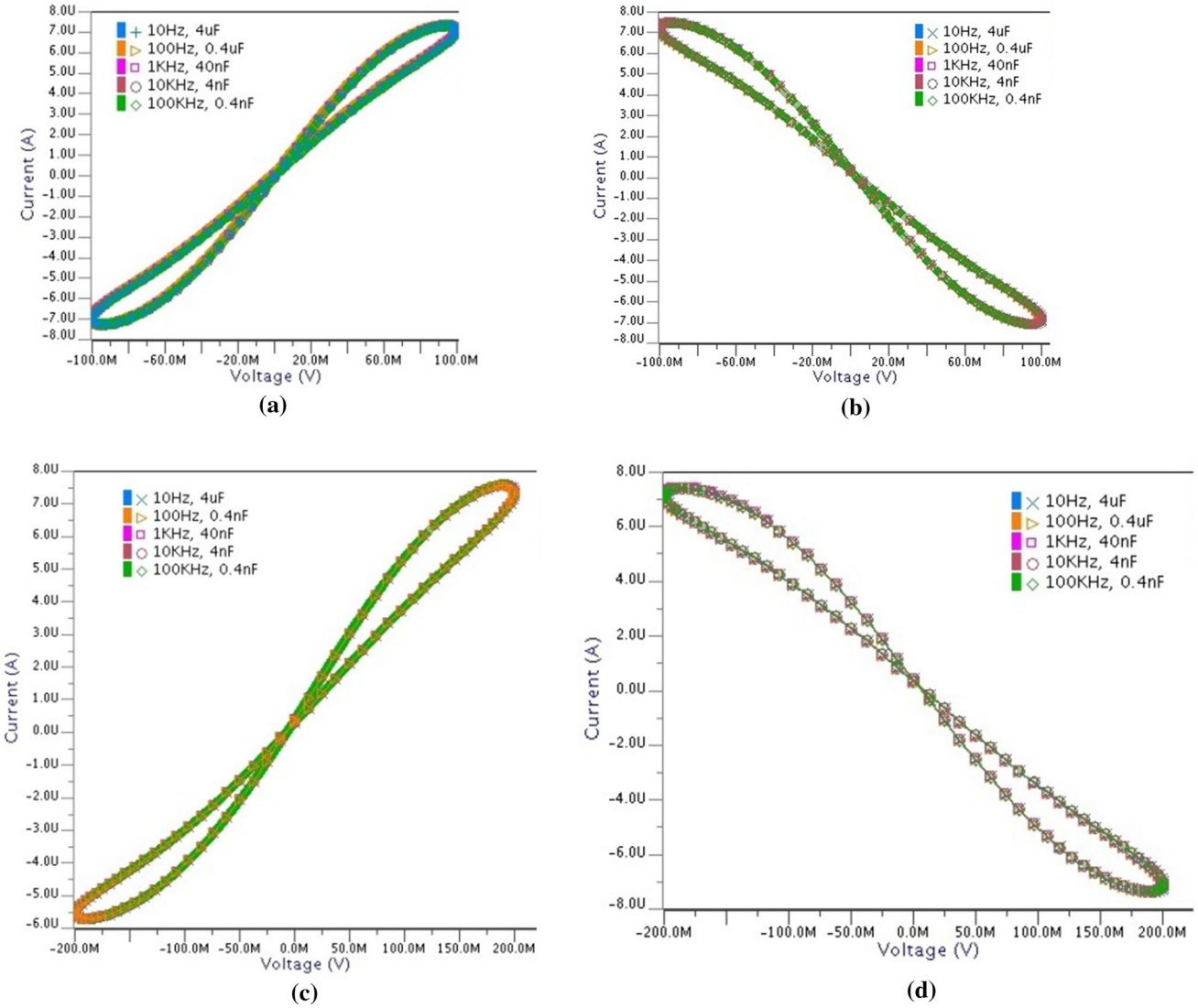

Fig. 10 Pinched Hysteresis loops of proposed memristor emulators for lower frequencies **a** grounded decremental **b** grounded incremental **c** floating decremental and **d** floating incremental

gain (β) both are the function of frequency and are represented by g_m (s) and $\beta(s)$. Therefore, the terminal characteristics of non-ideal FB-VDBA are given as

$$I_p = \frac{V_p}{Z_p}, \quad I_n = \frac{V_n}{Z_n} \tag{17}$$

$$I_{z+} = g_m(s).(V_p - V_n) + \frac{V_{z+}}{Z_{z+}}, \quad I_{z-} = -g_m(s).(V_p - V_n) + \frac{V_{z-}}{Z_{z-}} \tag{18}$$

$$V_{w+} = -[\beta(s).V_{z-} + I_{w+}Z_{w+}], \quad V_{w-} = -[\beta(s).V_{z+} - I_{W-}Z_{w-}] \tag{19}$$

where Z_p, Z_n, Z_{z-}, Z_{z+}, Z_{w-} and Z_{w+} are parasitic impedances of p, n, $z+$, $z-$, $w+$ and $w-$ terminals of FB-VDBA.

The transconductance $g_m(s)$ can be given as

$$g_m(s) = \frac{g_{m0}}{1 + \frac{s}{\omega_{gm}}} \tag{20}$$

where g_{m0} is the transconductance at lower frequencies of operation and ω is the pole frequency.

The gain of buffer amplifier of FB-VDBA can be given as

$$\beta(s) = \frac{\beta(0)}{1 + \frac{s}{\omega_\beta}} \tag{21}$$

where, $\beta(0)$ is the gain at lower frequencies and ω_β is the corresponding pole frequency.

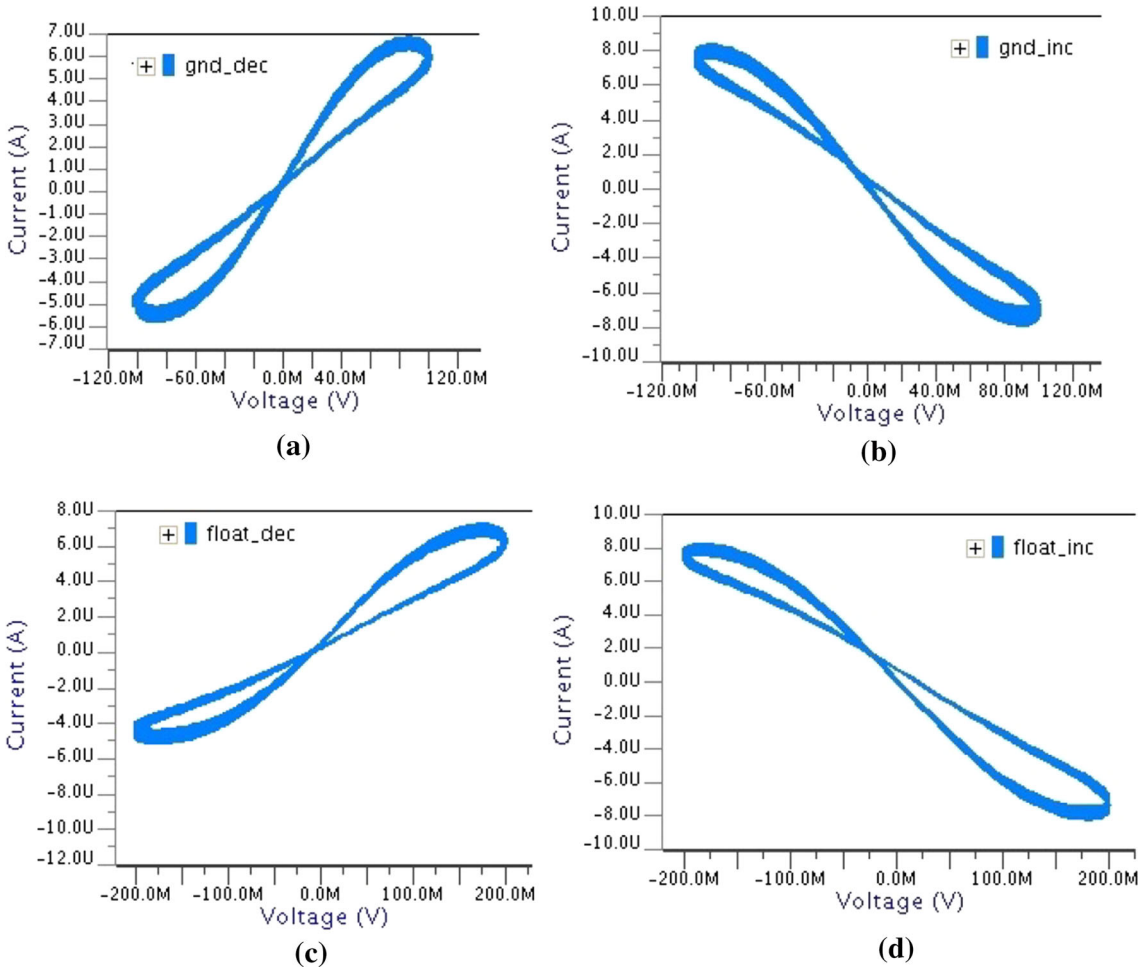

Fig. 11 Monte Carlo Pinched Hysteresis loops: **a** grounded decremental **b** grounded incremental **c** floating decremental **d** floating incremental

6.2 Performance of Grounded Memristor Emulator Circuit Including Parasitics

Non-ideal equivalent model of proposed grounded memristor emulator circuit is shown in Fig. 14 which includes the effect of parasitic impedances. The parasitic resistance and capacitance (R_p and C_p) appear in parallel at "p" terminal of FB-VDBA and is represented by parasitic impedance Z_p. Similarly, parasitic resistance and capacitance (R_n and C_n) are connected in parallel at "n" terminal of FB-VDBA and is represented by parasitic impedance Z_n. Parasitic resistance and capacitance (R_{z-} and C_{z-}) appear in parallel at "z−" terminal and are represented by parasitic impedance Z_{z-}. Similarly, parasitic resistance and capacitance (R_{z+} and C_{z+}) are connected in parallel at "$z+$" terminal and are represented by parasitic impedance Z_{z+}. The voltages (V_{z+} and V_{z-}) at $z+$ and $z-$ terminals are copied with the help of internal buffer of FB-VDBA. The parasitic resistance and inductance (R_{w-} and L_{w-}) appear in series at "w−" terminal and are represented by parasitic impedance Z_{w-}.

The values of parasitic impedances Z_p, Z_n, Z_{z-}, Z_{z+} and Z_{w-} are given by

$$Z_p = \frac{1}{sC_p + \frac{1}{R_p}}, \quad Z_n = \frac{1}{sC_n + \frac{1}{R_n}} \tag{22}$$

$$Z_{z+} = \frac{1}{sC_{z+} + \frac{1}{R_{z+}}}, \quad Z_{z-} = \frac{1}{sC_{z-} + \frac{1}{R_{z-}}} \tag{23}$$

$$Z_{w-} = R_{w-} + sL_{w-} \tag{24}$$

The routine analysis of Fig. 14 yields the value of current I_{z-} at intermediate terminal "z−"of FB-VDBA as

$$I_{z-} = G_m(s)V'_{\text{in}} = G_m(s)V_{\text{in}} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \tag{25}$$

where R_s is the source resistance of input voltage V_{in}.

The current I_{z+} of FB-VDBA is the same as obtained in Eq. (25).

$$I_{z+} = G_m(s)V_{\text{in}} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \tag{26}$$

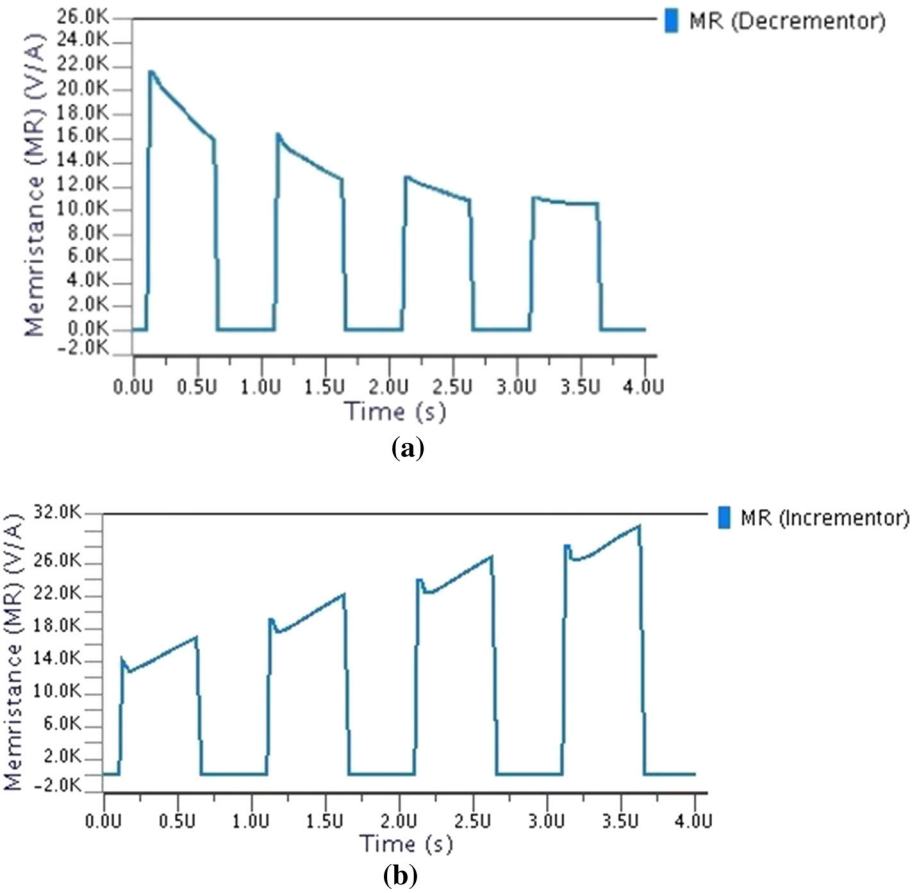

Fig. 12 Non-volatility tests: **a** grounded decremental **b** grounded incremental

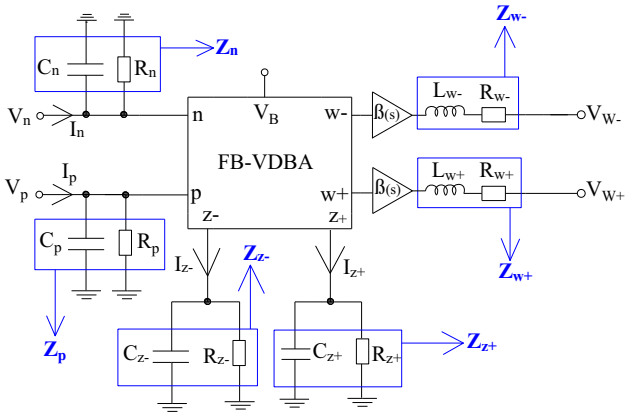

Fig. 13 Non-ideal model of FB-VDBA (Khatib and Biolek 2013)

The voltage V_z+ is obtained at $z+$ terminal of FB-VDBA as

$$V_{z+} = I_{z+} \times \frac{1}{s(C + C_{Z+}) + \frac{1}{R_{z+}}} \tag{27}$$

The value of V_z+ is obtained with help of Eqs. (26) and (27) as given in Eq. (28).

$$V_{z+} = G_m(s)V_{\text{in}} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \times \frac{1}{s(C + C_{z+}) + \frac{1}{R_{z+}}} \tag{28}$$

Since the value of $1/R_z + << s(C + C_{z+})$, Eq. (28) can be modified as

$$V_{z+} \cong G_m(s)V_{\text{in}} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \times \frac{1}{s(C + C_{z+})} \tag{29}$$

Equation. (29) can be rewritten as

$$V_{z+} \cong \frac{1}{(C + C_{Z+})} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \int G_m(s)V_{in}(t)\mathrm{d}t \tag{30}$$

The voltage V_{w-} can be expressed as given in Eq. (31) after considering the parasitic impedance Z_{w-} of FB-VDBA.

$$V_{w-} = -[\beta(s)V_{z+} - I_{w-}Z_{w-}] \tag{31}$$

The voltage transfer ratio between z + and w− terminals of FB-VDBA can be defined as

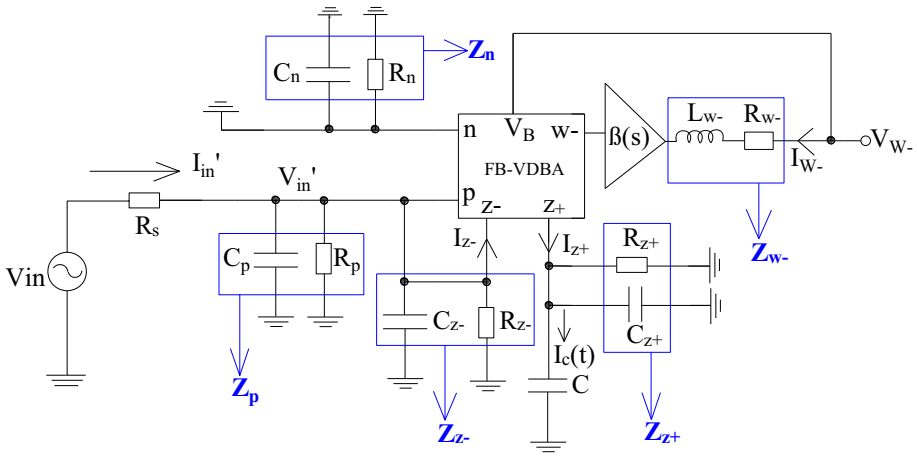

Fig. 14 Non-ideal equivalent model of proposed decremental grounded memristor emulator

$$\beta(s) = \frac{\beta(0)}{1 + \frac{s}{\omega_\beta}} \tag{32}$$

where, β (0) is the voltage transfer ratio between z + and w− terminals of FB-VDBA at dc and ω_β is the corresponding pole frequency.

Replacing the voltage V_{z+} from Eq. (30) into Eq. (31), the voltage V_{W-} can be written as

$$V'_w \cong -\left(\beta(s)\frac{1}{(C + C_{Z+})} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \int G_m(s)V_{in}(t)\mathrm{d}t - I_{w-}.Z_{w-}\right) \tag{33}$$

The biasing voltage V_B is directly connected to V_{W-} in Fig. 14 and can be expressed as

$$V_B \cong -\left(\beta(s)\frac{1}{(C + C_{Z+})} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \int G_m(s)V_{in}(t)\mathrm{d}t - I_{w-}.Z_{w-}\right) \tag{34}$$

The term $\int V_{in}(t)\mathrm{d}t$ can be represented by flux (ϕ) and thereby Eq. (34) is now changed to

$$V_B \cong -\left(G_m(s)\beta(s)\frac{1}{(C + C_{Z+})} \times \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}} \cdot \varphi_{in} - I_{w-}.Z_{w-}\right) \tag{35}$$

After replacing the voltage V_B from Eq. (35) into Eq. (5), we get

Equation. (36) can be rearranged as

$$G_m(s) = \frac{k}{\sqrt{2}}\left[-\left(G_m(s).\beta(s).\frac{1}{(C + C_Z)} \cdot \frac{1}{1 + G_m(s)R_s + \frac{R_s}{Z_p||Z_{z-}}}.\varphi_{\text{in}} - I_{W-}.Z_{w-}\right) - V_{\text{SS}} - 2V_{\text{th}}\right] \tag{36}$$

$$G_m(s) = -\frac{\frac{k}{\sqrt{2}}(V_{\text{SS}} + 2V_{\text{th}})}{1 + \frac{k}{\sqrt{2}}\left[\beta(s).\frac{1}{(C+C_Z)} \cdot \frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_p||Z_{z-}}}.\varphi_{\text{in}} - I_{W-}.Z_{w-}\right]} \tag{37}$$

The value of input current I_{in}' (*t*) can be obtained from Fig. 14 as

$$I'_{in}(t) = I_{z-} \times \left[1 + \frac{R_o}{Z_p||Z_{z-}}\right] \tag{38}$$

where R_0 is the output resistance of z− terminal of FB-VDBA.

After replacing the current I_{z-} from Eqs. (25) to (38), we get

$$I'_{in}(t) = G_m(s)V'_{in}(t)\left[1 + \frac{R_o}{Z_p||Z_{z-}}\right] \tag{39}$$

The value of memristance $M(\varphi_m)$ for the non-ideal decremental grounded memristor emulator circuit is obtained from Eq. (39) as

$$M(\varphi_m) = \frac{V'_{in}(t)}{I'_{in}(t)} = \frac{1}{G_m(s)} \times \frac{1}{1 + \frac{R_o}{Z_p||Z_{z-}}} \tag{40}$$

When the value of G_m (s) is substituted from Eq. (37) into Eq. (40), we get the value of memristance $M(\varphi_m)$ as

$$M(\varphi_m) = \frac{V'_{\text{in}}(t)}{I'_{\text{in}}(t)} = -\frac{1}{\frac{k}{\sqrt{2}}(V_{\text{SS}} + 2V_{\text{th}})} - \frac{\beta(s).\frac{1}{(C+C_{Z+})} \cdot \frac{1}{1+G_m(s)R_s+\frac{R_s}{Z_p||Z_{z-}}}.\varphi_{\text{in}} - I_{W-}.Z_{w-}}{(V_{\text{SS}} + 2V_{\text{th}})} \tag{41}$$

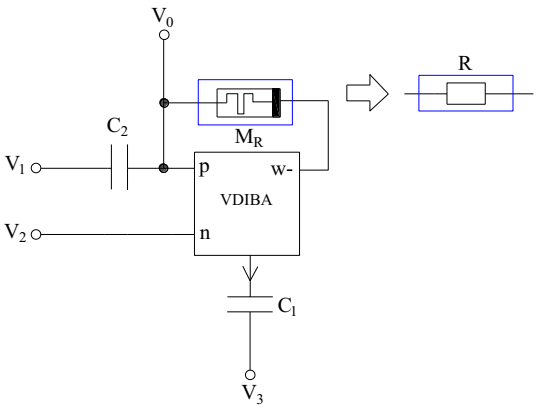

Fig. 15 Universal biquad filter reported in (Pushkar et al. 2014)

The fixed part of memristance remains same for ideal and non-ideal grounded decremental memristor emulator circuit, whereas variable part is changed due to parasitic impedances at various terminals of FB-VDBA. The value of parasitic capacitance C_{z+} is very low, and therefore, the effect of C_{z+} on the performance of memristor emulator circuit will be negligible. The source resistance value R_s is very low, and therefore, the effect of parasitic impedance Z_{z-} becomes negligible. The voltage gain (β) is very close to one, and it remains in acceptable range up to 1 MHz frequency. The parasitic impedance Z_{w-} appears in series and has negligible effect on the performance of memristor emulator circuits. It is observed from Eq. (41) that the effects of parasitic impedances on the performance of memristor emulator circuits are negligible and thereby its performance is found to be satisfactory in non-ideal conditions.

7 Application of Proposed Floating Decremental Memristor Emulator

The worthiness of proposed floating decremental memristor emulator circuit is verified by using it in the realization of universal biquad filter (Pushkar et al. 2014) as shown in Fig. 15. In universal biquad filter, the floating resistor (R) has been replaced by floating memristance (M_R) to verify its performance at high frequency. The average value of memristance (M_R) is set to1 kΩ. The values of capacitors are chosen as C1 = C2 = 20 pF and biasing current of voltage differencing inverted buffered amplifier (VDIBA) is chosen as 100 μA. The circuit diagram of VDIBA used to implement universal biquad filter is same as given in (Pushkar et al. 2014). The center frequency (fo) of VDIBA-based universal filter is given as

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_m}{R_0 C_1 C_2}} \tag{42}$$

The pinched Hysteresis loop of memristor emulator shrinks with the increase in frequency, and it gets converted to a single-valued function when frequency of sinusoidal input is increased beyond a critical frequency. This single-valued function is represented by a resistor. To show the performance of proposed floating decremental memristor emulator as a resistor at high frequency, universal biquad filters have been realized using both the resistor (R) and the proposed memristor (M_R). The obtained simulation results depicted in Fig. 16a, b show almost similar behavior and thus the performance of memristor as a resistor at high frequency is verified. The center frequency (f_0) has been obtained as 5.7 MHz.

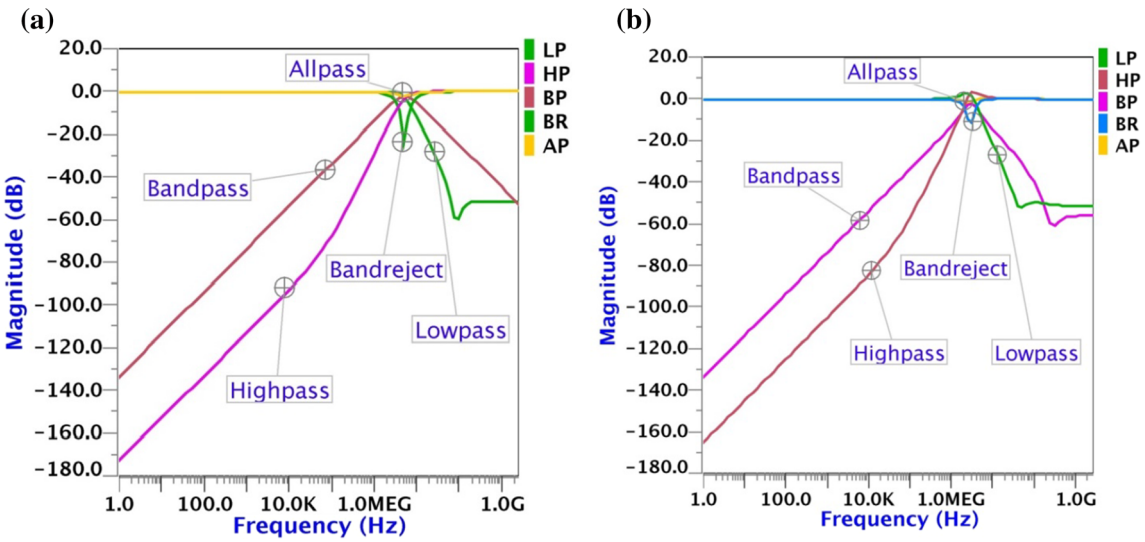

Fig. 16 Response of universal biquad using **a** resistor R **b** memristance M_R

8 Conclusions

New decremental/incremental memristor emulator circuits have been proposed using one fully balanced voltage differencing buffered amplifier (FB-VDBA) and a capacitor. The decremental memristors can be easily obtained from incremental memristors by interchanging the input terminals of voltage-tunable FB-VDBA. These configurations work satisfactorily for wide range of frequencies. Monte Carlo and non-volatility tests have been performed on proposed memristor emulators, and the obtained results are found to be satisfactory. The performance has also been verified by embedding the proposed floating decremental memristor emulator in the design universal biquad filter.

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