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From conductor to semiconductor: Diameter tuning of electrospun ITO nanowire for low-cost electronics

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ABSTRACT Constructing a semiconducting channel and electrodes using an identical material is a reliable method to fabricate low-cost, high-performance transistors. Wide-bandgap metal oxide semiconductors (MOSs) have been widely applied in various circuits. However, it is still a challenge to make low-cost transistors with a channel and electrodes based on identical MOSs. Here, we applied an electrospinning technique coupled with a nanowire transfer technique to fabricate high-performance, electrical-biased transistors with a one-dimensional indium tin oxide (ITO) nanowire, used as the semiconducting channel and the conducting source/drain (S/D) electrodes. The transition from a regular-conducting ITO to the newly-designed semiconducting ITO was achieved by tuning the needle diameter of the electrospinning nozzle. This method can be extended to the construction of future flexible and transparent transistors with both a channel and S/D electrodes.

Keywords: field-effect transistor, nanowire, electrospinning, low-dimension, lost-cost

INTRODUCTION

Transistors hold the key to constructing a constellation of circuits in the modern semiconductor industry [1,2], and this dominance is especially pronounced in the currently accelerating use of artificial intelligence [3,4], for which the flexibility and transparency of active materials are among the vital prerequisites for wearable electronics and embodied intelligence [5,6]. In this regard, wide-bandgap metal oxide semiconductors (MOSs) have been widely applied in a variety of flexible circuits for computing, transparent large-area electronics for interactive displays, transparent solar cells for power, and so on [7,8].

Among the plethora of MOSs, indium tin oxide (ITO) is unique in its aspects of large conductivity and high transparency [9–11], as well as its capability to transform from a conductor to a semiconductor [12–14]. This conductor-semiconductor transition is particularly valuable in devising a transistor configuration with active semiconducting materials and electrodes through a solely identical fabrication process with low-cost potential. Li *et al.* [15] reported on short-channel, active transistors using ultra-thin 4-nm ITO thin films as active semiconducting materials, from which they constructed high-performance logic inverters. However, the heavily involved ITO sputtering technique limited the potential of low-cost fabrication of the ITO-based transistors [15]. Afterwards, Si *et al.* [16] combined the ITO sputtering process with a wet-etching technique to obtain recessed, 1-nm ITOs as semiconductors combined with the originally sputtered ITO as source/drain (S/D) electrodes. Although this fine tuning of the ITO thickness demonstrated the potential for an ultra-small transistor configuration with a thin semiconductor channel and dielectric for high-speed calculation, the disadvantages of this complicated sputtering-etching fabrication process outweigh the benefits of the superior calculating capability [16], especially for certain low-power display applications in which a low cost is desirable [17–19]. Atomic layer deposition (ALD) is another complicated method to construct ITO-based transistors, yet the fine tuning of the indium/tin ratio can be obtained by more ideal, low-cost fabrication techniques [20].

Apart from the aforementioned conductor-to-semiconductor transition achieved *via* two-dimensional (2D) ITO or ITO thin films, no literature have been devoted to exploring 1D ITOs for conductor-to-semiconductor transitions *via* low-cost 1D material fabrication processes, despite various advantages of 1D nano configurations, e.g., the ultra-high surface-to-volume ratio and superior charge carrier transport characteristics [21–25]. Our group has previously developed a 1D nanowire MOS fabrication process combining low-cost electrospinning and a facile nanowire transfer technique by which we have fabricated high-performance ultraviolet phototransistors [26,27] and electrical- and optical-driven artificial synaptic transistors [28–31]. However, the MOSs implemented in those studies were utilized as semiconducting materials without a consideration of constructing a combination of transistor channel and S/D electrodes using one simple identical fabrication process.

In this work, we applied the electrospinning technique coupled with the nanowire transfer technique to fabricate high-performance, electrical-biased transistors with 1D ITO nanowire, producing both a semiconducting channel and the conducting S/D electrodes. The transition from a regular conducting ITO to the newly-designed semiconducting ITO has been achieved by meticulously adjusting the needle diameter of the electrospinning nozzle. When the needle diameter is 0.11 mm, the ITO-0.11 field-effect transistors (FETs) have superior electrical characteristics with an optimal on/off current

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ratio (I_{ON}/I_{OFF}) of 2 × 10^6 and a small threshold voltage (V_{th}) of 0.6 V. The resistor-loaded inverters based on the ITO-0.11 FETs have exhibited full swing output properties, and a suitable voltage gain of 3.5 at a supply voltage of 4 V. Additionally, an n-type MOS (NMOS) circuit was fabricated based on a depletion-mode (D-mode) ITO-0.21 and enhancement-mode (E-mode) ITO-0.11 FETs as load and drive devices to improve the gain of the inverter, with a relatively high gain (8.6) obtained. This work provides an efficient method to construct future flexible and transparent transistors with both a channel and S/D electrodes using the same simple fabrication process.

EXPERIMENTAL SECTION

Preparation of precursor solution

Indium nitrate ($In(NO_3)_3 \cdot xH_2O$, 0.135 g, 99.9%, Aladdin), stannous chloride ($SnCl_2 \cdot 2H_2O$, 0.011 g, 98%, Aladdin) and polyvinyl pyrrolidone (PVP, 0.8 g, 1,300,000 g mol^{-1}, Aladdin) were dissolved into 5 mL of *N*,*N*-dimethylformamide (C_3H_7NO, Aladdin). The initial solution was stirred at room temperature for 12 h to form a viscous ITO precursor solution.

Device fabrication

Firstly, the heavily doped p-type Si substrates were thoroughly cleaned in deionized water, acetone and ethanol in turn. Next, the ITO nanowires were fabricated *via* an electrospinning method by needles with inner diameters of 0.34, 0.21, 0.11 and 0.08 mm, respectively. The direct-current voltage was 15 kV and the flow rate was kept at 0.006 mL min^{-1}. Parallel nanowires were obtained on the metal collector. This was followed by a transfer method in which the prepared ITO nanowires were uniformly distributed onto a Si/SiO_2 substrate. Afterwards, the ITO nanowires as S/D electrodes were prepared through the electrospinning method using a shadow mask (width/length = 3000/100 μm). Finally, the nanowires were heated at 150°C for 10 min and treated with ultraviolet (UV) irradiation for 40 min to enhance the nanowire adhesion with the substrate. To completely remove the organic residues, the ITO nanowires were annealed at 500°C for 2 h.

Material and electrical characterization

The surface morphology and crystal structure of the nanowires were characterized using a combination of X-ray diffraction (XRD, Rigaku D/max-rB), scanning electron microscopy (SEM, Nova Nano SEM450, 15 kV), transmission electron microscopy (TEM, JEOL JEM 2100F, operated at 200 kV) and high-resolution TEM (HRTEM, JEOL JEM 2100F, operated at 200 kV). The composition and elemental distributions of the nanowires were analyzed using selected-area electron diffraction (SAED, JEOL JEM 2100F, operated at 200 kV). The optical characterizations were tested with a Shimadzu UV-visible spectrophotometer (UV-3600). The electrical properties of the fabricated FETs were measured under environmental conditions *via* a parametric analyzer (Keithley B2912A).

RESULTS AND DISCUSSION

Operation mechanism

Fig. 1a demonstrates the preparation process of the all-nanowire-based ITO FETs made by the electrospinning method. Importantly, both the channel and electrode regions of the FETs are comprised of ITO nanowires. The best electrical properties of the produced ITO FETs were obtained through adjusting the needle diameter of the electrospinning equipment, and varying the orientation of the obtained nanowires. The preparation process was mainly divided into two steps. First, we designed metal sheets as parallel nanowire collectors, and ITO nanowires with needle diameters of 0.11 mm (ITO-0.11) produced in a quasi-parallel direction above the collector under the biasing of an electric field. The prepared ITO-0.11 nanowires were then homogeneously distributed on the Si/SiO_2 substrate *via* a simple transfer method. Second, ITO nanowires were fabricated as the source and drain electrodes of FETs, in which the ITO-0.34 nanowires were uniformly distributed in the semiconductor region by a shadow mask. The configuration of the all-nanowire-based ITO FETs is pictured in the optical photograph shown in the inset of Fig. 1a.

The ITO exhibits n-type semiconducting characteristics in which the tin atoms act as cationic dopants to replace the indium positions in the In_2O_3 lattice, thereby further increasing the number of charge carriers with subsequent high conductivity [32]. As a result, the ITO is generally not suitable for the channel layer of FETs. In this context, we have successfully transformed the ITO from conductor to semiconductor *via* regulation of the needle diameter of the electrospinning device. As illustrated in Fig. 1b, the diameter and grain size of ITO nanowires decline with the decrease of needle diameters, which can lead to two important implications. First, a quantum size effect appears in the ITO-0.11 nanowires due to a grain size less than 10 nm, which further increases the band gap [33]. The additional energy required for the electrons to be driven from the valence band to the conduction band distinctly lowers the charge carrier concentration. Second, the smaller grain size results in a larger density of grain boundaries (the inset of Fig. 1b), and the atomic structure at the grain boundary produces more grain boundary defects [34]. Therefore, the free electrons will be trapped and create an electrical potential at the grain boundary, which impedes the transport of charge carriers in the ITO nanowires resulting in the reduction of carrier mobility. Regarding the variation in grain size, at certain annealing temperatures, the grain size of the ITO nanowires constantly increases due to numerous small grains aggregating into larger grains [35]. With increased nanowire diameter, the spaces where small grains form can be further increased [36]. Consequently, the large-scale aggregation of small grains can lead to larger grains, which facilitates the crystallization of the ITO nanowires.

Nanowire morphology

Fig. 2a illustrates the optical image of parallel ITO nanowires in the channel region. Macroscopically continuous and relatively consistent orientations are observed within the ITO nanowire arrays. We also adopted the electrospinning method to construct the ITO electrodes. As depicted in Fig. 2b, the nanowires in the electrode region of the ITO FETs are relatively uniform and very dense. In order to fully evaluate the diameters and grain sizes of the nanowires at different needle diameters, TEM was conducted. As demonstrated in Fig. 2c, the diameter and grain size of the ITO-0.11 nanowire are 66 and 8 nm, respectively. Fig. S1 shows that the diameters of the ITO-0.08, ITO-0.21, and ITO-0.34 nanowires are 57, 78 and 102 nm, and the corresponding grain size are 5, 12 and 17 nm, respectively. Based on the statistics of 60 nanowires from each sample, Fig. S2 illustrates that

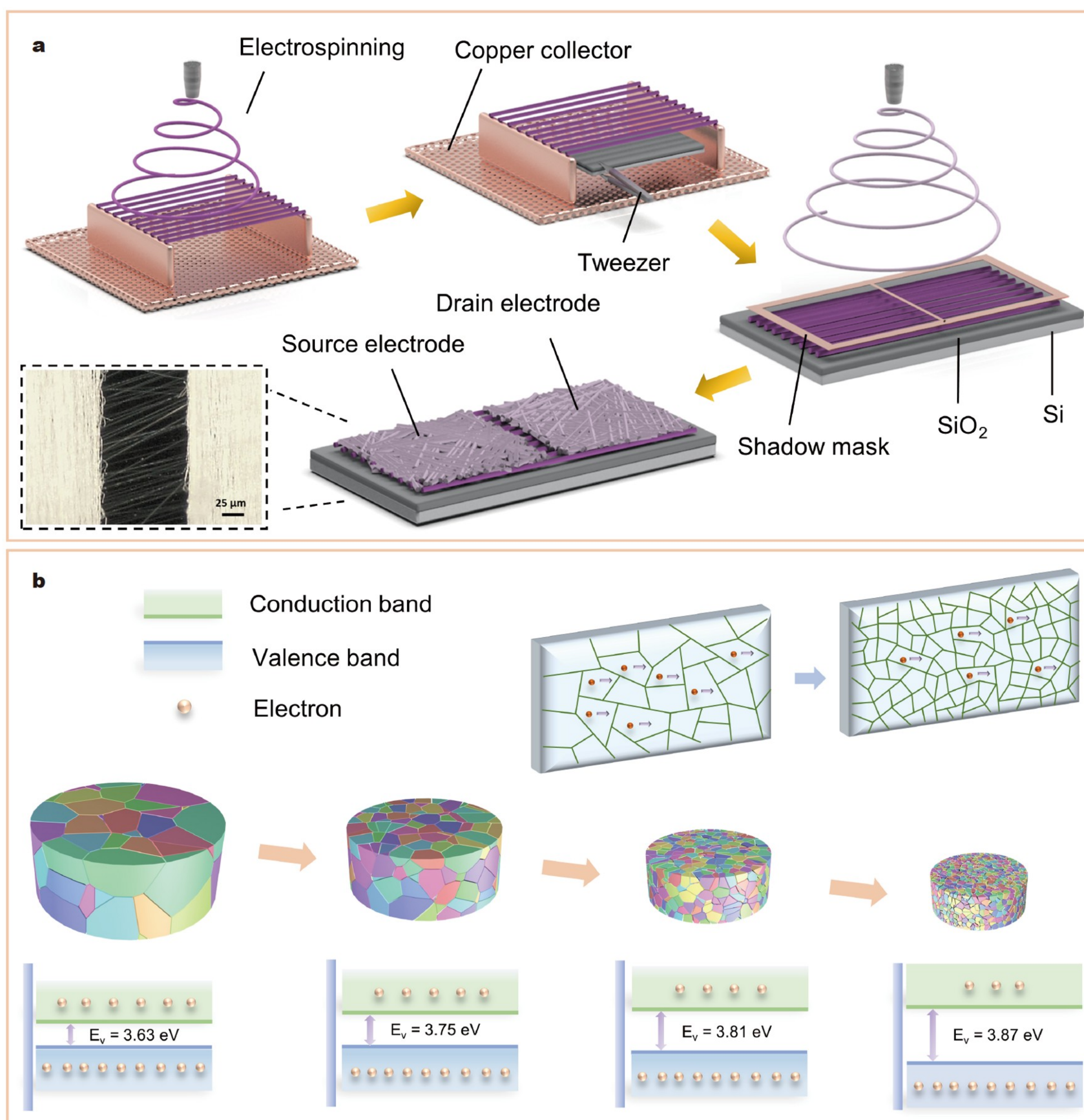

Figure 1 (a) Schematic illustration of the electrospinning method to fabricate transistors with both semiconductors and electrodes consisting of ITO nanowires. The inset presents an exemplified all-nanowire-based ITO FET. (b) Variation of band gap corresponding to different needle diameters. The inset in the up-right corner demonstrates the decrease of grain size as the nanowire diameter decreases.

the average diameters are 57 ± 3, 66 ± 4, 78 ± 3 and 102 ± 3 nm for the ITO-0.08, ITO-0.11, ITO-0.21 and ITO-0.34 nanowires, respectively. As shown in Fig. S3, the average grain sizes of the nanowires are 5 ± 2, 8 ± 2, 12 ± 3 and 17 ± 4 nm corresponding to the ITO-0.08, ITO-0.11, ITO-0.21 and ITO-0.34 nanowires, respectively. The grain size of the ITO nanowires diminished with further decreasing needle diameters, which introduced more grain boundaries, thus blocking the transmission of charge carriers [37].

XRD was conducted to evaluate the crystallinity of the ITO nanowires with different needle diameters. Fig. S4 shows the XRD patterns of the ITO nanowires with needle diameters of 0.34, 0.21, 0.11 and 0.08 mm, respectively. Obvious diffraction peaks appeared in the XRD diffraction patterns of all ITO nanowires, and the main diffraction peaks of (222), (400), (440) and (622) planes are consistent with the cubic phase of In_2O_3 (PDF#06-0416). All the samples exhibit a strong characteristic peak of (222), which belongs to the cubic In_2O_3 phase. Furthermore, due to the low proportion of tin in the ITO nanowires, the diffraction peaks for SnO_2 are not observed in the XRD pattern. All these results demonstrate that the ITO nanowires possess superior crystallinity under different needle diameters.

The detailed structure of the ITO-0.11 nanowire is shown in Fig. 2d, which is continuous with a straight and relatively coarse surface. In the electron diffraction pattern (Fig. 2e), the non-consecutive diffraction rings indicate the polycrystalline properties of the ITO nanowires. As presented in Fig. 2f, the HRTEM image further determines the crystallinity of prepared ITO nanowires in which the interplanar spacing of 0.27 and 0.25 nm correspond to the (321) and (400) planes. These match the properties of a cubic In_2O_3 lattice. In addition, the elemental distribution and composition of the ITO nanowires were confirmed using energy dispersive X-ray spectroscopy (EDS) map-

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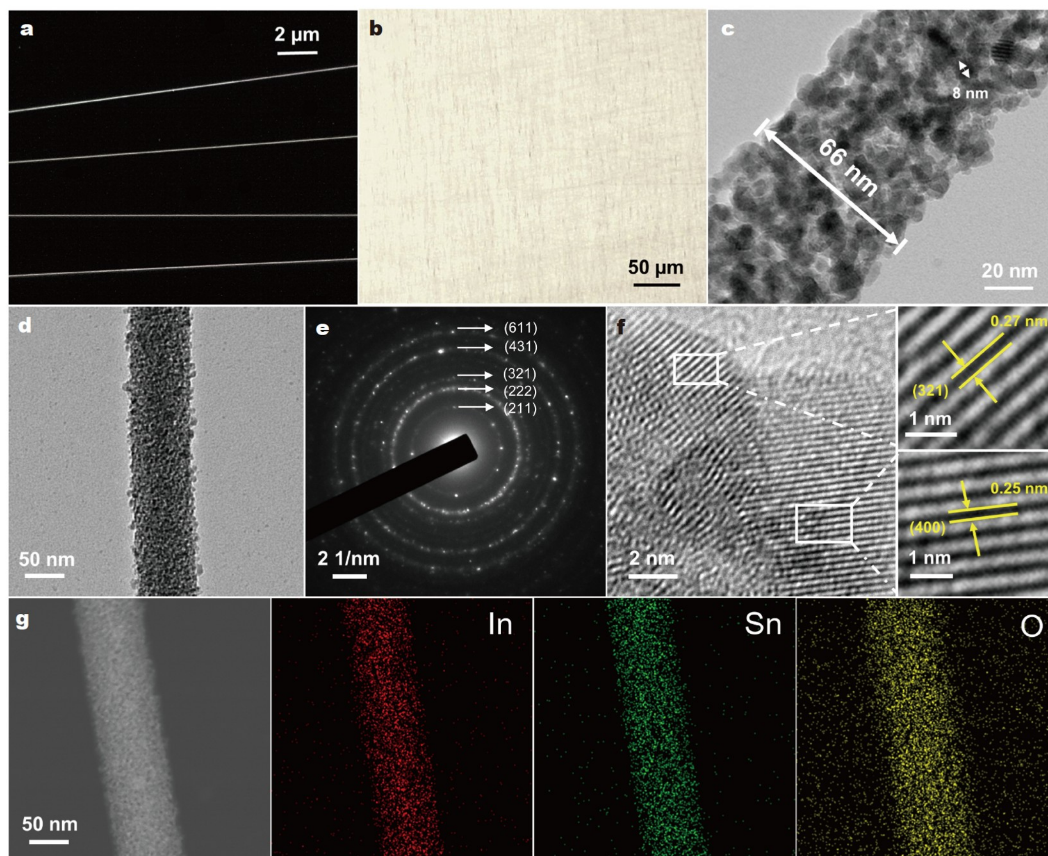

Figure 2 Optical images of (a) ITO nanowire arrays and (b) ITO electrode. (c, d) TEM images of single ITO-0.11 nanowire. (e) SAED of the ITO-0.11 nanowire. (f) HRTEM images of the ITO-0.11 nanowire. (g) Corresponding EDS elemental mapping.

ping. Fig. 2g demonstrates that all the In, Sn, and O atoms are homogeneously distributed in the nanowires, and proves that high-quality nanowires can be achieved by using the appropriate needle diameter.

Electrical performance

We carried out UV-visible spectrophotometry to analyze the bandgap changes of the ITO nanowires fabricated *via* varing the needle diameters of 0.34, 0.21, 0.11 and 0.08 mm, respectively. The optical absorption spectra of all the fabricated ITO nanowires are displayed in Fig. 3a. Fig. 3b illustrates the corresponding $(Ahv)^{1/2}$–(hv) curves, where A is the absorption, h is the Planck constant, and v is the incident photon frequency. And the bandgaps of 3.63, 3.75, 3.81 and 3.87 eV correspond to ITO-0.34, ITO-0.21, ITO-0.11 and ITO-0.08 nanowires, respectively. The bandgap of the ITO nanowires increases with decreased needle diameters because of the quantum size effect in the ITO nanowires. With the augmentation of the bandgap, more excitation energy is needed for the electrons to jump from the valence band to the conduction band, leading to a reduction in the on-current and off-current of the ITO FETs.

In order to investigate the influence of ITO FETs with different needle diameters on the electrical performance, we analyzed the transfer curves. As demonstrated in Fig. 4a, all devices exhibit n-type conductive behavior. The transfer curve of the ITO-0.34 FETs shows a large on-current (I_{ON}) of 1×10^{-4} A and off-current (I_{OFF}) of 8×10^{-6} A, which leads to a lower I_{ON}/I_{OFF} ratio and negative threshold voltage (V_{TH}). Owing to the larger grain size of ITO-0.34 nanowires, the smaller band gap facilitates the electrons jumping from valence band maximum to conduction band minimum, resulting in an increase in carrier concentration. However, the I_{ON} and I_{OFF} gradually decreases with decreasing needle diameters, and the best performance of the ITO FETs was achieved when the needle diameter was 0.11 mm with a corresponding I_{ON} and I_{OFF} of 4×10^{-5} and 2×10^{-11} A, respectively. The grain size of the ITO-0.11 nanowires is around 8 nm, which results in further widening of the band gap due to the quantum size effect. Therefore, the number of electrons in the conduction band gradually declines. When the needle diameter is reduced to 0.08 mm, the average grain size of ITO-0.08 nanowires is 5 nm, and the influence of quantum size effect is more pronounced, leading to a further decreased I_{ON} and I_{OFF}. All these results indicate that the simple electrospinning method can not only transform the ITO from a conductor to a semiconductor, but also obtain the best electrical properties by adjusting the needle diameters.

As illustrated in Fig. 4b, the corresponding V_{TH} of the ITO FETs gradually shifts from −7 to 9 V as the needle diameter decreases. The operating mode of the device successfully changes from D-mode to E-mode. Moreover, the optimal V_{TH} (0.6 V) can be obtained when the needle diameter is 0.11 mm. These results show that the carrier concentration of the ITO FETs can be controlled by changing the needle diameters. The output curve of the ITO-0.11 FETs is provided in Fig. 4c, revealing clear linear-saturation regions and n-type conduction behavior. In addition, the output curves of the ITO-0.08, ITO-0.21 and ITO-

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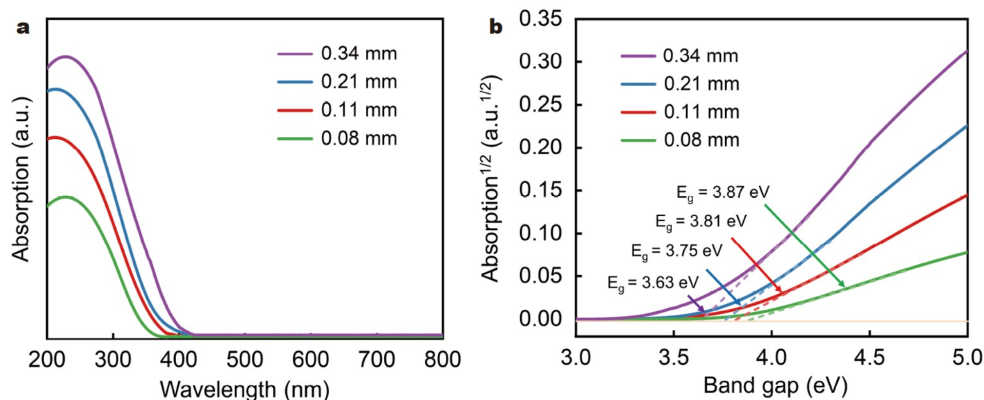

Figure 3 (a) Absorption spectra of ITO nanowires corresponding to different needle diameters. (b) Corresponding $(Ahv)^{1/2}$–(hv) curves.

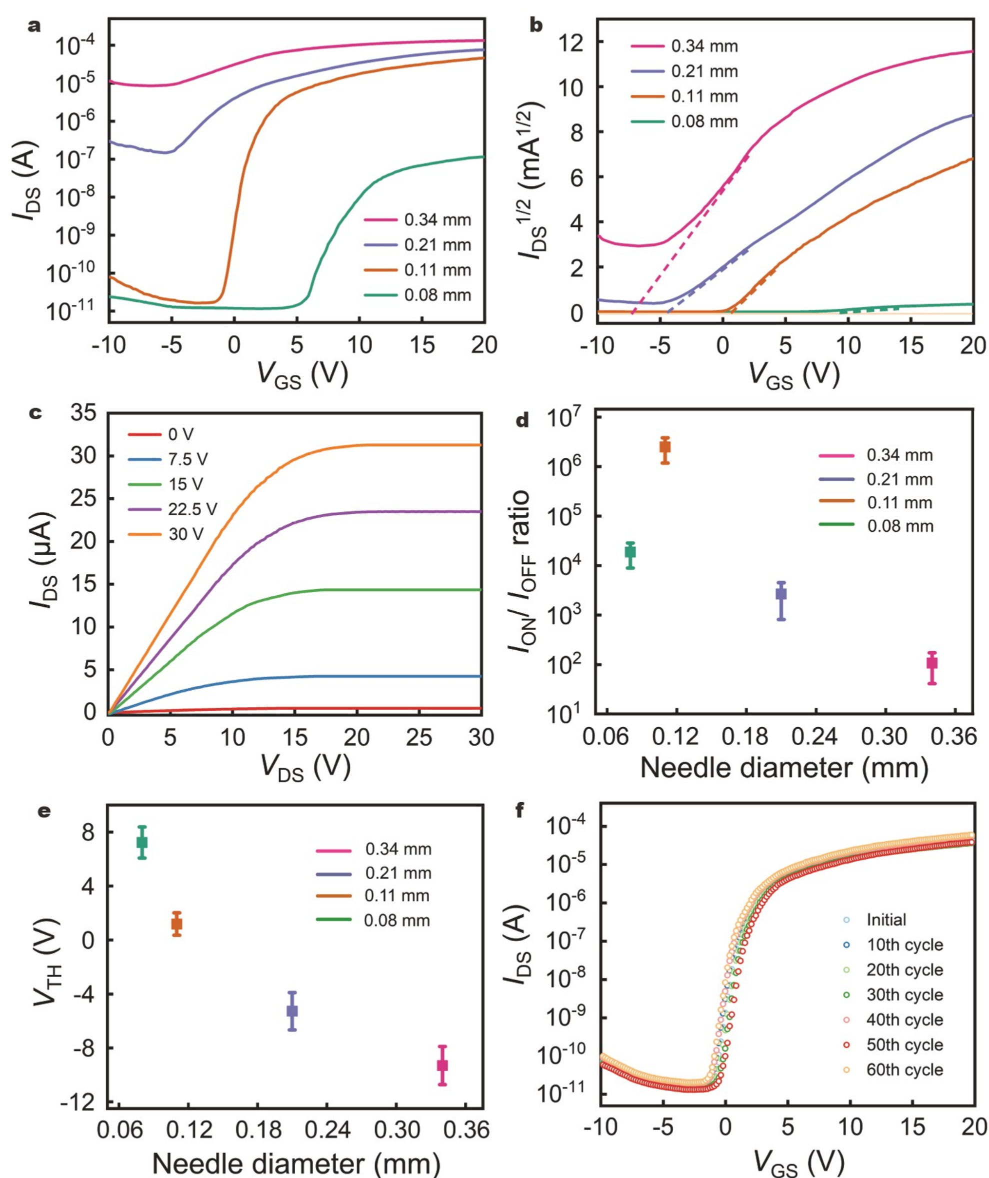

Figure 4 (a) Transfer curves of ITO FETs with needle diameters of 0.34, 0.21, 0.11 and 0.08 mm, respectively. (b) Corresponding V_{TH} obtained from the transfer characteristics. (c) Output curves of ITO-0.11 FET. Averaged I_{ON}/I_{OFF} ratio (d), and V_{TH} (e) of ITO FETs corresponding to different needle diameters. (f) Transfer curves of ITO-0.11 FETs at different cycle measurements.

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0.34 FETs are presented in Fig. S5a–c, demonstrating that the nanowires between the electrode and the channel district exhibit good contact.

To investigate the accuracy of the electrical performance, the I_{ON}/I_{OFF} and V_{TH} of the ITO FETs based on different samples have been considered to make error bars. As shown in Fig. 4d, e, the optimal I_{ON}/I_{OFF} and V_{TH} of the ITO-0.11 FETs were obtained, and the corresponding value are 2.4×10^6, and 0.8 V, respectively. Furthermore, relatively small error ranges are present in the ITO-0.11 FETs. We studied the transfer characteristics of the ITO devices under different cycles (Fig. 4f), and found that the I_{ON}, I_{OFF} and V_{TH} yield a negligible change, even after 60 cycles.

The charge carrier mobility (μ) can be calculated according to the following equation [38]:

$$I_{DS} = \left(\frac{W}{2L} C_i \mu\right)(V_{GS} - V_{TH})^2, \tag{1}$$

where W is the effective channel width, L is the channel length, and V_{GS} and I_{DS} represent the gate voltage and drain current, respectively. C_i is the capacitance of the dielectric layer. As illustrated in Fig. S5d, the carrier mobility has been calculated to be 0.35, 1.89, 3.58 and 6.67 $cm^2\ V^{-1}\ s^{-1}$ corresponding to needle diameters of 0.08, 0.11, 0.21 and 0.34 mm, respectively. The smaller needle diameters reduce the grain size of the nanowires, leading to a higher density of grain boundaries, which hinders the transport of charge carriers.

The leakage current of the ITO transistors is shown in Fig. S6a. The magnitude of the leakage current is maintained at 10^{-12} A, which is much lower than I_{DS} under the same V_{GS} sweeping range. This suggests that the influence of the leakage current on electrical performance of the transistor is negligible. Fig. S6b provides the current–voltage (I–V) curve of the ITO electrode. The current linearly increases in the positive direction with increased voltage, corresponding to the ohmic law of conductors.

To further investigate the underlying application of the ITO FETs in integrated circuit, NOT-gate logic circuit was designed. As presented in Fig. 5a, they were mainly composed of ITO-0.11 FET and an exterior resistor of 470 kΩ, and the corresponding structure pattern is shown in Fig. S7. Fig. 5b illustrates the voltage transfer properties of the logic circuit, in which the full swing characteristics were fully exhibited under different supply voltages. The optimal voltage gain ($-dV_{OUT}/dV_{IN}$) obtained at a supplied drain voltage (V_{DD}) of 4 V (Fig. 5c), corresponds to a value of 3.5. Furthermore, we tested the dynamic output response of the inverter by implementing a square-wave input voltage (5 V) with a frequency of 1 Hz. Fig. 5d shows that the output voltage possesses good inversion characteristics with short signal delays after changing the input voltage. In order to further improve the gain of the inverter, we designed an NMOS circuit to realize the logic function of the inverter, mainly composed of a D-mode ITO-0.21 load FET and E-mode ITO-0.11 drive FET. The specific circuit design is shown in Fig. S8a. Fig. S8b demonstrates the transfer curves of the load and drive ITO FET, and the inset shows the schematic circuit diagram of the NMOS inverter. In addition, the voltage transfer curve in Fig. S8c obviously exhibits the inverse characteristic of the

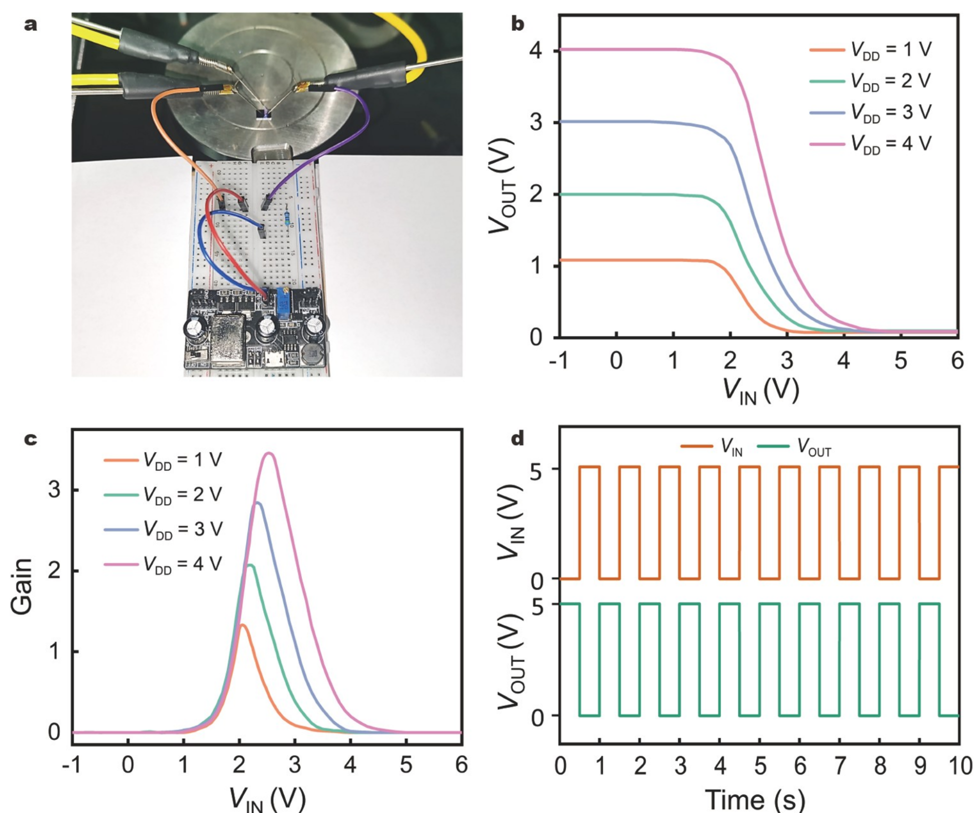

Figure 5 (a) Circuit diagram of the inverter based on ITO-0.11 FET and a resistor of 470 kΩ. (b) Voltage transfer properties and (c) the corresponding gains of the inverter with different supply voltages. (d) Dynamic output response under the square-wave voltage input of 5 V at the frequency of 1 Hz.

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output voltage. Changing the input voltage, a higher gain (8.6) can be obtained under the interaction of the D-mode and E-mode ITO FET (Fig. S8d). All of these demonstrate that the inverter can effectively achieve a transformation of logic signals (1 and 0) in a digital circuit.

CONCLUSIONS

In conclusion, high-performance, low-cost ITO FETs can be achieved *via* a facile one-step electrospinning method. Importantly, we have successfully transformed the ITO nanowires from a conducting metal to a semiconductor by adjusting the needle diameter. When the needle diameter is 0.11 mm, the ITO-0.11 FETs reveal optimum electrical characteristics, including an optimal I_{ON}/I_{OFF} of 2×10^6, a small V_{TH} of 0.6 V, and a suitable μ of 1.89 $cm^2 V^{-1} s^{-1}$. Moreover, resistor-loaded inverters based on the ITO-0.11 FETs exhibit full swing output properties, and a voltage gain of 3.5 with a supply voltage of 4 V. Using a D-mode ITO-0.21 FET to replace the resistor as a load device, the inverter achieved a higher gain of 8.6 at the same measurement conditions. This work introduces the promising potential of ITO FETs for large-scale, low-power electronic devices.

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1 Guo E, Xing S, Dollinger F, *et al.* Integrated complementary inverters and ring oscillators based on vertical-channel dual-base organic thin-film transistors. Nat Electron, 2021, 4: 588–594
2 Zheng Z, Zhang L, Song W, *et al.* Gallium nitride-based complementary logic integrated circuits. Nat Electron, 2021, 4: 595–603
3 Dai Y, Hu H, Wang M, *et al.* Stretchable transistors and functional circuits for human-integrated electronics. Nat Electron, 2021, 4: 17–29
4 Liu Y, Pharr M, Salvatore GA. Lab-on-skin: A review of flexible and stretchable electronics for wearable health monitoring. ACS Nano, 2017, 11: 9614–9635
5 Gwon G, Choi H, Bae J, *et al.* An all-nanofiber-based substrate-less, extremely conformal, and breathable organic field effect transistor for biomedical applications. Adv Funct Mater, 2022, 32: 2204645
6 Petti L, Münzenrieder N, Vogt C, *et al.* Metal oxide semiconductor thin-film transistors for flexible electronics. Appl Phys Rev, 2016, 3: 021303
7 Myny K. The development of flexible integrated circuits based on thin-film transistors. Nat Electron, 2018, 1: 30–39
8 Park JW, Kang BH, Kim HJ. A review of low-temperature solution-processed metal oxide thin-film transistors for flexible electronics. Adv Funct Mater, 2019, 30: 1904632
9 Oh SJ, Kwon JH, Lee S, *et al.* Unveiling the annealing-dependent mechanical properties of freestanding indium tin oxide thin films. ACS Appl Mater Interfaces, 2021, 13: 16650–16659
10 Shao Y, Xiao X, Wang L, *et al.* Anodized ITO thin-film transistors. Adv Funct Mater, 2014, 24: 4170–4175
11 Benoy MD, Mohammed EM, Suresh Babu M, *et al.* Thickness dependence of the properties of indium tin oxide (ITO) FILMS prepared by activated reactive evaporation. Braz J Phys, 2009, 39: 629–632
12 Liang K, Li D, Ren H, *et al.* Fully printed high-performance n-type metal oxide thin-film transistors utilizing coffee-ring effect. Nano-Micro Lett, 2021, 13: 164
13 Sakata T, Nishitani S, Saito A, *et al.* Solution-gated ultrathin channel indium tin oxide-based field-effect transistor fabricated by a one-step procedure that enables high-performance ion sensing and biosensing. ACS Appl Mater Interfaces, 2021, 13: 38569–38578
14 Zhou Y, Chen J, Yu R, *et al.* A full transparent high-performance flexible phototransistor with an ultra-short channel length. J Mater Chem C, 2021, 9: 1604–1613
15 Li S, Tian M, Gao Q, *et al.* Nanometre-thin indium tin oxide for advanced high-performance electronics. Nat Mater, 2019, 18: 1091–1097
16 Si M, Andler J, Lyu X, *et al.* Indium-tin-oxide transistors with one nanometer thick channel and ferroelectric gating. ACS Nano, 2020, 14: 11542–11547
17 Kim DW, Min SY, Lee Y, *et al.* Transparent flexible nanoline field-effect transistor array with high integration in a large area. ACS Nano, 2020, 14: 907–918
18 Wang B, Thukral A, Xie Z, *et al.* Flexible and stretchable metal oxide nanofiber networks for multimodal and monolithically integrated wearable electronics. Nat Commun, 2020, 11: 2405
19 Liu A, Zhu H, Liu G, *et al.* Draw spinning of wafer-scale oxide fibers for electronic devices. Adv Elect Mater, 2018, 4: 1700644
20 Zhang Z, Hu Y, Lin Z, *et al.* Atomically thin indium-tin-oxide transistors enabled by atomic layer deposition. IEEE Trans Electron Devices, 2022, 69: 231–236
21 He J, Liu X, Song L, *et al.* High annealing stability of InAlZnO nanofiber field-effect transistors with improved morphology by Al doping. J Phys Chem Lett, 2021, 12: 1339–1345
22 Zhang H, Meng Y, Song L, *et al.* High-performance enhancement-mode thin-film transistors based on Mg-doped In_2O_3 nanofiber networks. Nano Res, 2018, 11: 1227–1237
23 Zhu X, Li Y, Zhang H, *et al.* High-performance field effect transistors based on large ratio metal (Al、Ga、Cr) doped In_2O_3 nanofibers. J Alloys Compd, 2020, 830: 154578
24 Song L, Luo L, Li X, *et al.* Modulating electrical performances of In_2O_3 nanofiber channel thin film transistors *via* Sr doping. Adv Elect Mater, 2019, 5: 1800707
25 Wang F, Song L, Zhang H, *et al.* ZnO nanofiber thin-film transistors with low-operating voltages. Adv Elect Mater, 2018, 4: 1700336
26 He J, Xu P, Zhou R, *et al.* Combustion synthesized electrospun InZnO nanowires for ultraviolet photodetectors. Adv Elect Mater, 2022, 8: 2100997
27 Yang L, Liu H, Han J, *et al.* Ultra-low-dose CT lung screening with artificial intelligence iterative reconstruction: Evaluation *via* automatic nodule-detection software. Clin Radiol, 2023, 78: 525–531
28 Chang Y, Cong H, Zhou R, *et al.* Enhanced artificial synaptic properties enabled by arrays of electrolyte-gated electrospun InZnO nanowires. ACS Appl Electron Mater, 2022, 4: 2570–2579
29 Cong H, Chang Y, Zhou R, *et al.* Rational tuning of the cation ratio in metal oxide semiconductor nanofibers for low-power neuromorphic transistors. Sci China Mater, 2023, 66: 3251–3260
30 Xin S, Chang Y, Zhou R, *et al.* Ultraviolet-driven metal oxide semiconductor synapses with improved long-term potentiation. J Mater Chem C, 2023, 11: 722–729
31 Zhou R, Zhang W, Cong H, *et al.* Metal oxide semiconductor nanowires enabled air-stable ultraviolet-driven synaptic transistors for artificial vision. Mater Sci Semicond Proc, 2023, 158: 107344
32 Kim H, Horwitz JS, Kushto G, *et al.* Effect of film thickness on the properties of indium tin oxide thin films. J Appl Phys, 2000, 88: 6021–6025
33 Sun W, Qian C, Wang L, *et al.* Switching-on quantum size effects in silicon nanocrystals. Adv Mater, 2015, 27: 746–749
34 Zu H, Chang Y, Li H, *et al.* Modulating the transport properties of metal oxide nanofibers transistors by controlling the grain size. IEEE Electron Device Lett, 2021, 42: 855–858
35 Feng W, Zhou H, Chen F. Impact of thickness on crystal structure and optical properties for thermally evaporated PbSe thin films. Vacuum, 2015, 114: 82–85
36 Gao MZ, Job R, Xue DS, *et al.* Thickness dependence of resistivity and optical reflectance of ITO films. Chin Phys Lett, 2008, 25: 1380–1383
37 Marom H, Ritterband M, Eizenberg M. The contribution of grain boundary scattering *versus* surface scattering to the resistivity of thin polycrystalline films. Thin Solid Films, 2006, 510: 62–67
38 Fan C, Liu A, Meng Y, *et al.* Solution-processed SrO_x-gated oxide thin-film transistors and inverters. IEEE Trans Electron Devices, 2017, 64: 4137–4143

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Supplementary information Supporting data are available in the online version of the paper.

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从导体到半导体: ITO纳米线直径调控制备低成本电子器件

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摘要 金属氧化物半导体(MOSs)由于具有优异的光电学性能和稳定性, 在场效应晶体管(FETs)中具有广泛的研究价值. 然而, 以相同的MOSs材料作为FETs的沟道和源漏电极仍存在较大挑战. 本文采用静电纺丝工艺和纳米线转移技术, 以一维氧化铟锡(ITO)为主体, 构筑了低成本高性能全纳米线FETs. 通过简单调节纳米线的直径, ITO实现了由导体向半导体的转变, 基于最佳的ITO纳米线作为沟道和电极材料组建的FETs获得了较大的开关比(10^6)和较低阈值电压(0.6 V). 此外, 基于全静电纺丝工艺制备的增强型和耗尽型ITO纳米线FETs实现了非门逻辑及n型MOS (NMOS)电路. 该方法为未来实现柔性透明光电子器件提供了可行方案.

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