



# Design and Investigation of Solar PV Fed Single-Source Voltage-Lift Multilevel Inverter Using Intelligent Controllers

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Received: 10 June 2021 / Revised: 19 November 2021 / Accepted: 28 December 2021 / Published online: 26 February 2022  
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## Abstract

The demand for sustainable energy has increased significantly over the years due to the rapid depletion of fossil fuels and also affect the greenhouse. Hence, compared with other Renewable Energy (RE) systems, it is highly preferred for solar photovoltaic device that must be extremely suitable for most of the sun irradiation regions. The proposed research work investigates a solar PV fed single phase Symmetric Voltage-Lift Inverter (SV-LI). The proposed inverter structure operates with symmetric model possibly for 7- level, 15- level, 21- level, 25- level, 35- level, and 45-levels of the output voltage. But, this article presented symmetric single phase inverter that can be obtained from suggested fifteen level structure by using different operating load conditions. The suggested structure can produce medium output voltages without using any extra filter, multiple power switching, or auxiliary H-bridge circuit. The objective of the research work is achieved with reduced number of power electronic switches. Later from an application point of view, the proposed SV-LI is connected to the R and RL load. The performance of multilevel inverter is improved by using different intelligent techniques such as Fuzzy Logic (FL)-based controller design, Fuzzy-Proportional Integral (F-PI)-based controller design, MPP-Fuzzy based controller design and Artificial Intelligent Techniques approach for analysis with MATLAB/Simulink platform. The development of SV-LI operating different load connected system is analyzed with improvement of output voltage, reactive power, and minimized harmonics level.

**Keywords** Solar-Photovoltaic (S-PV) · Symmetric voltage-Lift Inverter (SV-LI) · Fuzzy Logic Controller (FLC) · Maximum Power Point (MPP) · Proportional Integral (PI)

## List of Symbols

$\eta$	Efficiency
$V$	Voltage
$I$	Current
$W$	Watts
$V_0$	Output Voltage
$I_0$	Output Current
$V_{in}$	Input Voltage
$I_{in}$	Input Current
$kW_{in}$	Kilowatt Velocity $-\omega$
$V_{mp}$	Maximum peak voltage
$R_{pm}$	Revolution per minute

$T$	Shaft torque
Hz	Frequency
$V_{oc}$	Open circuit voltage
$I_{sc}$	Short circuit current
bhp	Brake horse power
$P_w$	Power loss
$P_{in}$	Power input
H	Head
Q	Flow rate
$\rho$	Density of fluid handled
g	Gravitational Constant
K	Duty Cycle
mH	Milli Henry
$\mu F$	Micro Fraud
$\Omega$	Ohm
H	Henry
m	Meter
$\alpha$	Firing angle
$I_{ph}$	Photo generated current

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$I_{\text{sat}}$	Diode saturation current
$R_{\text{p}}$	Parallel resistance
$R_{\text{s}}$	Series resistance

## Abbreviations

S-PV	Solar photovoltaic
SV-LI	Symmertic voltage—Lift Inverter
GA	Genetic algorithm
FA	Firefly algorithm
PSO	Particle swarm optimization
MPP	Maximum power point
P&O	Perturb & Observe
FPGA	Field program gate array
MLI	Multilevel inverter
RL	Resistive load
PV	Photovoltaic
DC	Direct current
AC	Alternating current
Nser	Number of series module
Npar	Number of parallel module
F.F	Fill Factor
COS	Change-Over switch
MI	Modulation index
SPM-TS	Singe pole multi-through switch

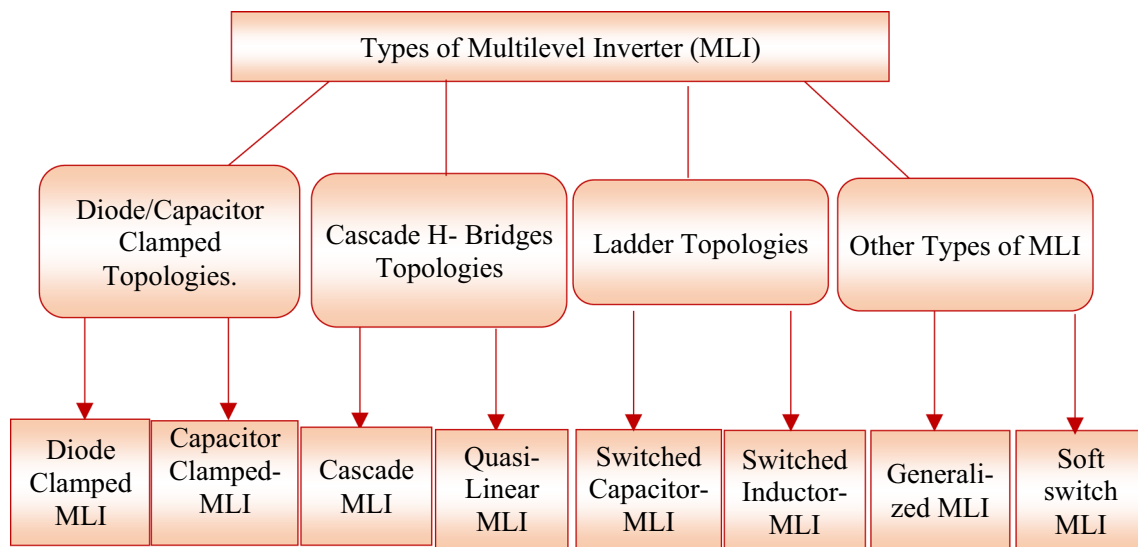
## 1 Introduction

Electrical or mechanical loads are governed by the power supply. The electrical power or voltage is transferred to certain loads should comply with Power Quality (P-Q) standards. Most P-Q issues are hidden from the solar power distribution electrical system, but their consequences result based on higher demand utility. The P-Q analysis in electrical load is generally divided into two categories: Nonlinear Load (N-LL) and Linear Load (LL). The power factor improvement in LL & N-LL observed much attention in the recent scenario for engineering researchers. However, it is necessary to improve the quality of the energy from these PV sources to safeguard the load connected equipment and maintain the customer continuity of supply without any disturbances. To fulfill the goal, it is necessary to connect intelligent techniques assists by the power electronic based multilevel inverter which enables the P-Q improvement in between the input source, and loads. Therefore, the development of electrical power is dramatically shifted to sustainable energy sources. Johny Renoald et al. (2021) have prescribed that in 2030 the total RE produced worldwide is expected to meet 55% compared to other resources (Johny Renoald et al., 2021).

The Solar-Photovoltaic (S-PV) panels are a versatile energy technology that can help electrical customers within all kinds of electricity needs. PV generation will supply a large proportion of the electricity demand suggested by the World Energy Council 2020 and can meet solar energy demand by 16% as much as 2030 needs in India (Albert & Stonier, 2021). Due to the reduction in fossil fuel, and the greenhouse effect need for RE has grown a lot over the years. The growth of the solar-power module in India ranged from 2.6 to 28.18 GW in 2019–2020 and the future it would be around 34 GW and 40 GW due to the increased demand for the electricity is needed (Solar power total installation capacity in India demands prepared by Ministry of New and Renewable Energy, Annual Report 2019) (Johny Renoald et al., 2016). However, it is necessary to improve the P-Q in RE sources for putting forth electrical load. The renewable power conversion from one stage to another stage without any disturbance, and continuity of the power supply is very important to the customer as prescribed by Hossain et al. (2018)

The solar electricity is developed by power semiconductor devices. It is capable of converting the incident PV energy Direct Current (DC) within a theoretical efficiency range while varied from 3% up to 31%, and global solar power demand also grow by 9% in every year estimated by Johny and Albert (2020). In such efficiency depends on manufacturing technology, temperature, panel tilt angle, shadows, and incident light spectrum, etc., the minimum harmonic content of output voltage produced by a single-phase grid-tied inverter is operating under low solar irradiance conditions applied in R load and RL load. Which is operating in ON/OFF grid mode under the sufficient PV-irradiance conditions proposed by Shanmugam et al. (2021). The input source of S-PV that aims to enhance P-Q with harmonious reduction process in various loads with the help of optimization or intelligent techniques, and it is convenient to integrate for both functionalities of power generation as well as P-Q development by using in Multilevel Inverter (MLI) (Kaliannan et al., 2021).

The Direct Current (DC) sources are used in the input side of the series converter; therefore, the multilevel converters are attractive for S-PV applications. In solar fed MLI is a standalone proposed system operated in OFF grid Balance of System Equipment (BSE), and it has been used for off-grid mode like electric motor drives, R, RL load. The BSE encompasses all equipment of a PV system other than the solar panels. MLI's have special functions adapted for added PV arrays includes with the Maximum Power Point (MPP) tracking with the parameter of current or voltage. In the PV array, the terminal voltage is not equal to the constant MPP, since the MPP is increasing in array voltage to improve P-Q development using intelligent techniques. To fulfill the goal, it is necessary to connect an electronics-based multi-level inverter which enables the P-Q improvement in between



**Fig. 1** Traditional and modified/MLI

**Table 1** Compare and implementation requirements in Traditional MLI

Implementation and specific requirements	NPC (Gnanavel et al., 2021)	FC (Oghorada et al., 2019)	CH-B (Ahmed et al., 2019)	MMC (Debnath et al. 2015)	Conventional (Mohd & Ali, 2018)
Design & complexity	Low	Medium (Capacitors)	High	Low	High
Modularity	Low	High	High	Medium	Medium
Control scheme	Voltage Balance	Voltage setup	Power share	Voltage share	Voltage share
Fault tolerance	Difficult	Easy	Easy	Easy	Easy

the DC sources, and loads (Ramaraju et al., 2022). Symmetric Voltage-Lift inverter (SV-LI) circuits having multiple series capacitors or capacitor bank ( $C_6 - C_{12}$ ). It is help to generate reactive power to meet the demand of the inductive loads. This will keep that reactive power from having to flow all the way from the utility to the loads (R, RL load). The novelty of the proposed work is focused on absence of filter components with minimize THD level.

## 2 Literature Review

The input renewable source is S-PV fed into MLI, which aims to improve the power quality with minimize the harmonics processes in various loads and it is convenient to integrate for both systems of power generation and distribution as reported by Bagalini et al. (2019). In general, there are four sorts of classical multilevel inverters structures like Diode/Capacitor clamped, Cascade H-Bridge, Ladder topology, and other types of conventional/modified MLI as shown in Fig. 1. These types are particularly supportive to increase the output voltage level. Different MLI compare and implementation of specific requirement mechanism is shown in

Table 1. An off-grid systems with unbalanced load (Dynamic change of load) R and RL load to evaluate the system dynamic performances of symmetrical 15 level MLI verified with voltage and current harmonics.

A DC source modularity is equal, and the results are proved in nonlinear (RL) load conditions in both simulation and hardware models. That is vertically routines in a reference wave to attain the appropriate multilevel output waveform (Janardhan et al., 2021). Daula et al. (2021) have emphasized modify MLI with the basic unit required 3-DC sources and 10 switches to synthesize fifteen level output. It will be many researchers describe the additional advantage of inverter control challenges such as increasing voltage level minimize power quality problems, and the absence of semi-conductor devices like as bulky switches, inductors, filter elements, and DC sources (Siddique et al., 2021). Bana et al. (2020) has suggested the method of solar-PV MLI, which aims to improve power quality by harmonics reduction in various loads. There are three categories of classical or traditional MLI structures which are especially helpful to improve the output voltage level (Bana et al., 2020). In each modulation scheme is a different control mechanism for providing the voltage level by using traditional, conventional,

**Table 2** Assessment of fifteen level traditional MLI

Different types of multilevel inverter (MLI)	Total number of stage	Number of main diodes	Number of switches	Number of clamping diodes	Number of DC bus capacitor	Number of balancing capacitors
Switched Capacitor- (MLI) (Barzegarkhoo et al., 2016)	15 level	0	7	11	1	6
FC (MLI) (Thangamuthu, 2021)		28	28	0	14	91
Binary Ladder- (MLI) (Banaei et al., 2013)		0	6	0	6	0
Modified Ladder- (MLI) (Alishah et al., 2021)		0	4	0	3	0
NPC (MLI) (Fahad et al., 2021)		28	28	182	14	0
CH-B (MLI) (Palanisamy et al., 2022)		28	28	0	7	0
Conventional (MLI) (Abeera & Chandrahasan 2020)		3	12	6	3	0
Modular (MLI) (Bubovich & Ilya 2020)		3	7	0	3	0
Switched Series/Parallel- (MLI) (Tsunoda et al., 2014)		6	14	0	3	1
Proposed (SV-LI)		2	1	0	7	1

and modular MLI. The several classical and modified multilevel inverter drawbacks are listed as follows;

1. Traditional (NPC, FC, CH-B) and conventional multilevel inverter configurations are needed more than one isolated DC supply.
2. Efficiency, switching, and THD level is poor for real power transmission in traditional (NPC, FC, CH-B) and also conventional multilevel converters.
3. The basic output voltage frequency is a range up to 50 Hz, but the switching devices frequency is too high and the control circuit is complexity in traditional (NPC, FC, CH-B) multilevel converters.
4. Traditional converters (NPC, FC, CH-B) trigger a lot of harmonics and produce a high fluctuation in load voltage and analysis the effects of lower harmonics generated in conventional inverters. But more equipment and filters are needed for lower THD levels.
5. A large number of semiconductor devices are used in traditional inverters (NPC, FC, CH-B, and MMC) such as high rating switches, clamping diodes, and capacitors.
6. To maintain the level of balanced output voltage with MMC topology supplied with the capacitor, excess controllers are required.
7. Traditional inverters (NPC, FC, and CH-B) generate maximum output voltage is produced from half of the DC input voltage.
8. The MMC circuit does not require output filters, and the resulting pulse frequency is highly rated to avoid the need for a filter but the number of levels available within a multiple switching component. The literature review of multilevel inverter topologies is briefly described of reduces components such as a capacitor,

power switch, diode, and DC source, etc., as shown in Table 2. The sustainable energy technologies such as Solar-Photovoltaics (S-PV) and wind power have a key role to play for electricity generation. To minimize the pollution with low-cost interface multilevel inverters are increased to continuous power development. The conventional inverter topologies integrate with multiple levels using many clamping diodes, DC sources, clamping capacitor, bulky filters, and may extend establishment zone because of growth in converter cost, and its convoluted control circuits are not preferable. The MLI or electrical DC voltage source inverters leads in two cases: (1). Symmetrical model, (2). Asymmetric model.

The asymmetric model of the inverter has been designed a high number of voltage level achieved with more number of bulky switches, and driver circuits for generating various levels. Here, the symmetrical model inverter minimum number of voltage levels is to achieve the maximum number of output. Now symmetrical MLI topologies, DC powers are contained an equivalent output voltage which guarantees equal magnitude and it is the same magnitude of voltage that is forwarded into a series-connected inverter circuit. The multilevel power converter has been introduced as high power to medium power applications. Even though the conventional and modular multilevel PWM inverters are widely used in industrial applications.

The PV input sources fed into the Double Lift Converter (DLC) is operated with maximizing DC voltage. It converts DC output voltage into SV-LI staircase output. The high number of voltage levels is achieved by the maximum number of switches and gate driver circuits that are needed for all multi-inverting level accomplished in asymmetric inverters. Now, the symmetric proposed voltage-lift multilevel inverter less number of multiple levels are applied to enhance the maximum output voltage.

Dhivya and Renoald (2017) have suggested reducing the discharging negative sequence of voltage or current supply across the load terminals are enhanced to improve P-Q with the help of DC-link capacitors (Dhivya and Renoald, 2017). They primarily differ in size and location, and also unique in several system parameters and characteristics. The design and improvement of the proposed inverter are elucidated under the following steps:

1. Selection of Solar PV.
2. MPP-based standalone-PV system.
3. Double-Lift Converter (DLC).
4. Design of SV-LI.

### 3 Design of Proposed Inverter

The Proposed SV-LI consists of single MOSFET switch  $S_2$ , 2-freewheeling diodes, and 7-parallel main switching capacitors ( $C_6 - C_{12}$ ) combined with SPM-TS (Single Pole Multi Terminal Switch) as shown in Fig. 2a. The DC-link capacitor is combined with SPM-TS (or) one pole eight terminal Wiper pole switch split into DC voltage convert multilevel staircase output as shown in Fig. 2b. The solar-PV array module type is normally designed as sun-power 305 Watts. The design of a single-phase inverter depends upon the input rating of Solar-PV. It contains the series-connected modules as per the string is 9, modules as per the number of cells are 96, and the parallel number as per string is 250. There are four Solar-PV arrays connected in single module parameters are adjusted to fit the following under Standard-Test Conditions (STC): Irradiance-1000 W/m<sup>2</sup>, Diode Quality factor (Qd), and cell temperature-25 °C as shown in Table 3.

#### 3.1 Selection of Solar-PV

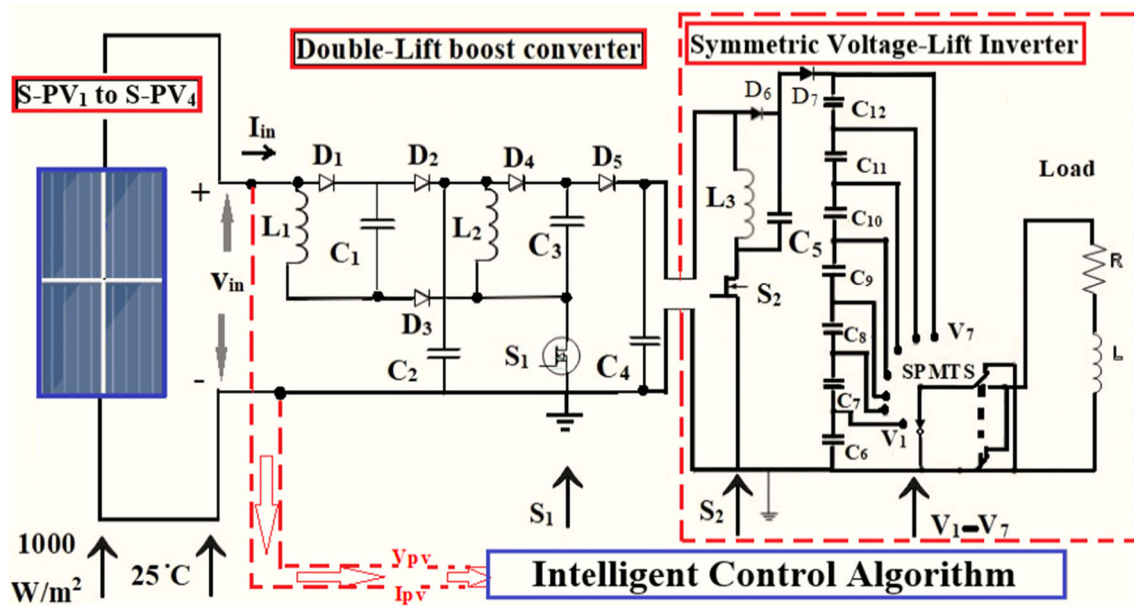
The PV array consists of numbers as per parallel ( $N_{par}$ ) module strings are connected in parallel, and each PV array consists of Numbers as per series ( $N_{ser}$ ) module strings are connected in series. The S-PV<sub>1</sub> to S-PV<sub>4</sub> made by supply are open-circuit voltage ( $V_{oc}$ )-64.2 V, short-circuit current ( $I_{sc}$ )-5.96 A, the voltage at maximum power point ( $V_{mp}$ )-54.7, current at maximum power point ( $I_{mp}$ )-5.58. In the photovoltaic arrays (SPV<sub>1</sub>-SPV<sub>4</sub>) PV terminal current is not uniform to the constant MPP when the panel output voltage is lowered due to cloudy conditions during checking of PV-module in the day time. The MPP rule assists with the optimization algorithm is supported to generate the Duty Cycle (D). The basic formula for maximum efficiency ( $\eta$ ) calculation of PV cell is given by the Eq. (1), and the ratio of maximum output power to the incident S-PV power using by radiation flux time for the area (A).

$$\eta = \frac{P_{max}}{E \cdot A_{cell}} \quad (1)$$

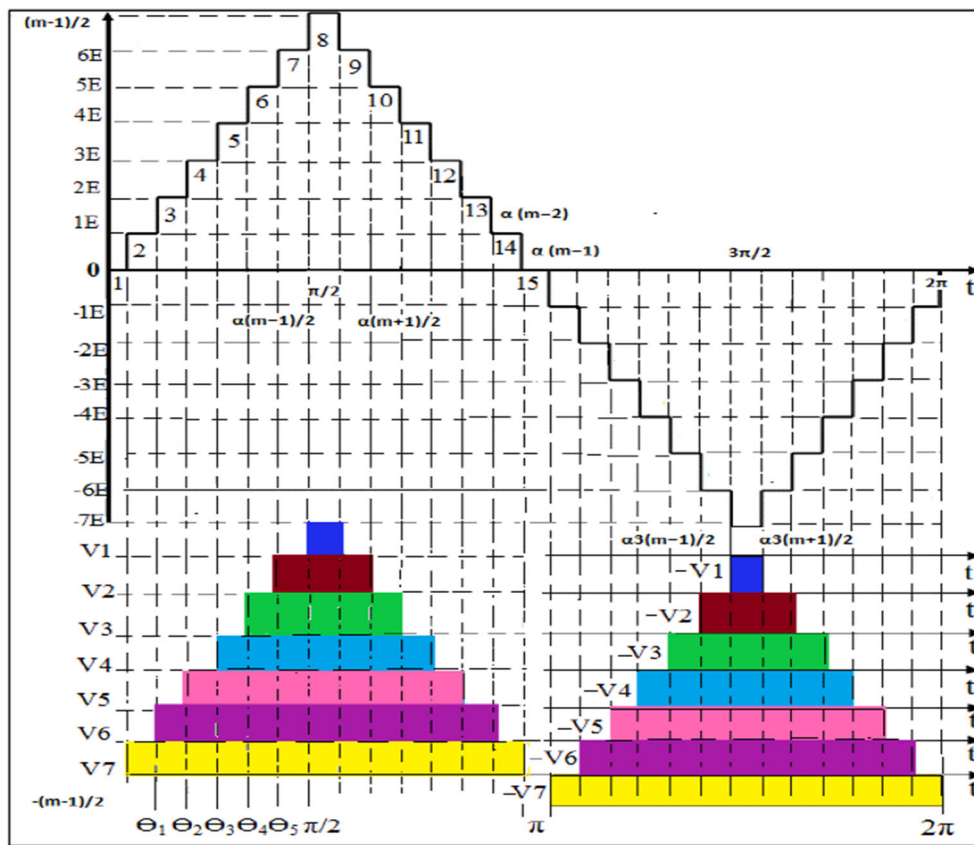
The number of PV modules wired in a series by the maximum voltage ( $V_{max}$ ) equals to multiplied with maximum system voltage 4 (PV panel) \* 16.07 = 64.28 V maximum PV-input voltage and current 5.96 A. This can increase the overall efficiency of the system. The basic formula for maximum PV cell efficiency ( $\eta$ ) is given by the ratio of output power to the occurrence PV maximum power, and the Filled Factor (FF) is verified by the equation as shown in (2) to (4).

$$P_{max} = V_{oc} \times I_{sc} \times FF \quad (2)$$

The S-PV array modules are used in the number of cells as per module (i.e., 96\*0.18 V = 17.28 V,  $P_{in}$  = 17.28 V ×



(a) Proposed Symmetric Voltage-Lift Inverter



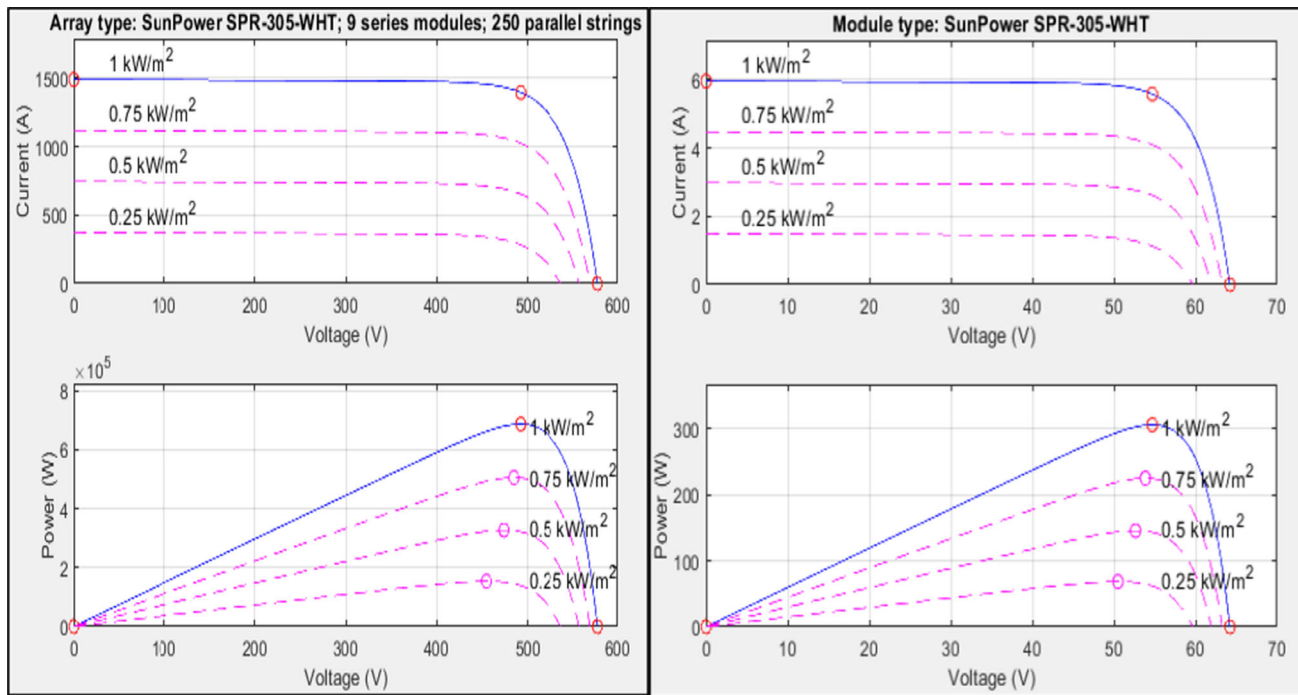
(b) 15-level output voltage waveform

Fig. 2 a Proposed symmetric voltage-lift inverter. b 15-level output voltage waveform



**Table 3** Deficiency report of PV- module MPP & parameters

Module specification under STC condition	Excluding MPP- Sun Power 305 Watts	Including MPP-Sun Power 305 Watts	S-PV module	Parameters
Maximum power ( $P_{max}$ )	295–300 W	305 W	Series resistance	$R_s$ -0.037998 $\Omega$
Voltage at $P_{max}$ ( $V_{mp}$ )	51 V	64.2 V	Parallel resistance	$R_p$ -993.51 $\Omega$
Current at $P_{max}$ ( $I_{mp}$ )	4.95 A	5.96 A	Saturation current	$I_{sat}$ -1.1753 $e^{-08}$ (A)
Open-circuit voltage ( $V_{oc}$ )	59.5 V	54.7 V	Reference photo	$I_{ph}$ -5.9602 (A)
Short-circuit current ( $I_{sc}$ )	4.51 A	5.58 A	Diode factor	$Q_A$ -1.3



**(a) Solar irradiation for array type**

**(b) Solar irradiation for module type**

**Fig. 3** a Solar irradiation for array type. b Solar irradiation for module type

1.01 A = 17.45 W) connected to the DLBC converter, which is operated and lift a voltage encouraged into the SV-LI. The S-PV array module is usually projected as S-PV<sub>1</sub>, S-PV<sub>2</sub>, S-PV<sub>3</sub>, and S-PV<sub>4</sub> made by supply 64.2 V and 5.96 A. The PV cell modules are connected as followed by two combinations of series and parallel modules. The single PV array maximum open-circuit voltage  $V_{oc}$  -17.28 V, and short circuit current  $I_{sc}$ -1.96A.

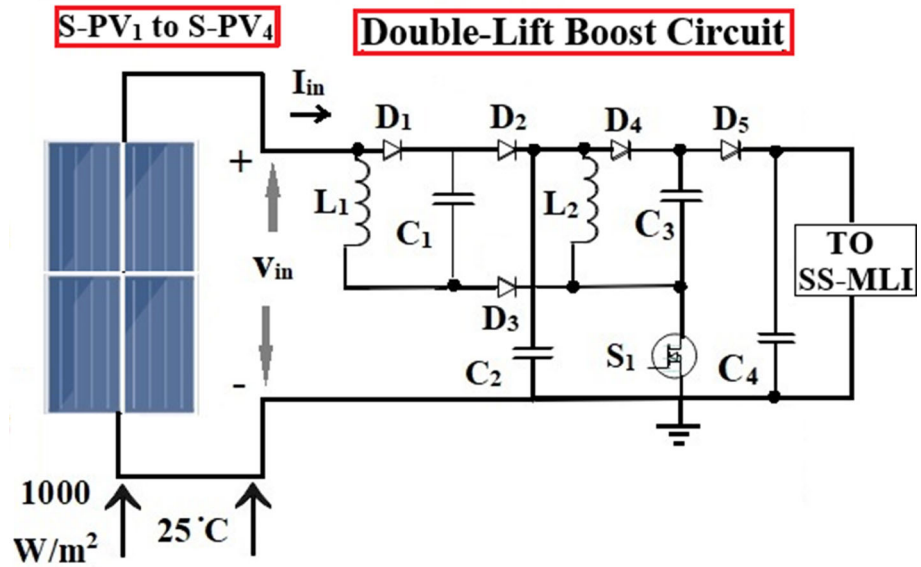
$$\text{Fill Factor(F.F)} = \frac{P_{in}}{V_{oc} \times I_{sc}} \tag{3}$$

$$\eta = \frac{V_{oc} I_{sc} F F}{P_{in}} \tag{4}$$

The MPP-based PV panel installations are considered in two methods: 1. Grid-connected S-PV model, 2. Standalone S-PV model. The standalone system is an automatic small-

scale PV system that produces electrical power to charges capacitor banks or battery banks during day time. The need for several sources on the input side of the converters is fed into MLI, that makes the multiple control and complexity issues should be created in MLI topology. Therefore, the PV installations may be preferable in residential, commercial or industrial, utility-scale, ground-mounted, rooftop-mounted, and wall-mounted or floating, etc. The MPP algorithm is used to extract the maximum power available from the PV module under certain conditions using Perturb and Observe (P&O) technique. In PV module voltage, which can produce the maximum power is referred to as the MPP or peak voltage. The maximum solar irradiation is variable with cell temperature in voltage, current, and solar power as the graph shows in Fig. 3a)and b.

Fig. 4 Double-lift circuit



### 3.2 Design of Double-Lift Boost Converter (DLBC)

The DLBC is modified from a step-up boost converter. Vanchinathan et al. (2021) have modified the DC-DC boost circuit, it consists of a coupled inductor, filters, charge pump capacitor, and active clamper circuit (Vanchinathan et al., 2021). These all components are more complexity of the control and complicated in the power circuit. Here, the (DC-DC) same method is revised so far, show that the output voltage is two times higher than the input voltage source  $V_1$ , but the requirement is much needed to reduce in module structure. Therefore, the proposed DLBC present with the minimum number of devices are required as shown in Fig. 4

Input voltage source ( $V_{in}$ ) for the converter is roughly around 64.2V, 5.96A, The performance of DLBC yields the output voltage is roughly around ( $V_{out}$ ) 128–130V<sub>dc</sub> calculated for both theoretically and practically. Which was improved by two significant parameters as namely inductors ( $L_1, L_2$ ) and capacitors ( $C_1, C_2$  &  $C_3$ ). As per the operation of PV-grid connected converter depending on the device type, because the sharing of AC amplitude in voltage arrives at the PV modules. In this stage, the single-phase transformer less converter is passed half of the load voltage with the help of PV modules. The parameters of DLBC are verified by the equation shows in (6) to (13). When the capacitor voltage  $V_{C1}$  is charged by input source ( $V_{in}$ ), in the stable state equation (Voltage across capacitor  $V_{C1} = V_{in}$ ) as shown in (11 & 14), that the voltage rise is across the  $C_1$ , and the voltage is indicated  $V_1$  as shown in the equation (5),

$$V_1 = \frac{2 - K}{1 - K} V_{in} \tag{5}$$

Here k-constant value,

$$\Delta I_L = (2\% \text{ to } 5\%) * I_{out(max)} * \frac{V_{out}}{V_{in}} \tag{6}$$

$$L = \frac{V_{in} \times (V_{out} + V_D - V_{in})}{\Delta I_L \times f_s \times (V_{out} + V_D)} \tag{7}$$

The capacitor voltage  $V_{C2}, V_{C3}$ , and  $V_{C4}$  are charged by  $V_1$  as shown in Eqs. (15)–(17). When current passing through Inductor  $L_2$  with increased voltage  $V_1$ , switch ( $S_1$ ) is in ON mode ( $KT$ ). When it decreases with the voltage level ( $V_{out} - 2V_{in}$ ), during the switch  $(1 - k) T_{off}$  period, the ripple of the inductor current ( $iL_2$ ) is,

$$\Delta iL_2 = \frac{V_1}{L_2} KT + \frac{V_0 - 2V_1}{L_2} iL_1(1 - K)T \tag{8}$$

$$\Delta iL_1 = \frac{V_{in}}{L} KT \tag{9}$$

$$T = \frac{1}{f} \tag{10}$$

The inductor current ( $iL_1, iL_2$ ) are determined by using equation numbers (8) & (9), then Eqn. 5, 7, 9, & 10 substitute in the Eq. 11. The converter circuit output is evaluated by  $D$  in the equation as shown in (12).

$$\Delta V_C = (2\% \text{ to } 5\%) * V_{out(max)} * \frac{I_{out}}{I_{in}} \tag{11}$$

$$D = \frac{V_{out}}{V_{in} + V_{out}} \tag{12}$$

The equation numbers (11) & (12) are substituted in Eq. (13).

$$C = \frac{I_{(out)} * D}{f_s * \Delta V_{out}} \tag{13}$$



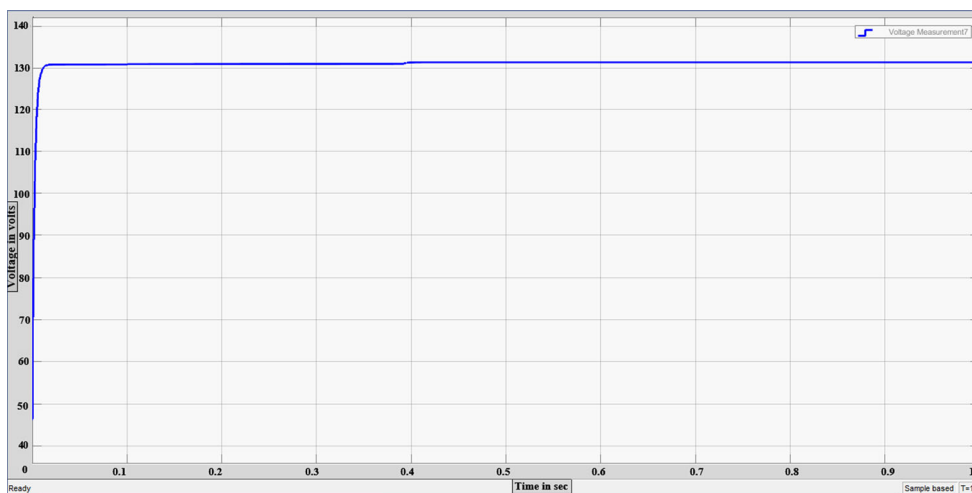


Fig. 5 Double-lift converter DC-output

The effect of capacitor  $C_1$  during switching off period;

$$\Delta V_{C1} = \frac{1}{f * R * C_1} \times V_1 \tag{14}$$

The effect of capacitor  $C_2$  during switching on period;

$$\Delta V_{C2} = \frac{K}{f * R * C_2} \times V_1 \tag{15}$$

The effect of capacitor  $C_3$  during switching off period;

$$\Delta V_{C3} = \frac{1}{f * R * C_3} \times V_0 \tag{16}$$

The effect of capacitor  $C_4$  during switching on period;

$$\Delta V_{C4} = \frac{K}{f * R * C_4} \times V_0 \tag{17}$$

where  $K$  is the duty cycle, and the voltage transfer gain as verified by the Eq. (18);

$$\text{Gain} = \frac{V_{in}}{V_0} \tag{18}$$

The maximum induced output voltage and currents from MPP passing through the next stage of converters as shown in Fig. 5.

### 3.3 Symmetric Voltage-Lift Inverter

An extremely significant element within this design of SV-LI, which is the number of required switches against the required voltage in the multilevel waveform. It generate fifteen level output (+ 7 V 0 & - 7 V), (+ 6 V 0 & - 6 V), (+ 5 V 0 & - 5 V), (+ 4 V 0 & - 4 V), (+ 3 V 0 & - 3 V), (+ 2 V 0 & - 2 V), and (+ 1 V 0 & - 1 V). With this, connection expressed

SV-LI number of multiple levels has been improved as point out below. Where (C) is specified the number of capacitors adding with only one switch used in the MLI equation as shown in (19),

$$N \text{ level} = 2 * \text{Capacitor}(C) + 1 * \text{Switch}(S), \tag{19}$$

$$2 * (3)C + (1)S = 7 \text{ levels} \tag{20}$$

$$2 * (7) C + (1)S = 15 \text{ levels} \tag{21}$$

$$2 * (10)C + (1)S = 21 \text{ Level} \tag{22}$$

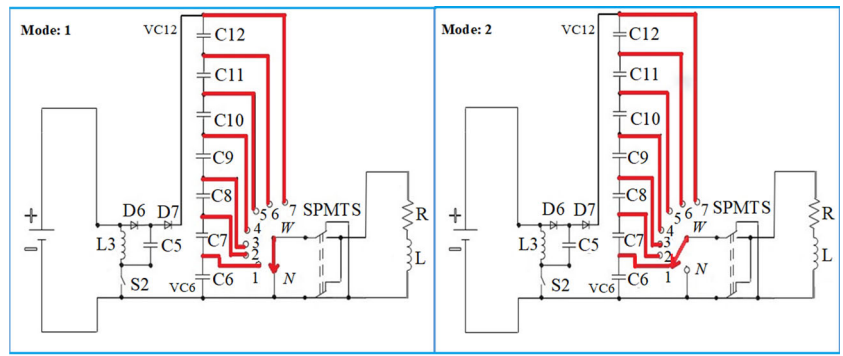
$$2 * (12)C + (1)S = 25 \text{ Level} \tag{23}$$

$$2 * (17)C + (1)S = 35 \text{ Level} \tag{24}$$

$$2 * (22)C + (1)S = 45 \text{ Level} \tag{25}$$

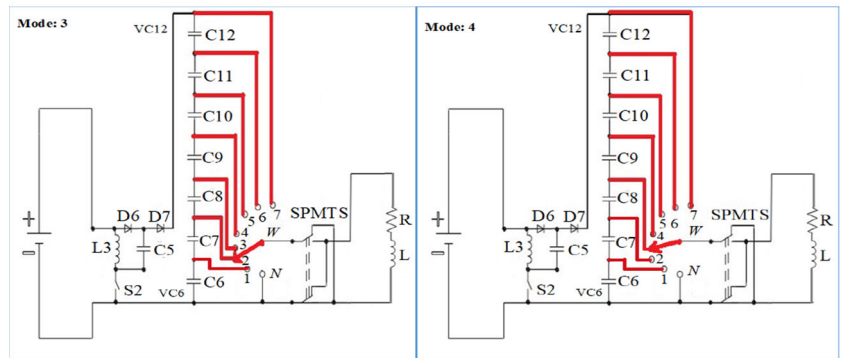
Proposed symmetric voltage lift inverter topology is a less number of equipments, and less voltage stress across the capacitor unit or main capacitor bank. The capacitor unit ( $C_6-C_{12}$ ) across the SPM-T switch is developed by 15 level output as shown in the Eq. (21). The main capacitor is combined with SPM-T switch, which is used to divide the MLI output voltage into fifteen levels. The capacitor band switch (or) SPM-T switch Turn on positive charging output terminal voltage from  $V_7, V_6, V_5, V_4, V_3, V_2, V_1, V_0$ , and negative discharging output terminal voltage turn off are  $-V_1, -V_2 -V_3, -V_4, -V_5, -V_6, \& -V_7$ , respectively, in SV-LI. The advantages of proposed topology are: (1) generates a maximum number of multilevel outputs increased by using multiple capacitors ( $C_6$  to  $C_{12}$ ) without increasing the number of additional switches, and circuit topology, (2) a Minimum number of semiconductor devices are used in SV-LI, (3) Reducing

**Fig. 6** a Mode: 1. b Mode 2.  
c Mode: 3. d Mode: 4. e Mode:  
5. f Mode: 6. g Mode: 7.  
h Mode: 8



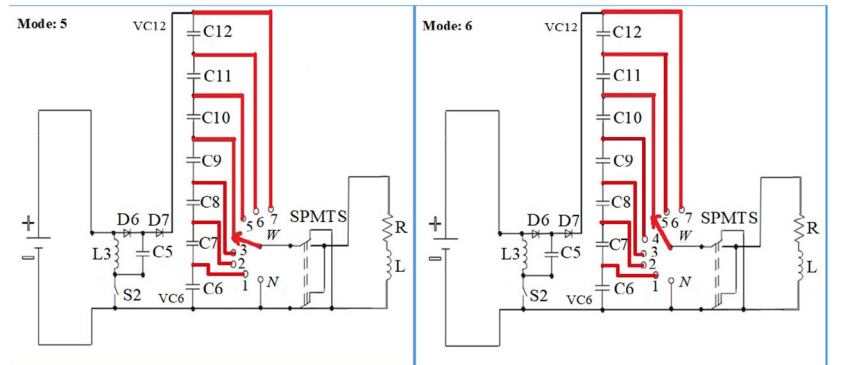
**(a) Mode: 1**

**(b) Mode 2**



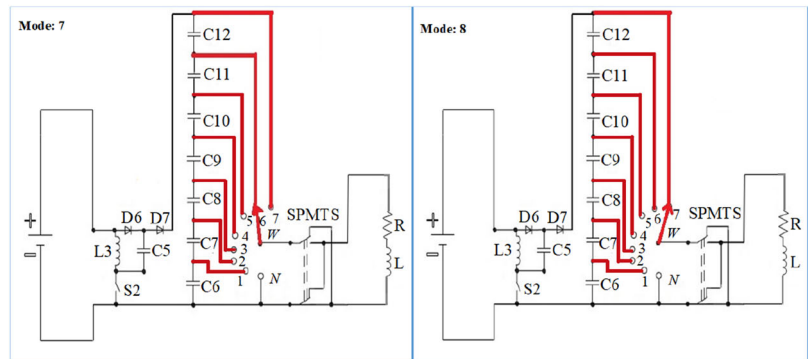
**(c) Mode: 3**

**(d) Mode: 4**



**(e) Mode: 5**

**(f) Mode: 6**



**(g) Mode: 7**

**(h) Mode: 8**

**Table 4** SV-LI switching method

Main capacitor-single pole multi terminal switch (SPMT) positive half cycle & negative half cycle (0–90°) to (90°–180°) & (180°–270°) to (270°–360°)	Total No. of level	Switch ON state	Output voltage level expression	Wiper pole band switch timer with seconds
Mode:1 ( $V_0$ )	1	$N$	$V_0$	0
Mode:2 ( $V_1$ )	2	$+ 1/1 V_{dc}$	$V_{C6}$	1 (5-Seconds)
Mode:3 ( $V_2$ )	3	$+ 1/2 V_{dc}$	$V_{C6} + V_{C7}$	1–2 (10 S)
Mode:4 ( $V_3$ )	4	$+ 1/3 V_{dc}$	$V_{C6} + V_{C7} + V_{C8}$	1–2–3 (15 S)
Mode:5 ( $V_4$ )	5	$+ 1/4 V_{dc}$	$V_{C6} + V_{C7} + V_{C8} + V_{C9}$	1–2–3–4 (20 S)
Mode:6 ( $V_5$ )	6	$+ 1/5 V_{dc}$	$V_{C6} + V_{C7} + V_{C8} + V_{C9} + V_{C10}$	1–2–3–4–5 (25S)
Mode:7 ( $V_6$ )	7	$+ 1/6 V_{dc}$	$V_{C6} + V_{C7} + V_{C8} + V_{C9} + V_{C10} + V_{C11}$	1–2–3–4–5–6 (30S)
Mode:8 ( $V_7$ )	8	$+ 1/7 V_{dc}$	$V_{C6} + V_{C7} + V_{C8} + V_{C9} + V_{C10} + V_{C11} + V_{C12}$	1–2–3–4–5–6–7 (35 S)
Mode:9 ( $V_6$ )	9	$- 1/6 V_{dc}$	$-(V_{C6} + V_{C7} + V_{C8} + V_{C9} + V_{C10} + V_{C11})$	1–2–3–4–5–6 (40 S)
Mode:10 ( $V_5$ )	10	$- 1/5 V_{dc}$	$-(V_{C6} + V_{C7} + V_{C8} + V_{C9} + V_{C10})$	1–2–3–4–5(45 S)
Mode:11 ( $V_4$ )	11	$- 1/4 V_{dc}$	$-(V_{C6} + V_{C7} + V_{C8} + V_{C9})$	1–2–3–4 (50S)
Mode:12 ( $V_3$ )	12	$- 1/3 V_{dc}$	$-(V_{C6} + V_{C7} + V_{C8})$	1–2–3 (55 S)
Mode:13 ( $V_2$ )	13	$- 1/2 V_{dc}$	$-(V_{C6} + V_{C7})$	1–2 (60 S)
Mode:14 ( $V_1$ )	14	$- 1/1 V_{dc}$	$- V_{C6}$	1 (65 S)
Mode:15 ( $V_7$ )	15	$V_0$	$V_0$	0

voltage stress across the semiconductor devices, and (4) the symmetrical SV-LI strategy utilizes single MOSFET switch and capacitor energy banks connected with the ground, so that the S-PV source voltage level is increasing and this can generate a higher incentive in MLI output voltage. The SV-LI differ from conventional inverters, as an individual inverter fed into four PV modules are series-connected in a single S-PV module, this may improve the overall efficiency of the system.

### 3.4 Modes of Operation

In this regards, the mode of process SV-LI is operated under one complete cycle (0°–360°), which is operated (0–180°) is positive half cycle switching and (180°–360°) is negative half cycle switching method.

#### 3.4.1 Positive Half Cycle of SV-LI (0–180°)

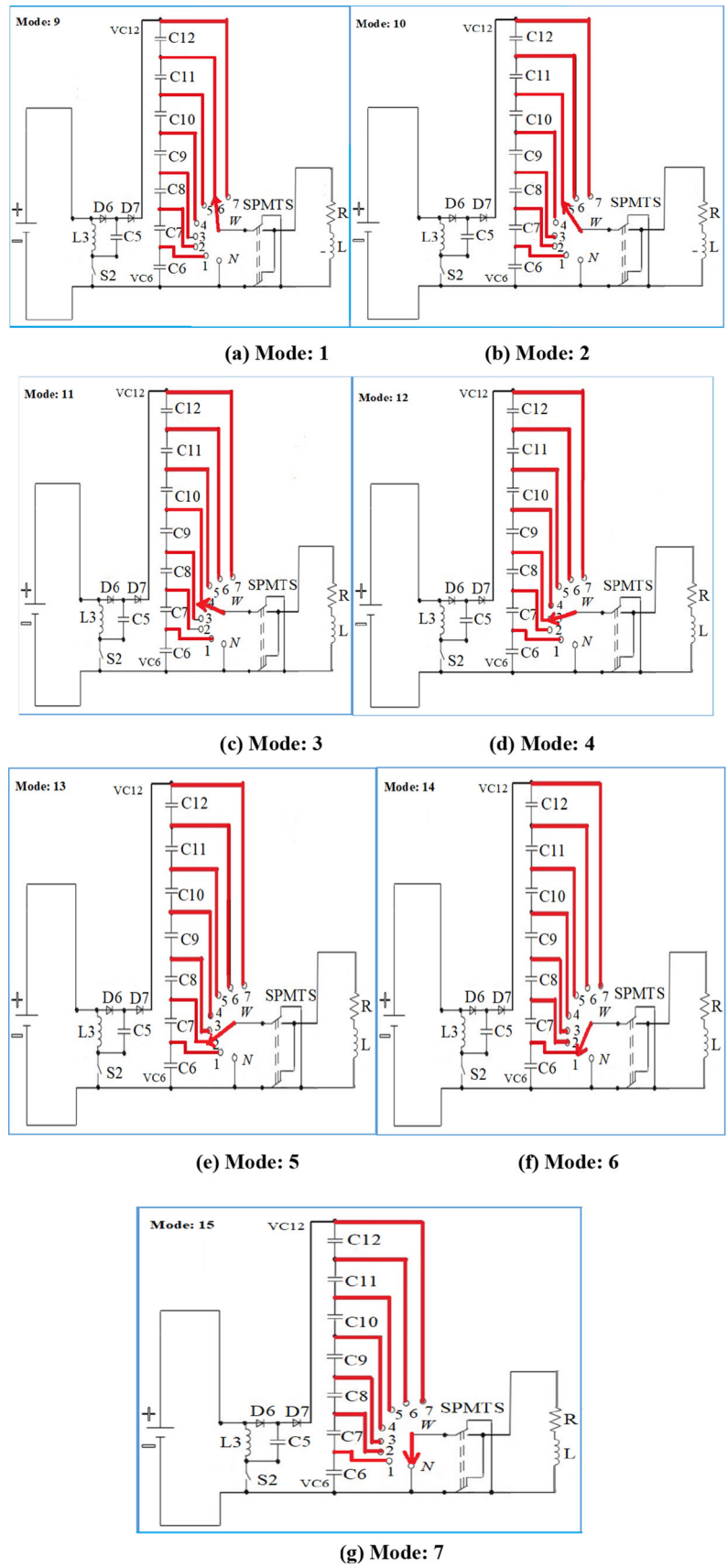
The Symmetric MLI is operated, when the inverter switch  $S_2$  is ON. The inductor ( $L_3$ ), and capacitor ( $C_5$ ) are charged by the DLBC (DC) supply. The output voltage switch position ( $V_0$ ) is in a positive half cycle (0–90° & 90°–180°) mode, when it is at the node in between  $D_7$  (diode) and  $C_{6, 12}$  (capacitor), there will be a potential voltage across the capacitor  $V_{C6}$  and  $V_{C12}$ . When the switch is ON condition, the wiper pole

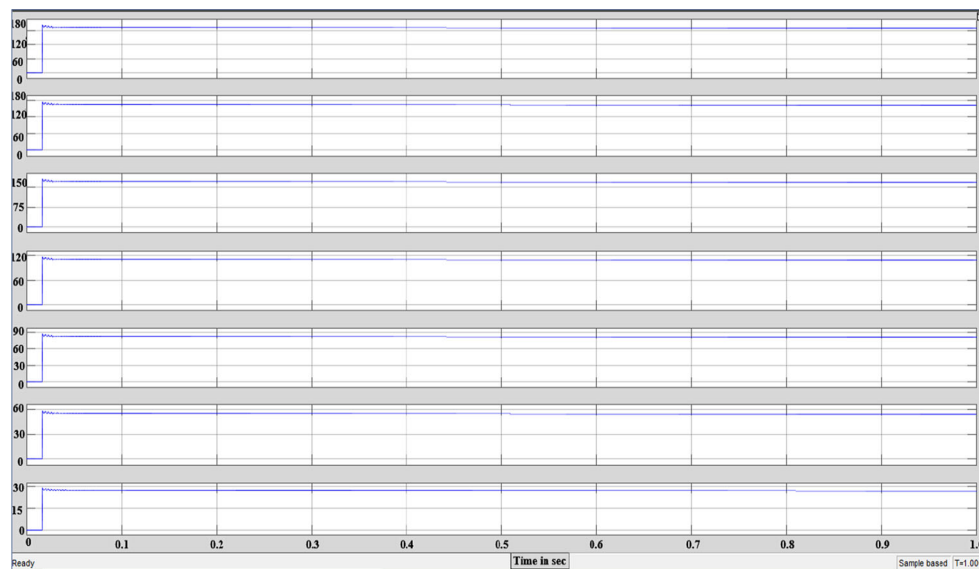
terminal voltage ( $V_{WN}$ ) is equal to the  $V_{dc}$  switching (ON) period. One wiper pole switch is one pole multi-terminal switch; it is also called as SPM-T.

$V_0$  (mode: 1) = 0 (neutral) when it is at the node in between  $C_6$  and  $V_0$ , there will be a potential voltage across the output will be followed by Two Pole Two Through (2P2T) switch, once the 2P2T switch is closed, that forward output voltage will be transfer to the next state of load ( $R, RL$ ) as shown in Fig. 6a. The SV-LI Switching methods are shown in Table 4. The same process should be followed,

- $V_1$  (mode:2) =  $+ 1/1V_{dc}$  when it is at the node in between the capacitor  $C_7$  and  $C_6$ , there will be a potential voltage rise across the capacitor  $V_{C6}$  and finally, the SPM-T switch is at a point  $V_0$ , that shows the voltage path depicted in Fig. 6b
- $V_2$  (mode:3) =  $+ 1/2V_{dc}$  when it is at the node in between the capacitor  $C_8$  and  $C_7$ , there will be a potential voltage rise across the capacitor  $V_{C7}$ , that shows the voltage path is given in Fig. 6c
- $V_3$  (mode:4) =  $+ 1/3V_{dc}$  when it is at the node in between the capacitor  $C_9$  and  $C_8$ , there will be a potential voltage rise across the capacitor  $V_{C8}$ , that shows the voltage path is given in Fig. 6d
- $V_4$  (mode:5) =  $+ 1/4V_{dc}$  when it is at the node in between the capacitor  $C_{10}$  and  $C_9$ , there will be a potential voltage

**Fig. 7** a Mode: 1. b Mode: 2.  
c Mode: 3. d Mode: 4. e Mode:  
5. f Mode: 6. g Mode: 7





**Fig. 8** Capacitor across switching voltage in SV-LI

rise across the capacitor  $V_{C9}$  as shows the voltage path given in Fig. 6e.

- $V_5$  (mode:6) =  $+ 1/5V_{dc}$  when it is at the node in between the capacitor  $C_{11}$  and  $C_{10}$ , there will be a potential voltage rise across the capacitor  $V_{C10}$ , that shows the voltage path is given in Fig. 6f.
- $V_6$  (mode:7) =  $+ 1/6V_{dc}$  when it is at the node in between the capacitor  $C_{12}$  and  $C_{11}$ , there will be a potential voltage rise across the capacitor  $V_{C11}$  as shows that the voltage path is given in Fig. 6g.
- $V_7$  (mode: 8) =  $+ 1/7 V_{dc}$  under the condition, 2P2T switch is closed. When it is at the node in between  $D_7$  (diode) and  $C_{12}$  (capacitor), there will be a potential voltage rise across the capacitor  $V_{C12}$  as shows in Fig. 6h. It is taken as the accurate charging output voltage for the positive half cycle of the load. The same process should be followed in the next positive quadrant cycle of the load ( $90^\circ$ – $180^\circ$ ).

### 3.4.2 Negative Half Cycle of SV-LI ( $180^\circ$ – $360^\circ$ )

The output voltage switching position ( $- V_6$ ) is in negative half cycle mode when it is at the node in between  $N$  (neutral) and  $C_{11}$ , there will be a negative potential voltage rise across the capacitor ( $- V_{C6}$ ), which is named as, mode: 9 =  $- 1/6V_{dc}$ , when it is at the node in between the capacitor  $C_{10}$ – $C_{11}$ , there will be a negative potential voltage rise across the capacitor ( $- V_{C11}$ ), that shows in voltage path is given in Fig. 7a.

- $- V_5$  (mode: 10) =  $- 1/5V_{dc}$ , when it is at the node in between the capacitor  $C_9$ – $C_{10}$ , there will be a negative

potential voltage rise across the capacitor ( $- V_{C10}$ ), that shows in voltage path is given in Fig. 7b.

- $- V_4$  (mode: 11) =  $- 1/4V_{dc}$ , when it is at the node in between the capacitor  $C_8$ – $C_9$ , there will be a negative potential voltage rise across the capacitor  $- V_{C9}$ , that shows in voltage path is given in Fig. 7c.
- $- V_3$  (mode: 12) =  $- 1/3V_{dc}$ , when it is at the node in between the capacitor  $C_7$ – $C_8$ , there will be a negative potential voltage rise across the capacitor ( $- V_{C8}$ ), that shows in voltage path is given in Fig. 7d.  $- V_2$  (mode: 13) =  $- 1/2V_{dc}$ , when it is at the node in between the capacitor  $C_6$ – $C_7$ , there will be a negative potential voltage rise across the capacitor ( $- V_{C7}$ ), that shows in voltage path is given in Fig. 7e.
- $- V_1$  (mode 14) =  $- 1/1V_{dc}$ , when it is at the node in between the capacitor  $C_6$ – $N$  (neutral), there will be a negative potential voltage rise across the capacitor ( $- V_{C6}$ ) and  $V_0$ , that shows the voltage path is given in Fig. 7f. Mode-15 is the operating point as neutral. When it is at the node in between  $N$  (neutral) and  $C_6$ , there will be potential voltage rise across the capacitor ( $- V_{C6}$ ), It will be followed 2P2T switch, once that switch is closed, the reverse output voltage will be transfer to the next state of load ( $R, RL$ ) shown in Fig. 7g. The capacitor switching voltage across the SPM-T switch as shown in Fig. 8. The same process should be followed in the next negative quadrant cycle of the load ( $270^\circ$ – $360^\circ$ ).



## 4 Intelligent Techniques Implementation for Solar FED SV-LI

The fuzzy electronics techniques are commonly used in digital electronics and provide adaptive control of improved system performance. The real power from S-PV is extracted with the help of MPP-algorithm, and it's fed into DC-DC/AC converters. The PV cell modeling and design is considered for the proposed SV-LI, in this section is described in details of the fuzzy-based intelligent such PI, MPP-based controller. It has been explained and detailed about the control scheme of the proposed MLI to get expected multilevel output. The proposed inverter work is suitable for renewable energy application. Fuzzy-based MPP method has been applied for S-PV panel application. Under the different environments, the PV panel is operated in four different variable irradiation (Max-1000 w/m<sup>2</sup>), and temperature (up to-60 °C) conditions. The proposed system was applied MPP associate PI controller. The PV inverter module to associate with MPP-device is highly essential for produce maximum voltage gain, and the required SV-LI output should be measured across in the N-LL condition. Therefore, fuzzy-based techniques are implemented in the following steps;

1. Fuzzy Logic (FL)-based controller design
2. Fuzzy-Proportional Integral (F-PI)-based controller design
3. MPP-Fuzzy based controller design (MPP-F)
4. Artificial Intelligent Techniques (AIT)

### 4.1 Fuzzy Logic Implementation

This section improved P-Q with help of fuzzy intelligent techniques, and it is associated with MPP for controlling the PV output voltage to achieve as smooth control in a closed-loop manner. To attain the maximum power (305 W) is achieved by PV array in a standalone approach. The P-Q improvement is to provide in a closed-loop manner, and the PV will be rapidly to generate the voltage with minimum harmonics level. Furthermore, it can be developed with the generated pulses to the next stage of the converter, and also perform as a charge controller of the module.

#### 4.1.1 Fuzzy Logic Controller Design

The digital electronics is assists a vital role in FL strategy for making the process to be controlled and simplify the system model. It can minimize the complex problem such as linear and nonlinear problems. A fuzzy control system is a real-time expert system that implements part of the expertise of a human operator or engineering digital process, and its digital logic on discrete values of either 0 or 1. The FL allows the knowledge to be expressed with the subject concepts such

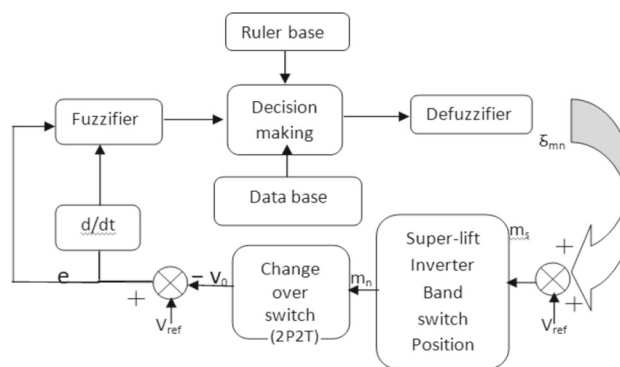


Fig. 9 Block diagram of FL-controller scheme

as very short, bright, and mapped into the exact numerical ranges.

The design of Fuzzy Interface System (FIS) is divided into five modules: fuzzifier, database, rule based, decision maker, and defuzzifier presented as shown in Fig. 9. The fuzzy offers a remarkably simple way to draw definite conclusions from ambiguous, vague, or imprecise details. Therefore, the development of rules is written in MATLAB code and translates with the help of FL tool-box. The FIS output always depends on the irrespective of the input, which is necessary to control the fuzzy crisp variables, and it has been explained the detailed about control scheme of SV-LI to get expected multilevel output. The FIS-defuzzification unit is transformed the fuzzy variables into crisp variables, the most important features of FIS are a less intensive design of mathematical requirements, and widely used in machine logic control.

#### 4.1.2 Implementation Procedure and Parameterization

The environmental benefits and economic dimension is required to S-PV with the new power electronic inverter topology by using an intelligent method such as FL-controller to simulate the MATLAB platform. The RMS productivity voltage of fifteen level SV-LI is developed from fuzzy control rules created based on the following criteria:

1. The FL is developed by fuzzy logic toolbox. The different variable that represents the content of the preceding rules are chosen as an error, it is denoted by (e). The process of state variable representing the rule-consequent content is chosen as the control output, it is denoted by (u). These variables are described by triangular waveform, once the references are to make minute change in MI is furthermore improvement in output multilevel waveform, the error signal is discriminate in between the output and set-point as shown in Fig. 10a.
2. The output voltage of SV-LI is compared with reference sinusoidal multilevel output waveform to compute the error (E) =  $V_{ref} - V_{out}$ . The error signal (e) is given

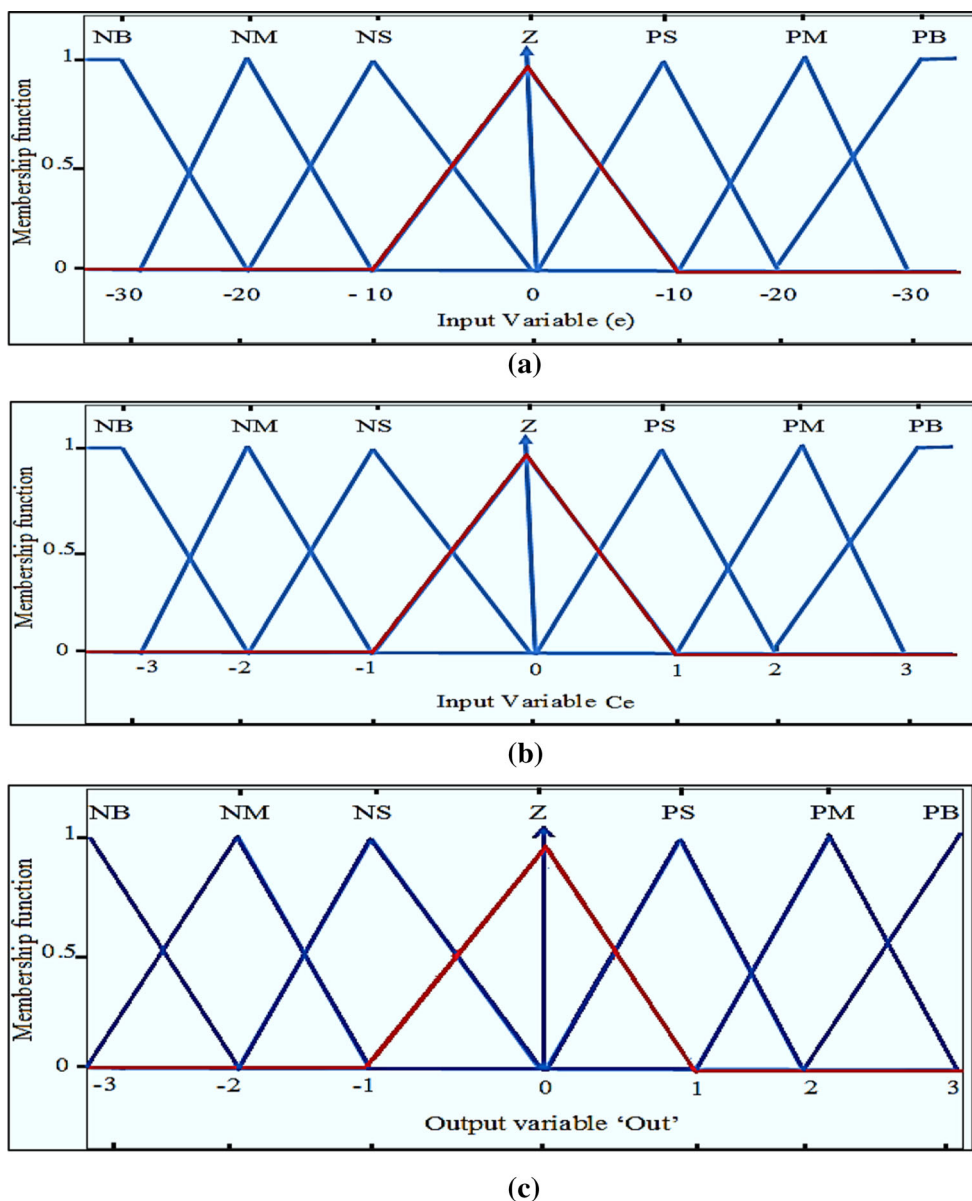


Fig. 10 Membership function a Error signal b Change of error signal c Reference signal

input of the FL controller, the change of MI is essential to be varied in a large level, and bring the output to the reference is quick. The Membership Function (MF) of changes of the error signal Mamdani as shown in Fig. 10b.

- There are two inputs in FL, (i) Error signal, (ii) Change of error signal. These two input signals are converted into FL membership value as shows in the given Eq. (26) and (27). Once the SV-LI output is higher than the reference point, it changes of MI should be negative and vice versa. This result of the saturation level for limiting the minimal values of THD and the maximum level of multilevel voltage.

$$E(t) = r(t) - y(t) \tag{26}$$

$$E_r(t) = e(t) - e(t - 1) \tag{27}$$

where  $E$ -Error,  $E_r$ -Error rate, and these crisp values are separated into seven FL subset, it converts into fuzzy variables. The rate of conversion of error is calculated  $(COE) = E_n - E_{n-1}$  and the  $d/dt$  serves as the input attributes for the fuzzy controller. Where the  $V_0$  is the end result output voltage of SV-LI, the  $V_{reference}$  is the preferred output voltage and  $\delta_{mn}$  is change-over band switch position by the  $n$ th sampling instant, and the  $\delta_{mn}$  is updated the switch position commanding sig-

nal generate to the FL controller. It can be compared with a reference voltage ( $V_{ref}$ ) to generate the optimum switching angle ( $\theta$ ) and switching signal ( $m_s$ ). The reference membership signal is shown in Fig. 10c.

Required PWM generation, which provides the appropriate gate signal to the multilevel inverter switch. The change-over switch-2P2T ( $m_n$ ) operation depends on the previous state of band switch position. The Fuzzification is direct record highlights for knowledge and profit alongside standard utilization. The fuzzification values are called as crisp value and it is used to develop the defuzzification procedure. The rules-based fuzzy systems are sequentially connected in software. To obtain correct productivity defuzzification has been performed in the fuzzy ruler view. The range of fuzzy variable depends on input and output parameters. It is described the fuzzy set with linguistic variables, and their membership functions. Based on the membership function, inputs to the FL controller are taken as a change in voltage error (CE), and change in current error (E). It is converted to the linguistic FL variables, as well as FL controller output for the duty cycle arrangements obtained in a fuzzy rules. Fuzzy rules play a major role in controller design. The principles are made from a fuzzy inference system using mamdani algorithm presented.

## 4.2 Fuzzy-PI Based Controller Design

The closed-loop simulation of FL-based controller is carried out SV-LI and DLBC. The PV power is extracted via (DC-DC) converter, and the duty cycle is varied as per MPP-based solar irradiation arrangements. The S-PV array modeling and design of the proposed system are described with fuzzy-PI based controller. The fuzzy surface and ruler views have been presented in the previous Sect. (7.1). In this section is focused on PI controllers decide and tuned by FL-controller according to the flowing reasons. (1). Control the output voltage error in MLI, (2). Control the output voltage frequency, (3). The transient response was enhanced in N-LL condition. There are two gain blocks incorporate in Simulink model, and it is a feed-forward path from the input PV source model fed with D-LC and multilevel inverter.

### 4.2.1 Implementation Procedure

PI controller switching point was tuned by FL controller. According to the system required for a fast dynamic, and transient response due to track the voltage for the reference value, settling, and low overshoot timing. Solar-PWM inverter has been operated with single-phase, and single input using for the fuzzy-tuned PI controller. Which is slowly minimized the fuzzy rules in distance rules method and it is compared to FIS using for fuzzy intelligent technics, and it specifies about the uncertainty of the 50%, 100% load variation using fuzzy-

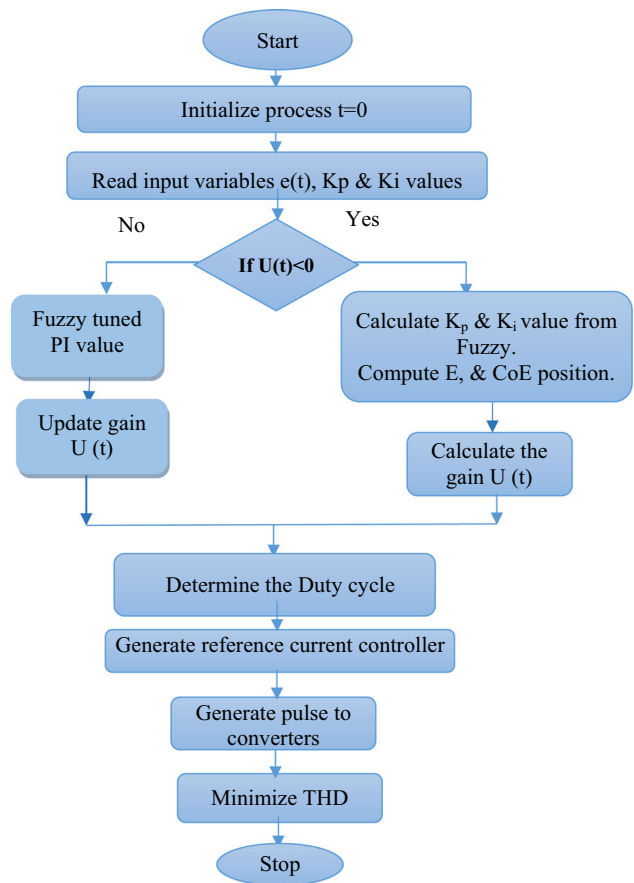


Fig. 11 Flowchart for estimation in Fuzzy-PI tuning parameters

tuned PI control methods. The following steps are described by the FL controller to calculated tuning parameters for the PI controller.

- Initial process  $T = 0$ , and read the input variables are  $K_p$  and  $K_i$  values. The PV voltage and current is two nonlinear input, and the system output is only one fuzzy output depicted into the PI controller.
- Calculate the  $K_p$ ,  $K_i$  values from the FL controller, and the quality of the error, according to the errors are fed to the FL-controller.
- The fuzzy-PI controller design is obtained in nonlinear control surface, that is why the reason behind the fuzzy tuning PI controllers are replaced by traditional FL-Controller. The control surface is adjusted FIS, such as rules, and MF, and it will be operating in mamdani-method to approach for FIS system.
- Define the rules in positive and negative MF with the Error (E) and Changes of Error (CoE). When the linear surface errors are easily solved by E & CoE. The control data is properly provided in nonlinear system, due to errors are too large in the closed-loop controller. Finally, Determine

**Table 5** Fuzzy-PI membership function of error (a)  
 K<sub>p</sub>-Membership function (b)  
 K<sub>i</sub>-Membership function (c)  
 Tuned parameter values

Output ( $K_p$ )	Error							
	NB	NM	NS	ZE	PS	PM	PB	
Change of error	(a)							
	NB	NB	NB	NB	NB	NM	NS	ZE
	NM	NB	NB	NB	NM	NS	ZE	PS
	NS	NB	NB	NM	NS	ZE	PS	PM
	ZE	NB	NM	NS	ZE	PS	PM	PB
	PS	NM	NS	ZE	PS	PM	PB	PB
	PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB	
Output ( $K_i$ )	Error							
	NB	NM	NS	ZE	PS	PM	PB	
Change of error	(b)							
	NB	NB	NB	NB	NB	NM	NS	ZE
	NM	NB	NB	NB	NM	NS	ZE	PS
	NS	NB	NB	NM	NS	ZE	PS	PM
	ZE	NB	NM	NS	ZE	PS	PM	PB
	PS	NM	NS	ZE	PS	PM	PB	PB
	PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB	
$K_p$	$K_i$	Sampling time in Sec			Maximum peak output voltage			
(c)								
0.21	0.60	0.5			203			
0.30	0.61	0.5			204.6			
1.45	5.59	0.5			205.01			
:	:	:			:			
2.6	4.63	0.5			206.6			
3.75	3.65	0.5			200.4			
7.6	2.61	0.5			210			
2.23	1.60	0.5			209.8			
1.13	0.63	0.5			210			
0.6	0.52	0.5			205.5			

the duty cycle and it generates pulses passing through the converters to minimize the harmonics level.

$K_p$ -Proportional gain,  $K_i$ -Integral gain,  $K_d$ -Differential gain, and  $Z$ -discrete value.

$$U(t) = K_p + K_i \frac{T_s * Z}{Z - 1} + K_d * \frac{Z - 1}{T_s * Z} \tag{28}$$

The PI controller is tuned by FL-based controller, the PI controller gain is tuned for multiple error signals for the solar variable irradiation. Figure 11 shows the estimation of fuzzy-PI tuning control procedure. The PI techniques are generating the error and reference signal, due to the variation of FIS. The  $K_p$  and  $K_i$  parameter values are described by the Eqs. (28), and (29). The discrete PI controller is tuned manually for different error values to regulate multilevel output voltage by FL based controller. Where  $T_s$ -Sampling time,  $u(t)$ -Conventional PI controller output,  $e(t)$ -Input variable,

$$U(t) = K_p e(t) + K_i \int e(t) dt + K_d \frac{de(t)}{dt} \tag{29}$$

There are two inputs made by nonlinear MF of FL, the discrete-time of input signals are allowed into a FIS, and it can prevent the step change in reference signal from directly trigger to the PI controller. The PI controller gives the pulse into the respective converter switches. The overall Simulink model from an input (e) is a Solar-PV source, the PV output is fed into FL-based PI controller. The variation pulse with

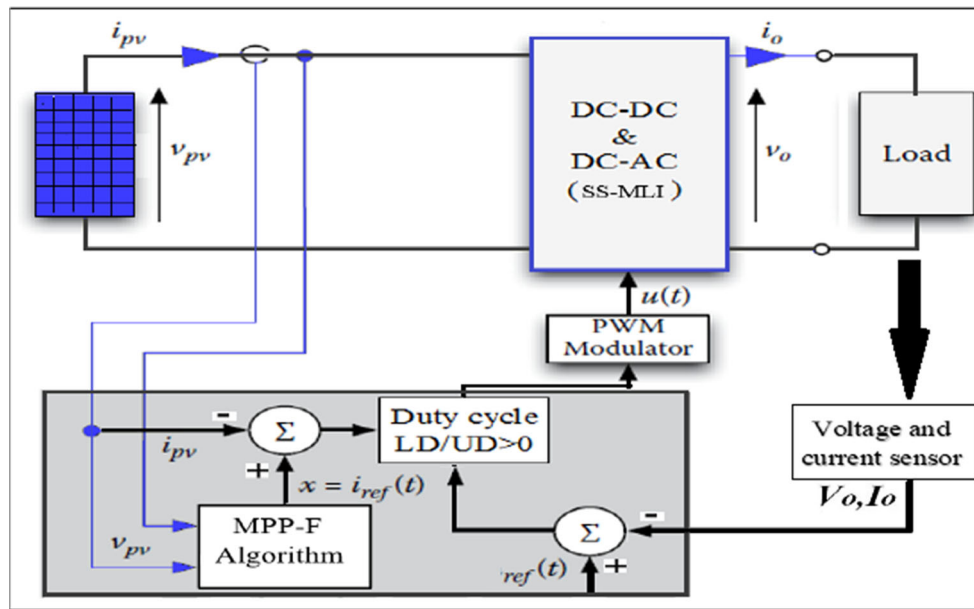


Fig. 12 Block Diagram of RL load connected SV-LI with MPP-Fuzzy controller

Table 6 Parameter for MPP-tuned fuzzy controller

MPP Parameters	Values
Maximum power ( $P_{max}$ )	305 W
Maximum Voltage ( $V_{mpp}$ )	64.2 V
Maximum Current ( $I_{mpp}$ )	5.96A
Converter Duty cycle ( $D$ ) output ( $D$ initial)	1
Increment value used to Increase/decrease (Delta $D$ )	$3e^{-4}$
Lower limit ( $D_{max}$ ) value	0.4
Upper limit ( $D_{max}$ ) value	0.58

different solar irradiation condition, it will ensure that the error signal ( $e$ ) is used in a proportional derivative.

When the PI controller is linear, therefore, the linear fuzzy-tuned PI Structure is properly designed. One of the most significant stages in an FL controller design process is produced by the MF. It can describe in the input and output variables of the MF in PI controller scheme. It is appropriate for calculated in  $K_p$  and  $K_i$  variables fixed into PI controllers. The SV-LI voltage and current are controlled by change of error ( $C_e$ ) and functions of errors with respective solar irradiation conditions. The change of error signal is mention as  $e(K) - e(K - 1)$ . It is used to function for the input and output variables in FL-MF of error shown in Table 5a & b. The adjustable FIS is achieved as a better way to get multi-level output across the RL load. Table.5(c) shows the tuned value for PI controller with maximum peak voltage value.

### 4.3 MPP-Fuzzy Based Controller Design

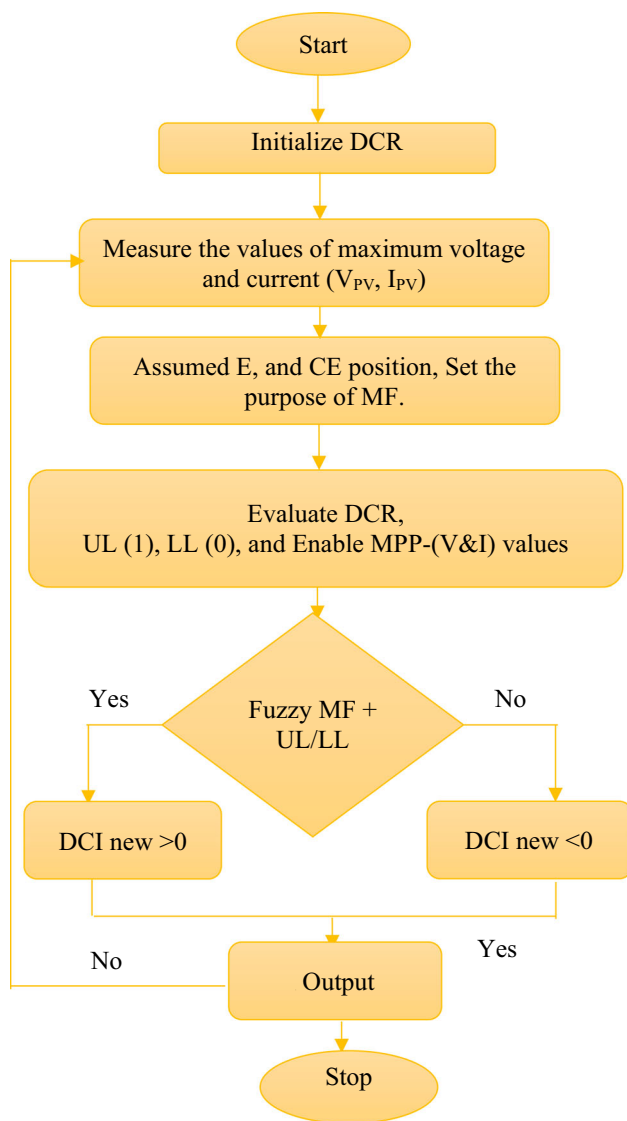
The MPP-Fuzzy (MPP-F) tuned controller using for generate Duty Cycle Incremental (DCI) method, the proposed scheme is generated by variation of duty cycle into converter and inverter switches, therefore incremental output should be measured across the RL load. The MPP-F logic Algorithm is used to get input power from S-PV module. The efficiency of the solar system needs to be improved by MPP (P&O) method as shown in Fig. 12. In several MPP-intelligent based controllers are developed in the part of power converters, it is verified with output gain of the solar-PV system and inverter output power improvements are described. This type of intelligent control is addressed, so far maybe work well for all environmental conditions, due to sudden changes in reference voltage or current threshold values. Due to overcome the drawback, the MPPT controllers are generated a duty cycle with the help of a fuzzy-based controller. It can generate the switching signals for all the DLB converters and SV-LI. The switching signal of the converters is operated with a PWM modulator. It is possible for optimum voltage and current variation, due to that the maximum power extraction is possible in RL load conditions.

#### 4.3.1 Duty Cycle Incremental Using MPP-Fuzzy Algorithm

The DCI using for MPP-fuzzy based algorithm to follow the steps are,

*Step 1* Initialize the PV voltage and current value as well as the Duty Cycle Ratio (DCR) in between 0 & 1.





**Fig. 13** Flow chart for MPP-Fuzzy controller

*Step 2* Measure the values of maximum tracking voltage ( $V_{PV}$ ) and current ( $I_{PV}$ ) with the help of P&O method.

*Step 3* In fuzzy-based intelligent, the reference error ( $E$ ) and change of error ( $CE$ ) signal position assumed to the purpose of forming MF.

*Step 4* The corresponding DCR value evaluates, using Upper Limit ( $UL$ ) & Lower Limit ( $LL$ ), Delta ( $D$ ), and enable MPP-values ( $V_{PV}$  &  $I_{PV}$ ) are taken as respective fuzzy rules for DCI as shown in Fig. 13.

*Step 5* For each DCR in sequential order, update the Fuzzy (F)-MF of each duty cycle, and its position  $UL$  (1) &  $LL$  (0). The duty cycle updates its position in each MF.

*Step 6* Once the criterion is reached DCI should be repeated, or otherwise, go to step 2, and the above steps until reaching the maximum power.

*Step 7* Stop.

The DCI method is used output, from the earlier system of MPP controllers such as Differential-Power (DP) and Differential-Voltage (DV). The proposed system has special function adopted, the solar PV array is adjusted with the help of MPP (P&O) controller. Therefore, the varied voltage to assist the intelligent controller such as FL-tuned controller. The MPP controller reference voltage and current gain are tuned for many error and control signals into a fuzzy controller concerning the solar variable irradiation conditions. The FL inputs of Error ( $E$ ), change of error ( $CoE$ ), and the reference signals are calculated in the Eqs. (30) & (31), and these are all error signal values fed into FL toolbox. It can generate the optimum PWM generation.

The output of the DCR is calculated by using MPP-F controller based PV approach as shown in the Eq. (32). The aim of MPP-TIFC rule is to incorporate with variety of upper, lower limit ( $D$ -max), and incremental step-by-step values ( $\Delta D$ ). That helps to find the most effective optimum converter DCR in MATLAB-Simulink parameters as shown in Table 6. Where, the solar power and voltage are referred by  $P_{PV}$ , and  $V_{PV}$ . The output of the Duty Cycle Ratio is referred by DCR.

$$\text{Error}(K) = \frac{P_{PV}(K) - P_{PV}(K-1)}{V_{PV}(K) - V_{PV}(K-1)} \quad (30)$$

$$\text{CoE}(K) = E(K) - E(K-1) \quad (31)$$

$$\text{DCR} = D(K-1) + dD(K) \quad (32)$$

#### 4.4 Artificial Intelligent Techniques (AIT)

Artificial neural networks (ANNs) are developed to mimic the nature of the human brain. In the attempt of developing such networks mathematics related to the optimization methods were used. In general the neural networks are typically organized as layers and these layers consist of the nodes which are connected each other in different fashions for the respective topologies. The nodes consist of the activation functions which can be customized. The learning situations in neural networks may be classified into three distinct types (Murugesan et al., 2021). These are supervised, unsupervised, and reinforcement learning. In supervised learning, an input vector is presented at the inputs together with a set of desired outputs, one for each node, at the output layer. The neural networks should be trained by applying the patterns to the network via the ‘input layer,’ which are connected to the one or more hidden layers. The patterns are processed through the layers of the system by the weighted connections. The schematic diagram of the artificial network has been shown in Fig. 14. In Fig. 15 is recognized all the hidden, input and output layers of the network. The input values are fixed,

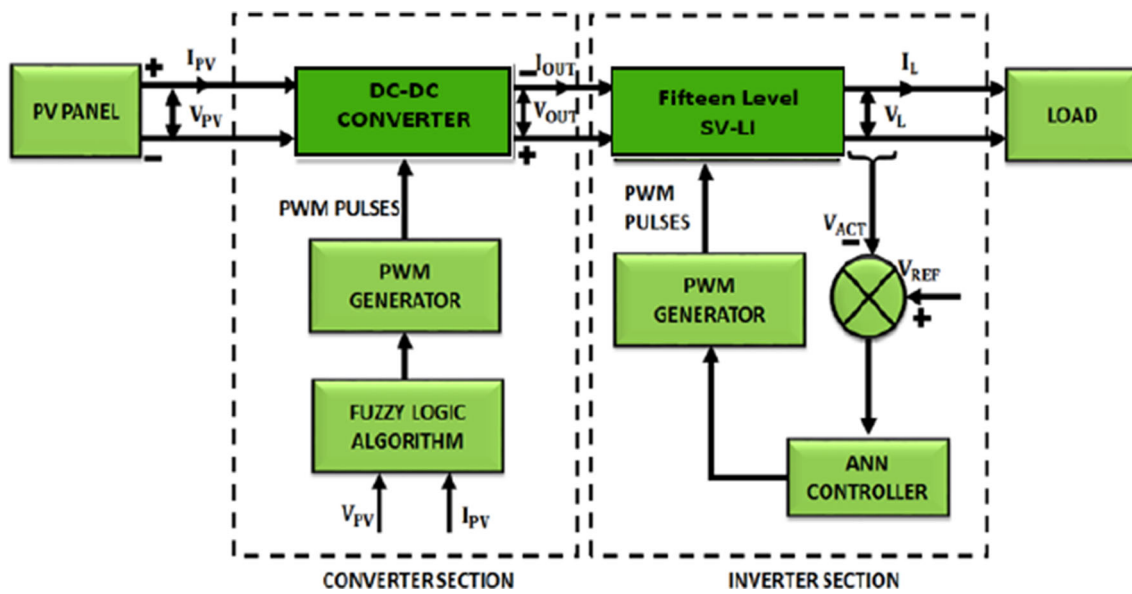


Fig. 14 ANN-based fifteen level inverter block diagram

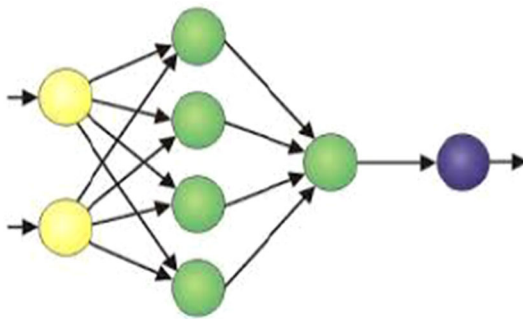


Fig. 15 Schematic diagram of ANN

the weights (synaptic coefficient) and the bias parameters values are controlled the output. The specification consider the fifteen level inverter using artificial intelligent techniques shown in Table 7a, and the simulation parameters are shown in Table 7b.

A forward pass is done, and the errors between the desired and actual response for each node in the output layer are computed. These error values are then used to determine weight changes in the net according to the learning rule. The mathematics involved in the neural networks was not too difficult even technical engineers can understand the behavior or the operation of the neural networks. As per the voltage error values are calculated in Eq. (33). The value of the error is used to train ANN techniques, which is offered the appropriate values of the error signals. Hence the ANN can provides the optimum pulse and switching angle values ( $\delta$ ) calculated

Table 7 (a) Specification of AIT. (b) Simulation parameters

Parameters	Values & function
(a)	
Input layer	2
Hidden layer	5
Output layer	1
Learning rate	0.06
Network algorithm	Back propagation
Goal	$1e^{-6}$
Training function	Purelin
Activation function	Sigmoid & Tangential
Rule	Delta and perceptron rule
(b)	
Maximum voltage $V_{mpp}$	64.2 V
Maximum current $I_{mpp}$	5.96 A
Open-circuit voltage ( $V_{oc}$ )	54.7 V
Short-circuit current ( $I_{sc}$ )	5.58 A
Inductor	450 mH
Capacitor unit (DC-DC)	1600 $\mu$ F
Capacitor unit (DC-AC)	2800 $\mu$ F
R load	40 $\Omega$
RL load	40 $\Omega$ + 30 mH

in Eq. (34). Where ‘ $d$ ’ is the duty cycle, ‘ $k$ ’ is the number of iteration, ‘ $\alpha$ ’ is the pulse, and ‘ $\delta$ ’ is the switching angle.

$$\text{Verror} = \text{Vreference value} - \text{Vactual value} \tag{33}$$

$$d(K + 1) = d(k) - \left( \frac{\alpha \delta(k - 1)}{\delta d(k)} \right) \tag{34}$$

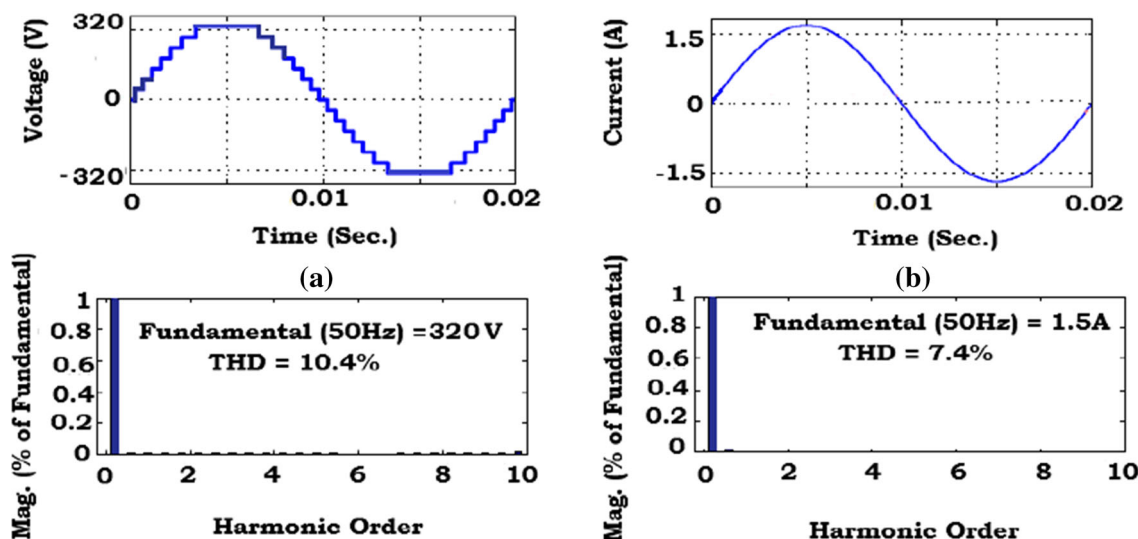


Fig. 16 Fifteen level RL load a Output voltage with FLC b Output current with FLC

### 5 Simulation Result and Discussion

The simulation results of fuzzy logic, Fuzzy-PI, MPP-fuzzy, and AIT approach has been verified by using MATLAB R2019a-Simulink tool. The fifteen level SV-LI output voltage can be obtained by using the same value of DC output in a single PV module nominal voltage and current is  $V_{dc} = 64$  V and  $I_{dc} = 5.96$  A. In general, there is a two-module voltage conversion presented in the proposed system, the first module SV-LI, and second module DLBC. The SV-LI overcome the existing multilevel inverter technics, which is tracking voltage of MPP in each sting and also an independent controller to each model, there are two major converters are performed in proposed system D-LC, SV-LI, and it is verified under modulation and intelligent control techniques. It is verified with the parameters of voltage, current, and power. The PV module is verified with various irradiation conditions from source to load side.

The ultimate aims of this control approach is generated with optimum results of modulation index, and switching angle values. The proposed method involves the fifteen level MLI using FL controller, working under the basic thinks to form the mapping with the help fuzzy interfacing process. Which is made by two inputs error and derivative signals, it is used to frame the MF. There are seven MF, output and derivative signals are formed. The rules are set by FL controllers performed with better output voltage and current generated with least harmonics level as shown in Fig. 16a & b. The fifteen—stage MLI offers the maximum output result three times of the solar feedback voltage. The FIS is provided to various output voltage in each different harmonic order, which is found out the switching angle of the inverter utilized in SV-LI.

Table 8 switching angle results in SV-LI

Modulation index (ma)	Phase angle ( $\theta_1$ )	Phase angle $\theta_2$	THD%
0.8	36.35	41.27	10.4
0.7	32.90	29.65	11.5
0.65	21.96	38.47	12.5
0.5	18.95	21.7	17.4
0.4	35.87	30.80	10.9
0.3	51.82	28.4	13.5

Table 8 is described as the simulation FL controlled switching angle of the SV-LI. When the MI is varied, the FIS of switching angles is generated from the different angles ( $\theta$ ) into the MLI switches. The values of MI is calculated from the below Eq. (35). The range of modulation index is varied from 0.8 up to 0.3. The fuzzy-based controller is evaluated in a closed-loop manner, and it is regulated SV-LI output in RL load condition.

$$\text{Modulation Index(MI)} = \left( \frac{V_{\text{reference}}}{V_{\text{carrier}}} \right) \tag{35}$$

The solar DC input of SV-LI variations according to the irradiation condition. The output is obtained across the RL load fed into solar SV-LI. The proposed converters are associated with the reference and error voltage signals. The FL error signal is applied to the gain of PI controller, i.e.,  $K_p = 7.6$  and  $K_i = 2.61$ . The SV-LI output of the PI value is compensated for the signals, which is added some required modulating signal and reference signal. Figure 17a shown the regulate fuzzy-PI controller output voltage and its FFT minimum harmonics analysis. Figure 17b shows regulate the

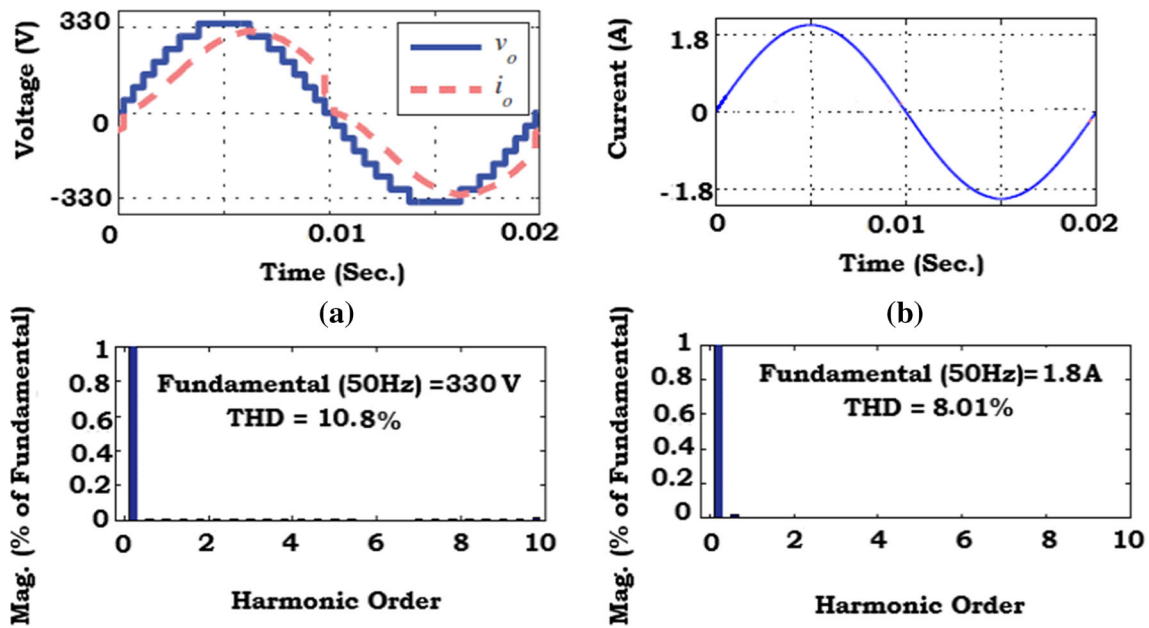


Fig. 17 Fifteen level Fuzzy-PI controller a Output voltage with FFT. b Output current with FFT

Table 9 Calculation of PV voltage, current, and power at fixed irradiation

Irradiation level (kW/m <sup>2</sup> )	Proposed MPP-(P&O) algorithm		
	Solar-PV output voltage (V <sub>PV</sub> )	Solar-PV output current (I <sub>PV</sub> )	Solar-PV output power (P <sub>PV</sub> )
0.25	44 V	1.8 A	79 W
0.5	46 V	3.5 A	161 W
0.75	49 V	4.3 A	210.7 W
1	51 V	5.99 A	305 W

fuzzy-PI controller output current and its FFT analysis in minimum harmonics level.

The MPP-Fuzzy control algorithm is operated in fixed temperature at 25 °C, the maximum power, voltage, and

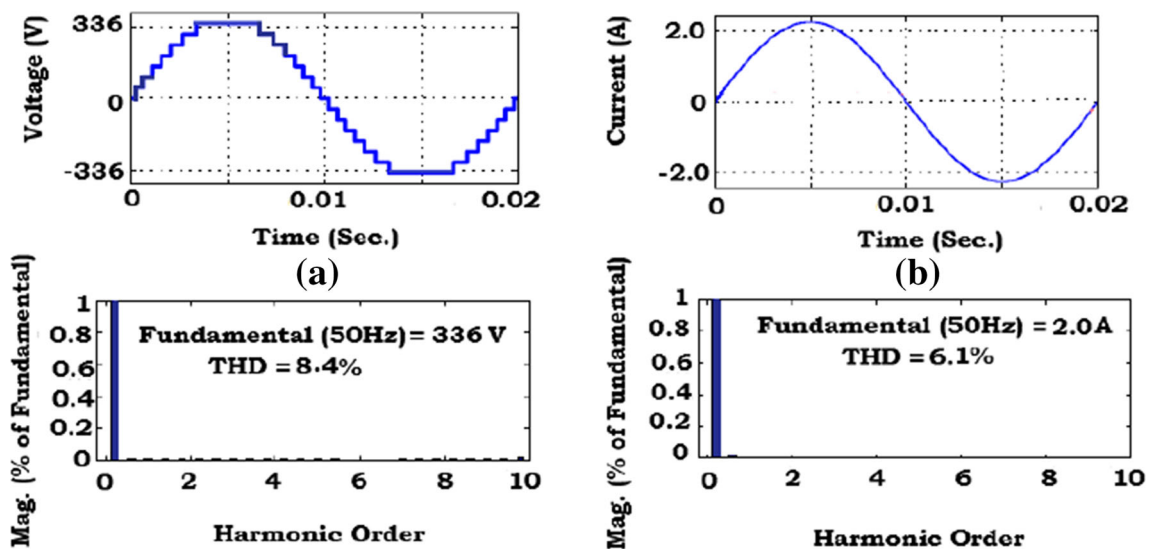


Fig. 18 Fifteen level MPP-Fuzzy based controller a Output voltage with FFT analysis b Output current with FFT analysis

**Table 10** Duty Cycle Incremental using for MPP-Fuzzy control Algorithm

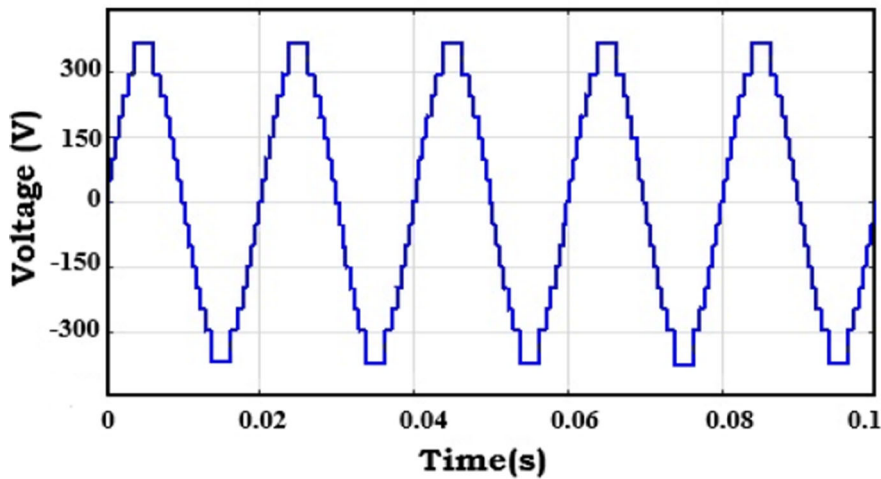
MPP-Fuzzy control Algorithm		
Duty cycle	Output voltage (V)	Output current (A)
0.4	320.9	1.91
0.5	325.56	1.98
0.6	320	1.90
0.7	330.5	1.95
<b>0.8</b>	<b>336</b>	<b>2.0</b>
0.85	320	1.90

current values are developed in full irradiation condition at 1 kW/m<sup>2</sup> as shown in Table 9. The dynamic change of RL load is operated in full load and half load conditions veri-

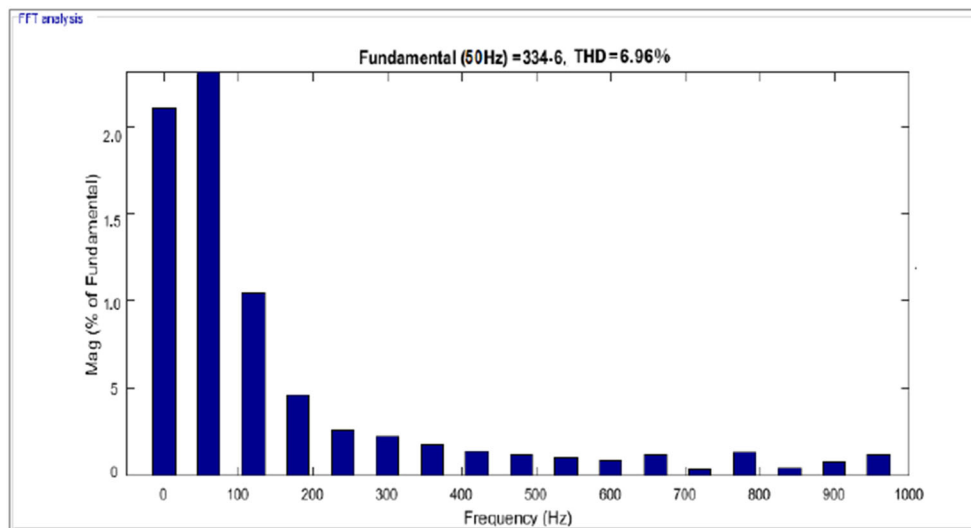
**Table 11** Simulation comparison results

Intelligent techniques	RL-load		RL-load	
	V <sub>out</sub>	I <sub>out</sub>	V <sub>THD</sub> (%)	I <sub>THD</sub> (%)
FL controller	320 V	1.5A	10.4	7.4
FL-PI controller	330 V	1.8A	10.8	8.01
MPP-FL controller	336 V	2.0A	8.4	6.1
AIT	340 V	2.0A	6.96	5.06

fied in the proposed method, it can be obtained pulses into two converter switches with the variation of duty cycle. The fifteen level SV-LI maximum voltage is achieved, and the FFT voltage harmonics are minimized up to 8.4% shows in Fig. 18a. The maximum current rating is achieved, and the FFT minimized harmonics levels are 6.1% presented in



**(a) Fifteen level output voltage of AIT**



**(b) FFT spectrum harmonics analysis of AIT**

**Fig. 19** a Fifteen level output voltage of AIT. b FFT spectrum harmonics analysis of AIT



**Table 12** Comparison of existing simulation results

Authors	Techniques	THD (%)
Azeem et al. (2019)	Fuzzy	20.27
Cherifi et al. (2019)	MPP-based FL controller	47
Rahila et al. (2020)	MPP-based FL controller	13.4
Elbarbary et al. (2018)	Fuzzy- PI Controller	20
Albert et al. (2021)	MPP controller	11.5
Babaie et al. (2020)	ANN	13
Mahendrarvarman et al. (2020)	ANN	11.2
Bute et al. (2020)	Fuzzy	15
Khushal Chaudhari et al. (2021)	Fuzzy	10.9
Santhiya et al. (2018)	Fuzzy	15.9

Fig. 18b. The output of the MPP-fuzzy based controllers is used maximum watts 305. The DCI using for MPP-Fuzzy control Algorithm output voltage is varied from 0.4 up to 0.8. The maximum power is  $230 V_{rms}$ , 2A achieved by DCI for MPP- fuzzy based controller a shown in Table 10. Figure 19a & b display the AIT multilevel output voltage are presented with minimum harmonics distortion in fifteen level SV-LI. Proposed MPP-fuzzy controller is first time implemented in symmetrical voltage-lift inverter, the novelty of this literature work is based on the several intelligent techniques such as fuzzy-based controller, fuzzy-PI controller, MPP-tuned fuzzy controller, and AIT approach.

Fuzzy-based MPP controller, and AIT results are represented with minimum load harmonics values, which is voltage and current harmonics operated in the dynamic change of RL load conditions. The minimum harmonic order of maximum voltage and current generate intelligent techniques as represented in Table 11. These intelligent controller is used for generate effective modulation index ( $m_a$ ) or duty cycle or switching angle values, and it is determined the outcome of sinusoidal voltage and current output with less harmonic distortion values, compared with simulation results as shown in Table 12.

## 6 Conclusion

Fifteen level SV-MLI is designed, simulated, and validated in a prototype experimental model without any additional filters and control power switching devices. The P-Q enhancement for the proposed inverter have been implemented using four intelligent techniques methods. Results are also obtained by using different levels of voltage, which shows SV-MLI can perform flexible voltage conversion. This research starting point is designed and explanation of MLI by using new topology named as symmetric voltage-lift inverter. Comparison of other types of conventional, modified, and classical MLI

has extra semiconductors needed for the power conversation. Therefore, conversion, conduction, and switching losses were very high. Which are overcome by this proposed MLI, it shows the least low order harmonics and better reactive power development. The improvement of reactive power is measured across the different loads, which helps to series capacitor bank unit in SV-LI. The main advantage of this proposed solar fed inverter approach is to implement without filter components that are minimized cost of the circuit.

**Funding** This research has not received any funding support.

## Declarations

**Conflict of interest** Author are declare that, there is no conflict of interest.

**Ethical Approval** This article does not contain any studies with human participants or animals performed by any of the authors.

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