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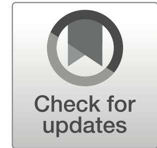
RESEARCH PAPER



Effect of substrates on the formation of Kirkendall voids in Sn/Cu joints

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Abstract
The reliability of flip-chip Sn/Cu solder joint strongly depends on Kirkendall voids, since it affects the mechanical properties of the solder joints. In this paper, the formation of Kirkendall voids (KVs) at the interface of Sn/Cu joints was investigated by changing various Cu substrates, namely, high-purity Cu (HP Cu), electroplated Cu (EP Cu), and vacuumed-sputtered Cu (VS Cu). It is found that the KVs did not appear at the Sn/HP Cu interface even after aging at 180 °C for 720 h. A large number of voids were observed at the Cu_3Sn/Cu interface in Sn/EP Cu and Sn/VS Cu joints during a short aging time. The size of voids formed in the Sn/EP Cu was larger relative to that in Sn/VS Cu. The formation of different voids at the Sn/Cu joints can be attributed to three factors, i.e., diffusion paths for Cu atoms increased from Sn/HP Cu, Sn/EP Cu, and Sn/VS Cu, different impurities (S, Cl, et al.) in Cu substrates, and different stress states at the Cu_3Sn/Cu interface.

Keywords Cu substrate · Interface · Kirkendall void · Grain size · Stress

1 Introduction

In the joints between Sn-based solders and Cu substrate, the presence of Kirkendall voids (KVs) always accompanies with the formation of Cu_3Sn layer during the thermal aging. With the miniaturization of solder joints, the voids usually formed at the Cu/Cu_3Sn interface have a detrimental effect on the reliability of joints [1–4].

Generally, the formation of KVs was attributed to the Kirkendall effect, that is, the unbalanced diffusion of component elements (mainly Cu and Sn) [5, 6]. Researchers found that the presence of impurities plays a very important role in the growth of KVs [1, 5–11]. For instance, Kim et al. [6, 8] indicated that the impurity element S incorporated during the electroplating process could segregate at the Cu_3Sn/Cu interface, reduce the activation energy barrier of the void nucleation, and accelerate the formation of voids. Yin et al. [5] [11] pointed out that the organic impurities were responsible for the formation of voids. In addition, due to the effect of impurities in electroplated Sn, the voids can also be developed in the Sn/high-purity Cu (HP Cu) couples [3].

In recent years, extensive research has been done on the effect of impurities on the formation of KVs [3, 6, 8, 9]. However, there have been few studies on exploring the microstructure of Cu substrate. Zou et al. [12] mentioned that the formation of voids might be affected by the grain size of Cu substrate. Therefore, a comprehensive and systematic research on the effect of various Cu substrates on the formation of KVs at the Sn/Cu interface is very necessary.

In these works, three types of substrates, i.e., HP Cu, electroplated Cu (EP Cu), and vacuumed-sputtered Cu (VS Cu), were designed to produce Sn/Cu joints. The concentration of impurities and grain size of Cu substrates were analyzed. The interface evolution, especially the Kirkendall voiding level, was discussed.

2 Experimental procedures

The solder used in this work was pure Sn (99.99%). Three kinds of substrates were used, designated as HP Cu, EP Cu,

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and VS Cu. HP Cu in dimension of 10 mm × 10 mm × 0.1 mm was 99.999% in purity. Electroplated (EP) Cu film in 10-μm thickness is processed with a solution which consists of $CuSO_4$, H_2SO_4, HCl, and PEG (polyethylene glycol) (the detailed contents could be found in refs. [13, 14]) and a VS Cu film is processed at a vacuum level of 4.99×10^{-5} Torr and electric current of 4 A for 2 h. The target and substrate were high-purity copper (99.999% in purity), and prior to the deposition process, the substrate was cleaned in acetone, followed by deionized water rinsing in an ultrasonic tank. The final deposited Cu film was 5 μm in thickness.

The surface microstructure of HP Cu, EP Cu, and VS Cu was observed by scanning electron microscopy (SEM), and the etchant of 5 g $FeCl_3$ + 8 ml HCl + 8 ml HNO_3 + 100 ml C_2H_6O was used to display the grain boundary. The mean grain sizes were measured with the software Image J. At last, the solder joints were prepared by melting Sn on the foils at 260 °C for 1 min. The isothermal aging for the as-reflowed samples was performed at 150 °C or 180 °C for different times. Then, these samples were mounted in epoxy and metallurgically polished. The cross-sectional microstructure at the interface was observed by SEM, the compositions of intermetallic (IMC) layer were determined by energy-dispersive spectroscopy (EDS), and the average thickness of IMC layers was measured with the software Image J. X-ray photoelectron spectroscopy (XPS) was used to characterize the presence of impurities (C, O, Cl, and S) in all kinds of Cu substrates. To observe the three-dimensional morphology of the interfacial IMC layers, the Sn solder was etched completely using a 10% HNO_3+90% distilled water solution.

3 Experimental results

Figure 1(a1) shows the interfacial microstructure of as-reflowed Sn/HP Cu joint. A layer of scallop-shaped Cu_6Sn_5 formed at the interface, and no voids appeared at the interface. After aging at 180 °C for 72 h, a Cu_3Sn layer emerged at the interface of Cu_6Sn_5/HP Cu, but no voids can be detected, as presented in Fig. 1(b1). Even after aging at 180 °C for 720 h, as seen in Fig. 1(c1), there still have no voids at the Cu_3Sn/HP Cu interface. Moreover, the thickness of the Cu_3Sn layer exceeds that of Cu_6Sn_5 layers. The interfacial microstructure of as-reflowed Sn/EP Cu joints can be observed in Fig. 1(a2). Similar to the Sn/HP Cu joints, the scallop-shaped Cu_6Sn_5 layer was formed at the interface. Only several voids can be found at the Cu_3Sn/EP Cu interface after aging at 180 °C for 24 h, as seen in Fig. 1(b2). After extending the aging period to 72 h, a large number of voids appeared, most of which located in the Cu_3Sn layer near the Cu_3Sn/EP Cu interface, as seen in Fig. 1(c2). Figure 1(a3–c3) shows the interface morphologies of the Sn/VS Cu joints. After the reflow treatment, the scallop-shaped Cu_6Sn_5 layer and the thin Cu_3Sn layer formed at the interface, but both of them were discontinuous. In addition, a small amount of KVs was detected during the soldering period (Fig. 1(a3)). After aging at 180 °C for 24 h, continuous IMC layers were developed and the KVs at the Cu_3Sn/VS Cu interface became denser (Fig. 1(b3)). With the further prolonging of aging time to 72 h, many small voids appeared at the Cu_3Sn/VS Cu interface (Fig. 1(c3)).

According to the experimental results above, KVs did not appear at the Sn/HP Cu interface even after aging at 180 °C for 720 h, but formed at the Sn/EP Cu and Sn/VS Cu interfaces after a short aging time. Moreover, the void size and number distribution of Sn/EP Cu were more than those of Sn/VS Cu.

4 Discussion and analysis

The reasons why the KVs of the Sn/Cu solder joint vary from HP Cu to VS Cu substrates are analyzed. Three main factors are presented as follows:

i. Diffusion paths for Cu atoms increased from Sn/HP Cu, Sn/EP Cu, and Sn/VS Cu. The microstructures of three kinds of substrates are shown in Fig. 2(a). It can be seen that the HP Cu has coarse grains and the mean grain size is about 30 μm. However, compared with HP Cu, the grain sizes of EP Cu and VS Cu are much smaller those of about 1.2 μm and 300 nm, respectively. The number of grain boundaries of Sn/HP Cu, Sn/EP Cu, and Sn/VS Cu interfaces is compared. The top morphology of the interfacial Cu_6Sn_5 is shown in Fig. 2(b). It is seen that the number of grain boundaries increased from Sn/HP Cu, Sn/EP Cu, and Sn/VS Cu.

It is well known that copper is the dominant diffusing species in the Sn/Cu reaction couple [15, 16]. The grain boundary diffusion is the dominant diffusion mechanism for Cu atom [17], due to the number of grain boundaries increased from Sn/HP Cu, Sn/EP Cu, and Sn/VS Cu. It means that the Cu flux increased from Sn/HP Cu, Sn/EP Cu, and Sn/VS Cu. The vacancy flux (J_v) by the Sn/Cu reaction couple can be expressed as follows

$$J_v = J_{Cu} - J_{Sn} \tag{1}$$

where J_{Cu} is the Cu atoms diffuse out of the Cu/IMC toward the Sn matrix and J_{Sn} is the Sn atoms that migrate from the Sn matrix to the IMC/Cu interface. It well known that the formation of KVs was attributed to the unbalanced diffusion of component elements, that is, Cu and Sn [6]. Since the Sn/VS Cu and Sn/EP Cu can supply bigger J_{Cu} than that of Sn/HP Cu due to more diffusion paths, there will be generation of more considerable vacancies at the Sn/VS Cu and Sn/EP Cu relative to the Sn/HP Cu at the Cu_3Sn/Cu interface.

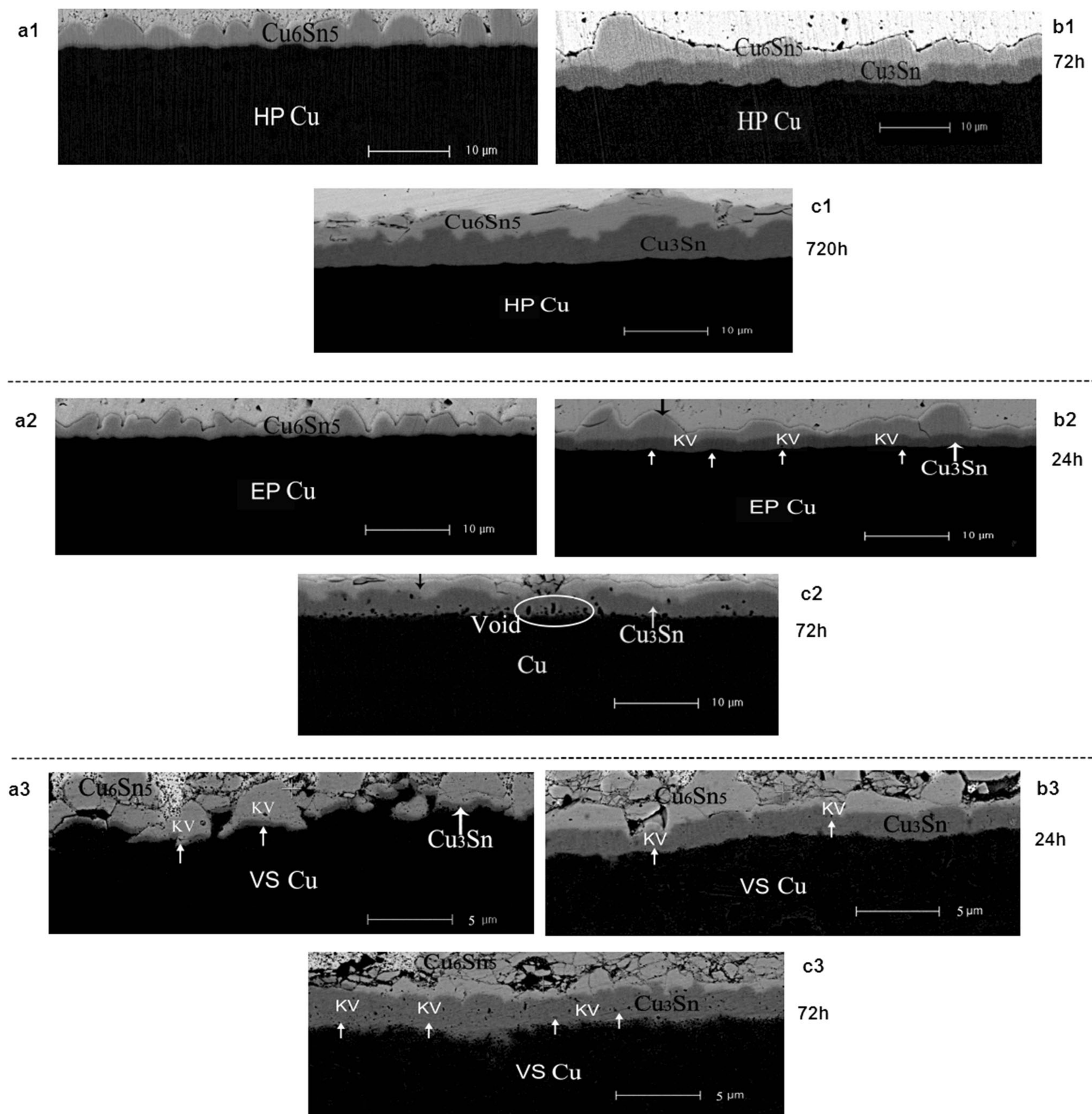

Fig. 1 BSE micrographs with comparison of the growth of the Kirkendall voids in solder joints of (a1–c1) 99.99 wt% bulk Sn and high-purity Cu, (a2–c2) 99.99 wt% bulk Sn and electroplated Cu, and (a3–c3) 99.99 wt% bulk Sn and vacuumed-sputtered Cu annealed at 180 °C for different times

ii. Different impurities in substrates. The formation of KVs is closely related to the impurities in the Cu substrate. Kumar et al. [18] revealed that the voids can be observed at the Sn/Cu (99.9%) interface at a relatively high temperature, while not at the Sn/Cu (99.999%) interface. Yu et al. [6] showed that the segregation of impurities (like sulfur) to the Cu/Cu_3Sn interface might lower the nucleation energy of KVs. Figure 3 and Table 1 show the atomic percentages of impurity elements, like C, O, S, and Cl, in HP Cu, EP Cu, and VS Cu by using XPS (the HP Cu is 99.999% in purity; the XPS spectra do not list). It is seen that the EP Cu contained the impurity element S and Cl, but the surface components of HP Cu and VS Cu are all purity Cu except basic existent elements C and O.

Due to the impurity, element S incorporated during the electroplating process could segregate at the Cu_3Sn/Cu

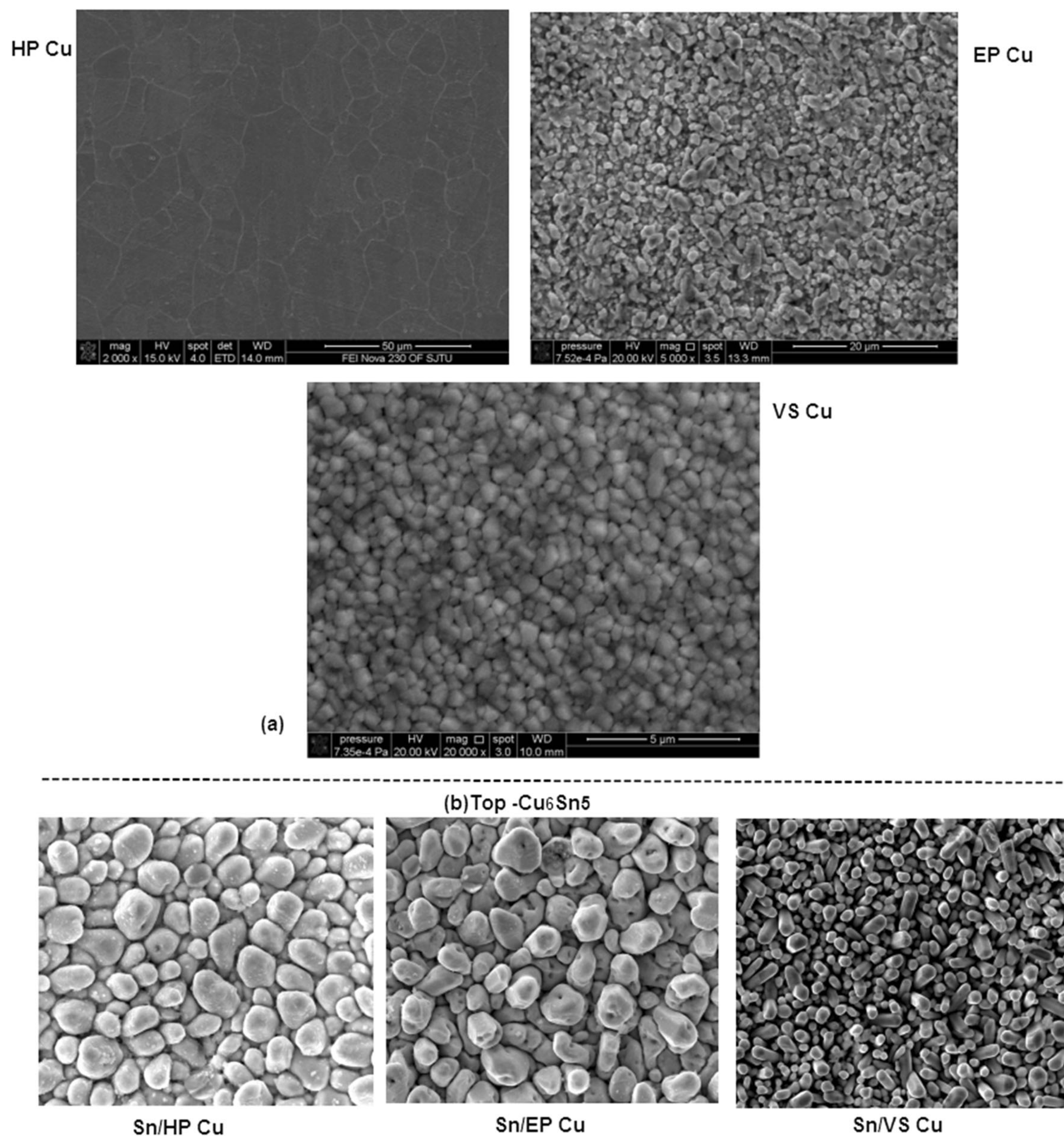

Fig. 2 Surface morphology of (a) HP Cu, EP Cu, and VS Cu VS. The top morphology of the interfacial Cu_6Sn_5 of (b) Sn/HP Cu, Sn/EP Cu, and Sn/VS Cu joints

interface, reduce the activation energy barrier of the void nucleation, and accelerate the formation of voids. Therefore, a large number of voids appeared at the Cu_3Sn/EP Cu interface and further prove that the impurity is one of the major reasons for Kirkendall voiding.

iii. Different stress states at the Cu_3Sn/Cu interface. There is a close correlation between the voids and the Cu_3Sn phase [19]. The voids always appear at the Cu_3Sn/Cu interface. The results in this work were also in accordance with this conclusion. The location of voids at the interface is related to the distribution of residual stress induced by phase transformation [20]. In the very early stage, the formation of IMC phases at the interface will cause a significant volume contraction [4, 20]. Song et al. [20] revealed that if the IMC layers were formed by Cu and Sn interdiffusion within a short time, the volume shrinkage was − 10.29 cm^3/mol ($\Delta V = V_{Cu3Sn} - 3V_{Cu} - V_{Sn}$) for Cu_3Sn or − 6.04 cm^3/mol ($\Delta V = V_{Cu6Sn5} - 6V_{Cu} - 5V_{Sn}$) for Cu_6Sn_5, and induced a tensile force according to force and momentum equilibria of the Cu-Sn system. Based on the structural information, the volume contraction can be estimated. When pure Cu and Sn react to form Cu_6Sn_5, a net 5.44% contraction in volume will occur. There will be a net 9.97% decrease in volume during the formation of Cu_3Sn. It can be noted that the

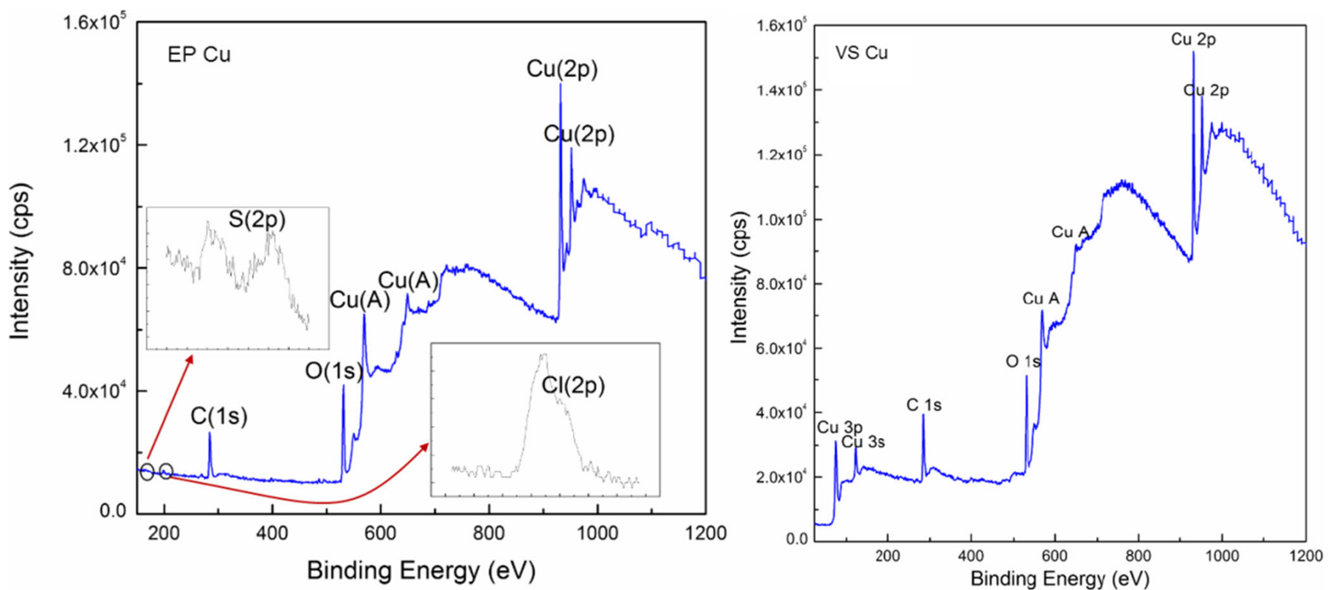

Fig. 3 The components of EP Cu (a) and VS Cu (b) substrates by XPS spectra

shrinkage rate of Cu_3Sn is approximately twice as high as that of Cu_6Sn_5, so the voids appear at the Cu_3Sn/Cu interface easily.

In the later stage of IMC formation after tensile force evolution, the IMC layer grows toward the Sn side by the dominant diffusion of Cu into Sn side. The molar volume (V_{Sn}) of

Fig. 4 Micrographs of the Cu_6Sn_5 and Cu_3Sn layers of Sn/Cu solder joint annealed at 150 °C: (a) 99.99 wt% bulk Sn and high-purity Cu, BSE image; (b) 99.99 wt% bulk Sn and electroplated Cu, BSE image; and (c) 99.99 wt% bulk Sn and vacuumed-sputtered Cu, BSE image

Table 1 XPS data for electroplated HP Cu, EP Cu, and VS Cu; C, O, Cl, and S denote the atomic percentages of C, O, Cl, and S

Sample	C	O	Cl	S
HP Cu	56.11	32.70	–	–
EP Cu	59.34	37.66	1.95	1.05
VS Cu	56.01	32.59	–	–

Sn was replaced with that (V_{IMC}) of Cu-Sn IMC (Cu_3Sn and Cu_6Sn_5). Song et al. [20] revealed that a compressive force resulted from the volume expansion of + 11.01cm^3/mol ($\Delta V = V_{Cu3Sn}$-$V_{Sn(with\ 3Cu)}$) and/or + 36.56 cm^3/mol ($\Delta V = V_{Cu6Sn5}$-$5V_{Sn(with\ 6Cu)}$). In addition, the formation of Cu_3Sn between Cu and Cu_6Sn_5 was due to the interstitial diffusion of Cu [15]. It also caused a compressive force with the molar volume expansion of + 18.49 cm^3/mol ($\Delta V = 5V_{Cu3Sn}$- $V_{Cu6Sn5\ (with\ 9Cu)}$). Figure 4 shows micrographs of the Cu_6Sn_5 and Cu_3Sn layers of Sn/Cu solder joint annealed at 150 °C for different times. Similar to the Sn/Cu joints annealed at 180 °C, the KVs did not appear at the Sn/HP Cu interface even after aging at 150 °C for 720 h, but formed at the Sn/EP Cu and Sn/VS Cu interfaces after a shorter aging time. However, during the annealing at 150 °C, the KVs of Sn/EP Cu and Sn/VS Cu interfaces were found to need longer aging times than those at 180 °C. Figure 5 shows the relationship between aging time and average thickness of Cu_6Sn_5 and Cu_3Sn layers in three kinds of joints. It can be seen that the growth rate of Cu_6Sn_5 and Cu_3Sn layers could be enhanced by grain refining of Cu substrates. Under the same thermal aging time, the thickness of total IMC layers increases from Sn/HP Cu, Sn/EP Cu, and Sn/VS Cu solder joint. In addition, with annealing increasing from 150 to 180 °C, the growth rate of Cu_6Sn_5 layers of three kinds of joints changed little, as seen in Fig. 5(a). The growth rate of Cu_3Sn layers of three kinds of joints grew much quickly, as seen in Fig. 5(b). To sum up, the thickness of total IMC layers of Sn/VS Cu and Sn/EP Cu solder joints was much thicker than that of Sn/HP Cu solder joints, especially for the Cu_3Sn layer. Therefore, the higher distribution of residual stress would be developed at the Sn/VS Cu and Sn/EP Cu interfaces relative to the Sn/HP Cu solder joints. Kim and Weinberg [6, 21] pointed that the residual stress facilitated the grain boundary diffusion of Cu atoms in solder joints and aggravated the unbalanced diffusion of Cu and Sn at the interface. Consequently, the higher distribution of residual stress at the Sn/VS Cu and Sn/EP Cu interfaces relative to the Sn/HP Cu solder joints is conducive to the formation of voids.

The common feature for HP Cu and VS Cu is that there existed negligible impurities in the substrates, but the VS Cu has much smaller grains and the higher stress at Cu_3Sn/Cu interface relative to the HP Cu. Although the grain size of EP Cu is larger than that of VS Cu, the impurity elements S and Cl are incorporated into EP Cu during plating. The KVs formed have a large void size and number distribution in the Sn/EP Cu solder joints compared with the Sn/VS Cu solder joints.

5 Conclusions

Three kinds of substrates were employed to investigate the formation of KVs in the Sn/Cu joints during the thermal aging. Numbers of voids appeared at the Cu_3Sn/Cu interface in Sn/VS Cu and Sn/EP Cu joints, but not in Sn/HP Cu joints. The results implied that the formation of voids could be accelerated due to the small grain size and more diffusion paths due to numerous grain boundaries in the Sn/VS Cu interface. The combination of impurities and small grain size in EP Cu

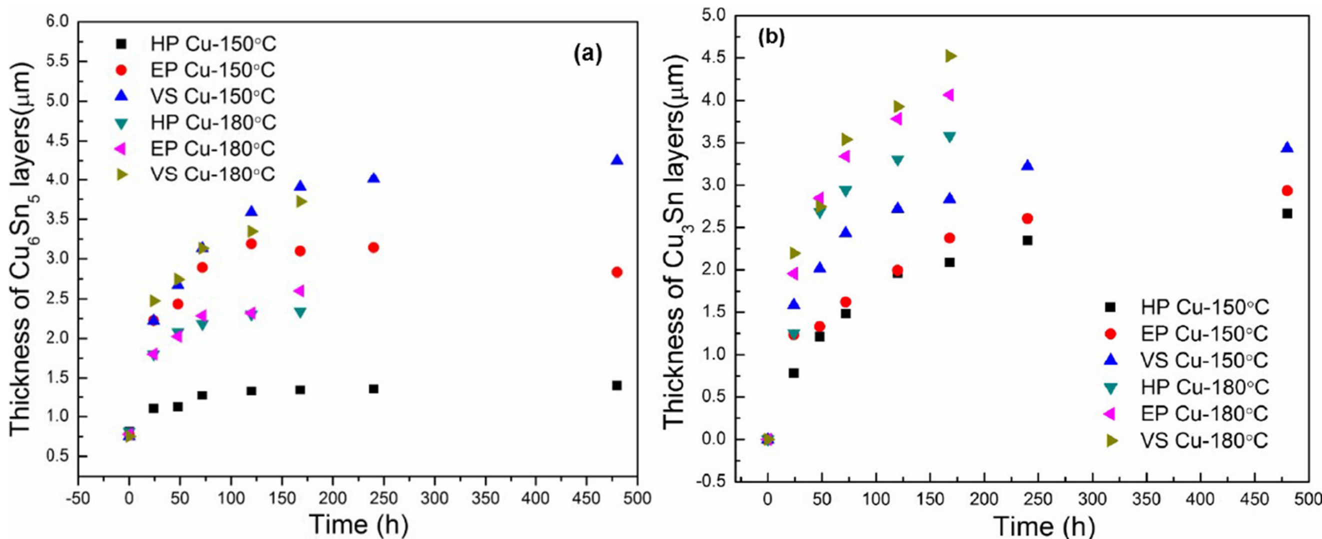

Fig. 5 Relationship between aging time and average thickness of (a) Cu_6Sn_5 and (b) Cu_3Sn layers in three kinds of joints

also promoted the formation of voids at the Sn/EP Cu interface. The size of these voids was much larger than that at the Sn/VS Cu interface. The high distribution of residual stress was developed at the Cu_3Sn/Cu interface in Sn/VS Cu and Sn/EP Cu joints, which would be helpful for the formation of voids.

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References

1. Baheti VA, Kashyap S, Kumar P, Chattopadhyay K, Paul A (2017) Bifurcation of the Kirkendall marker plane and the role of Ni and other impurities on the growth of Kirkendall voids in the Cu–Sn system. Acta Mater 131:260–270
2. Liashenko OY, Lay S, Hodaj F (2016) On the initial stages of phase formation at the solid Cu/liquid Sn-based solder interface. Acta Mater 117:216–227
3. Yang Y, Lu H, Yu C, Li Y (2011) Void formation at the interface in Sn/Cu solder joints. Microelectron Reliab 51(12):2314–2318
4. Buchovecky E, Jadhav N, Bower AF, Chason E (2009) Finite element modeling of stress evolution in Sn films due to growth of the Cu_6Sn_5 intermetallic compound. J Electron Mater 38(12):2676–2684
5. Yin L, Borgesen P (2011) On the root cause of Kirkendall voiding in Cu_3Sn. J Mater Res 26(3):455–466
6. Yu J, Kim JY (2008) Effects of residual S on Kirkendall void formation at Cu/Sn–3.5Ag solder joints. Acta Mater 56(19):5514–5523
7. Park JY, Seo W, Yoo S, Kim YH (2017) Effect of Cu electroplating parameters on microvoid formation and high-speed shear strength in Sn-3.0Ag-0.5Cu/Cu joints. J Alloys Compd 724(15):492–500
8. Kim JY, Yu J (2008) Effects of residual impurities in electroplated Cu on the Kirkendall void formation during soldering. Appl Phys Lett 92(9):947–1262
9. Kim J, Kim H (2010) Effects of organic additives on preferred plane and residual stress of copper electroplated on polyimide. Mater Chem Phys 120(2):341–347
10. Cho MG, Kang SK, Shih DY, Lee HM (2007) Effects of minor additions of Zn on interfacial reactions of Sn-Ag-Cu and Sn-Cu solders with various Cu substrates during thermal aging. J Electron Mater 36(11):1501–1509
11. Peter B, Liang Y, Pericles K (2011) Assessing the risk of "Kirkendall voiding" in Cu_3Sn. Microelectron Reliab 51(4):837–846
12. Zou J, Mo L, Wu F, Wang B (2010) Effect of Cu substrate and solder alloy on the formation of Kirkendall voids in the solder joints during thermal aging. International Conference on Electronic Packaging Technology & High Density Packaging IEEE :944–948
13. Yin L, Dimitrov N, Borgesen P (2012) Toward a better understanding of the effect of Cu electroplating process parameters on CuSn voiding. J Electron Mater 41(2):302–312
14. Liu Y, Wang J, Yin L, Kondos P, Parks C, Borgesen P, Henderson DW, Cotts EJ, Dimitrov N (2008) Influence of plating parameters and solution chemistry on the voiding propensity at electroplated copper–solder interface. J Appl Electrochem 38(12):1695–1705
15. Tu KN, Thompson RD (1982) Kinetics of interfacial reaction in bimetallic Cu-Sn thin films. Acta Metall 30(5):947–952
16. Kim S, Yu J (2012) Recrystallization-induced void migration in electroplated cu films. Scripta Mater 67(4):312–315
17. Porter DA, Easterling KE, Sherif M (1992) Phase transformations in metals and alloys, 2nd edition. Ref User Serv Q 1(2):245
18. Kumar S, Handwerker CA, Dayananda MA (2011) Intrinsic and interdiffusion in Cu-Sn system. J Phase Equilib Diff 32(4):309–319
19. Cheng EH, Kuo TT, Wang CC, Wu WH (2012) Inhibiting the growth of Cu_3Sn and Kirkendall voids in the Cu/Sn-Ag-Cu system by minor Pd alloying. Electron Mater Lett 8(5):495–501
20. Song JY, Yu J, Lee TY (2004) Effects of reactive diffusion on stress evolution in Cu–Sn films. Scripta Mater 51(2):167–170
21. Weinberg K, Böhme T, Müller WH (2009) Kirkendall voids in the intermetallic layers of solder joints in MEMS. Comput Mater Sci 45(3):827–831