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ORIGINAL ARTICLE

5-Input majority gate based optimized full adder circuit in nanoscale coplanar quantum-dot cellular automata

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Abstract

Quantum-dot cellular automata (QCA) is one of the alternative nanotechnologies that empower nanoscale circuit models with high performance and minimal energy depletion features. In this study, design for a 5-input majority gate (MV_5) is proposed. The reported design requires a smaller number of cells, lower time delay, less design cost, and area. The precision of this 5-in MV is confirmed by the theoretical validation, and the QCADesigner simulation engine is applied for proving the majority circuit with functionality. In addition, an optimized full adder (FAd) circuit is designed to consider the appropriateness of the proposed (MV_5). The outcomes exhibit that the designed full adder performs reliably well associated with contemporary multi-layer layouts, and executes well in the case of existing coplanar FAd circuits in all sides. The designed FAd obtains an improvement of 20% in terms of covered extent, 35% in cell extent, 32% in cell intricacy, 58% in delay, and 20% in cost correspondingly, as compared to its best counterpart. QCAPro, an energy valuation tool, is employed to assess the power consumption of the reported designs. The outcomes in this work corroborate that the hardware prerequisite for a QCA design is decreased, and circuits become simpler in gate counts and clock segments by considering the proposed design.

Keywords Nanoelectronics · Quantum-dot cellular automata · Majority gate · Full adder (FAd) · QCAPro

Introduction

Traditional complementary metal oxide semiconductor (CMOS) archetype has regulated our nanotechnology industry for over past decades; besides, it has sustained to be an effective replacement than preceding technologies [1, 2]. However, gradually a day will come when traditional CMOS technology of circuit designing will attain its shortcoming, and we will have to move to a contemporary technology [3]. Quantum-dot cellular automata (QCA) presents all images of becoming a dominant and improved substitute for the traditional CMOS archetype [4, 5]. In 1993, Lent et al. [1] presented QCA, and it was physically demonstrated in the year 1997 [1]. CMOS archetype is rigid to improve further due to limitations caused by short channel effect and continues to diminish the scope of gate oxides at the nanoscale. Moreover, there are far more scaling limitations in CMOS archetype [3–5]. Several researches are employed on devising nanoscale circuits with substitute techniques; for instance, single-electron transistor (SET) or QCA. Among them, QCA is notable due to its attractive features of small size, high performance, and minimal energy depletion [1, 2]. The notable advantage of QCA devices is the simplest connection among cells [6], where a correlation achieved only with adjacent cells; thus, the complete connection is not necessary [7, 8]. A number of QCA based digital devices have studied to date; designs for 5-input majority gate (MV) [9–18], designs of FAd [10, 14, 19–22], multipliers [23], dividers [24], memory circuits [25], counter [6] QCA based memory cells [26], flip flops [27–29], and multiplexer [30] have also been researched. The application of FAd is inevitable up-to-date transmission where accuracy performs an eminent function. Though the QCA archetype has some difficulties, and one of them is the absence of sophisticated QCA in industrial manufacture [31]. QCA is formed on the mutual repulsion

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and confinement of electrons, where the basic element is a squared cell with four quantum dots and two additional electrons inside [19, 20]. Moreover, it proposes a different view in data transmission where the data is conducted the transmission of polarization between QCA cells correspondingly. In this study, first, an effective 5-input QCA majority voter is designed, then using this majority voter, the design of FAd is realized. The foremost points of this study are as provided:

- Designing an effective single layer 5-input majority (MV_5) gate with minimal energy dissipation and cell intricacy.
- Based on the proposed majority voter, a single-layered design for FAd is proposed that utilizes minimal area, latency, cell, and cost compared to the best-listed one in the literature.
- Comparing the proposed MV_5 and FAd with other state-of-the-art designs regarding energy dissipation.

The MV_5 is a complex and one of the essential logical element in QCA. Many complex circuits can be designed without difficulty by MV_5. Up to now, several MV_5 structures are designed, but these designs face many lacking like layer availability, size, could not connect several designs. But, the proposed design solves these issues, and there is a possibility to add more designs with the inputs. The structural proof confirms constancy of the proposed MV_5 while energy estimation approves the low power utilization of designed MV. The designed FAd shows significance in the design, and experimental outcomes explain the significant enhancements in design level in terms of area, cell count, energy, and clock compared to that of traditional design styles.

The rest of the study is prepared as follows: "Preliminaries of quantum-dot cellular automata" presents an analysis of QCA structures with different kinds of crossing methods. "An analysis of 5-input majority gate" organizes a thorough study of existing MV5s. Moreover, the proposed majority voter accompanied by physical, resilient, and power study of preceding models is focused in this section. Later in "Designed Full Adder circuit in quantum-dot cells", the designed majority voter with a FAd circuit is provided along with simulation outcomes. A complete assessment of existing works with energy consumption is reviewed in "Comparative analysis with energy consumption models", and lastly, the study ends with a concluding part in "Conclusion".

Preliminaries of quantum-dot cellular automata

Some essential perceptions of QCA nanotechnology, like logical gates, wiring, clocking, and specific faults in QCA, are organized in this section.

Basic structures

The elementary computing component in QCA is a quantum cell, and every single cellblock encloses quartet quantum dots that are positioned in the four edges of a quadrangle. Every single quantum cell consists of pair electrons that mechanically tunnel concerning these dots through the minimal potential barrier. As shown in Fig. 1a concerning Coulombic revulsion potency, two steady formations of $P = +1$ and $P = -1$ are designed: which presents '1' and '0' in binary form correspondingly [1, 4]. QCA wires are formed with a structure of cells that are capable of emitting a response to the output signal. Two types of QCA wires, 90° and 45° are exhibited in Fig. 1b, and through the outline, it can be realized that the input in the 90° wire is shifted to the next phase starved of transform, however, in the 45° wire crossing, the feedback can be produced at the output phase.

The majority gate is measured as a significant block of QCA layouts. The 3-in MV is the vital analytical presentation in the QCA nanocircuits that determine the Boolean statement as presented:

$$MV(A, B, C) = AB + AC + BC, \quad (1)$$

Figure 1c presents the QCA illustration of a 3-in MV, and it should be stated that just fixing one of three inputs majority stable to '0' or '1', AND or OR operations can be generated [4]. Because of the remarkable space optimization of nanocircuits by the 3-in MV as assessed to silicon designed transistors, conceiving an optimum configuration for an MV_5 acquires many considerations, organized in Fig. 1d. The concept that amplifies the designing interest for this circuit in the study is its capability aimed at proposing the more well-organized FAd circuits [13]. The inverter is another vital block in QCA layouts. The cellular outlooks of the inverters are shown in Figure; where the first inverter circuit that is presented in Fig. 1e poses more cellblocks in contrast with the second one shown in Fig. 1f. The former inverter divergences the input into two routes and joins them by controlling a 45° wire that generates the contrasting polarization.

QCA clocking

QCA circuits need clock pulses so that the circuits operate properly. The clock pulse pursues two main objects. The first one is maintaining energy to circuits, and the next one is regulating data discharge in cells. The flow of electrons enabled by the clock pulses within cells; therefore, permit electrons to transform their formation in a pre-determined routine as well as adjust the blocks of channeling among the dots [4]. There are no power lineups in the QCA archetype. Clock zones allow the operation in a consecutive fashion [19, 20]. Generally, a clocking scheme contains four segments,

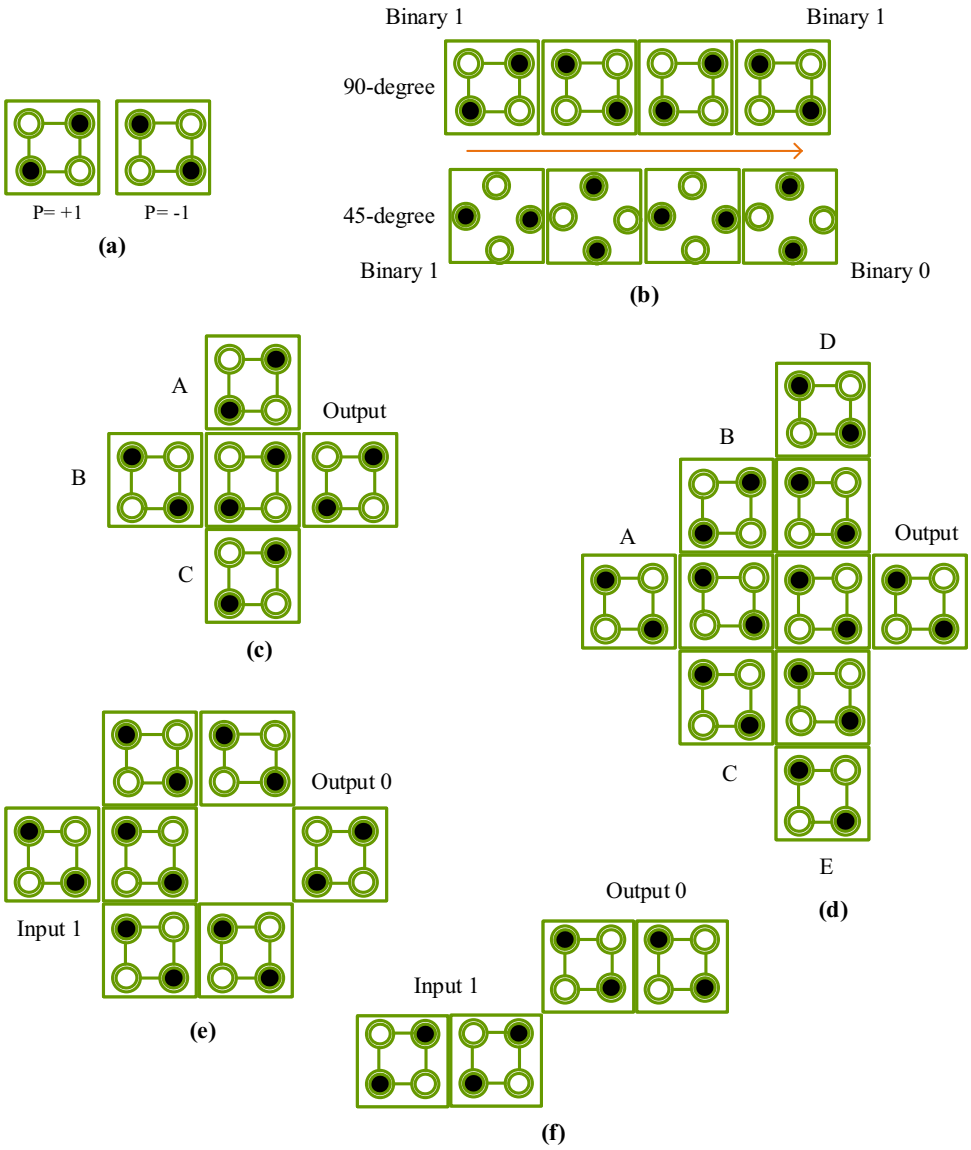

Fig. 1 QCA Structures; **a** basic cells, **b** 90° and 45° binary wire, **c** MV_3, **d** MV_5, **e** seven cell robust inverter, and **f** four-cell inverter

namely switch, hold, release, and relax, so explained in Fig. 2. Switch period introduces the procedure of cell polarization that remains up to the cell is fully polarized.

The cell retains its polarization once the clock pulse extents the higher level. The process is recognized as a hold phase. The diminution of the cellblock arises once the clock permits over the release phase. To end, the cell is un-polarized at the last clock pulse or Relax phase [32].

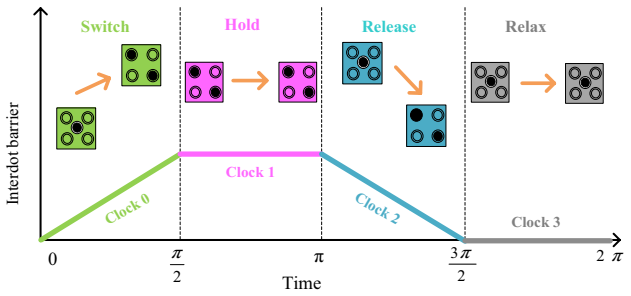

Fig. 2 Four phases clocking in QCA

Wire-crossing

In QCA configurations, interconnection design between elements requires to be controlled competently for an improved constancy. Until now, there are two distinct sorts of wire crossing are presented, namely, multi-layer and coplanar.

Several levels are employed as in-circuit layout for interconnection among QCA elements in a multi-layer design, as represented in Fig. 3a. Wiring is completed by distinct diploid

cells in coplanar crossing where these cells are rectangular to one another; therefore, they work exclusive of concerning adjoining cells. The first wire contains cells of 90° formations, and the second has 45° formations, as illustrated in Fig. 3b. One of the major shortcomings of this structure is that a little misalignment of cells throughout design might affect a cross-connecting between the two wires. Researches have been organized to lessen suchlike influences, as well to enhance the durability of the nanocircuits; nevertheless, these schemes turn out with oversized space overhead [33]. A special type of coplanar wiring is focused in Shin et al. [34] where a crossing is formed on the interference of clocking segments as presented in Fig. 3c.

QCA realization concerns

Molecular dots, metal islands, and semiconductor dots [35] are measured as QCA based archetypes [36]. Molecular dots have a precisely small extent and specify extreme frequency [37] where metal islands and semiconductor dots operate at minimal temperature. By recognizing the structural complications, all improvement could be materially applied. A major contentious limitation in applied QCA nanocircuits is their functional condition [4]. This minimum temperature is measured as a suitable division of a QCA cell [24]. Some surveys [35, 37] also have been carried out to review the possibility of expanding QCA temperature. These reviews illustrate the substantial aspects of the QCA by allowing QCA-designed circuits with excessive conditions.

Faults in QCA

Mostly, deficiencies in QCA ensue in the impeachment procedure. These faults are mainly separated into four groups, as presented:

- Cell exclusion or omission: this sort of fault arises by reason of the omission of one particular cell, as shown in Fig. 4a.
- Cell displacement: this category of defect arises because of the dislocation of cells from the primary position as exhibited in Fig. 4b.

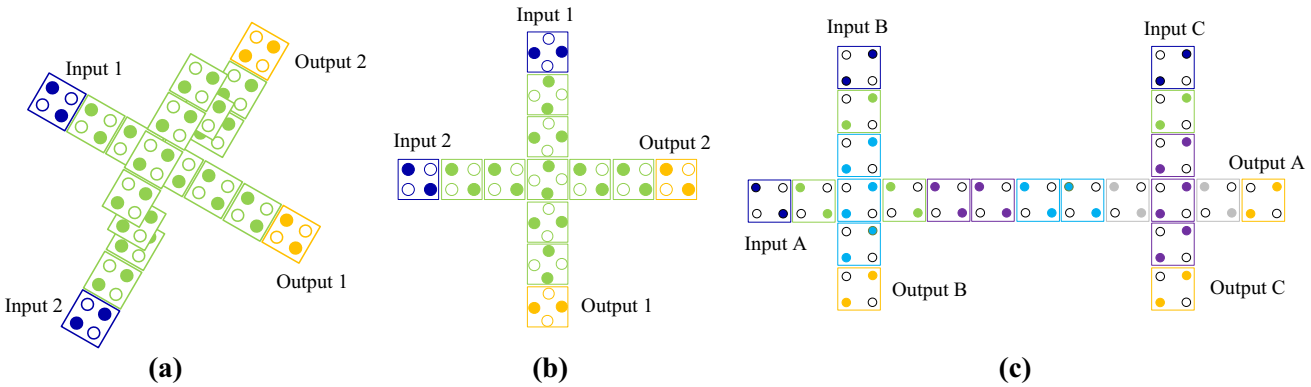

Fig. 3 Crossover in QCA **a** multi-layer, **b** coplanar, **c** wiring with single cell

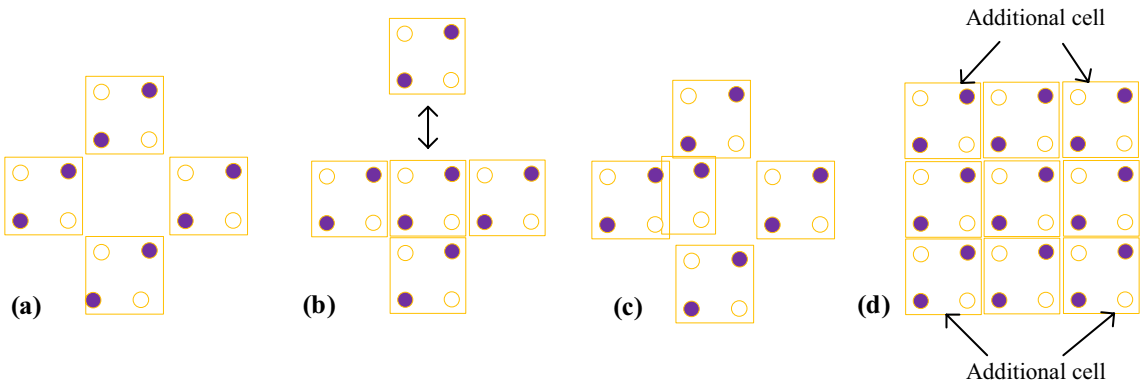

Fig. 4 Various kinds of faults in QCA; **a** exclusion, **b** displacement, **c** misalignment **d** extra cell accretion

- Cell misalignment: this kind of fault arises because of the misalignment of cells, as presented in Fig. 4c.
- Extra-cell accretion: this sort of fault arises by reason of the exclusion of the cell in bed, as shown in Fig. 4d.

An analysis of 5-input majority gate

For several years, nanocircuits based on QCA are developed with 3-input majority gates (3-in MV). In the meantime, specialists have presented the MV_5 schemes are well-organized concerning area occupied as well firm than the conventional ones. Each design integrates the identical synchronization style of 3-in MV. Already, a number of configurations for MV_5 have been focused [9–18]. The Boolean depiction of the MV_5 can be presented as follows:

$$\begin{aligned} MV_5(A, B, C, D, E) &= ABC + ABD + ABE + ACD + ACE \\ &\quad + ADE + BCD + BCE + BDE + CDE, \end{aligned} \tag{2}$$

The circuit design in [9], the output cell, is enclosed by input cells, which is problematic to contact the layout in a single crossing. The design in [10] undergoes from surplus consequence as input blocks are proximate enough to one another. Designs recommended in [11, 12] strove to alleviate the mentioned complications. A related study also has been presented in [13, 14]. A single layer design is proposed in [17] needs 11 cells, but the input cells are adjacent to each other. In [18], another layout is presented, which requires 11 cells, but this design encounters some polarization complications.

Structural proof

To substantiate a QCA gate, 32 distinctive input states are essential for a MV_5. In this study, we have deliberated only one position out of 32. We have studied $A=D=0$, $B=C=E=1$, to prove the precision of the proposed circuit. All the cells are equivalent dimension (18 × 18) nm, and the pair of adjoining cells are splitting by a distance of 2 nm. We have used a top-down approach to find potential energy. The estimation is counted from the adjoining cell of the output cell. The overall polarization is inverted at the output level. Using the adjacent cell of the output, there is no big impact on the considering cell to other cells. So, the overall estimation is accurate. Electrons are organized in such a method, which reduces their latent force to attain constancy. The force or energy U joining two charges is calculated with Eqs. (3) and (4), respectively [38]. The possible energy defined as U, between electron charges, is assessed from Eq. (5). In Eq. (3), K_{eq} is preset colon, and r is the space between electron charges:

$$U = \frac{K_{eq}}{r}, \tag{3}$$

$$K_{eq} = 9 \times 10^9 \times (1.6)^2 \times 10^{-38} = 23.04 \times 10^{-29} = A. \tag{4}$$

Two distinctive positions for electrons x and y are studied for cell 1, as indicated in Fig. 5a and b. The key concept following this is to locate a position that presents marginal latent energy.

For X electron,

$$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \approx 1.152 \times 10^{-20} J,$$

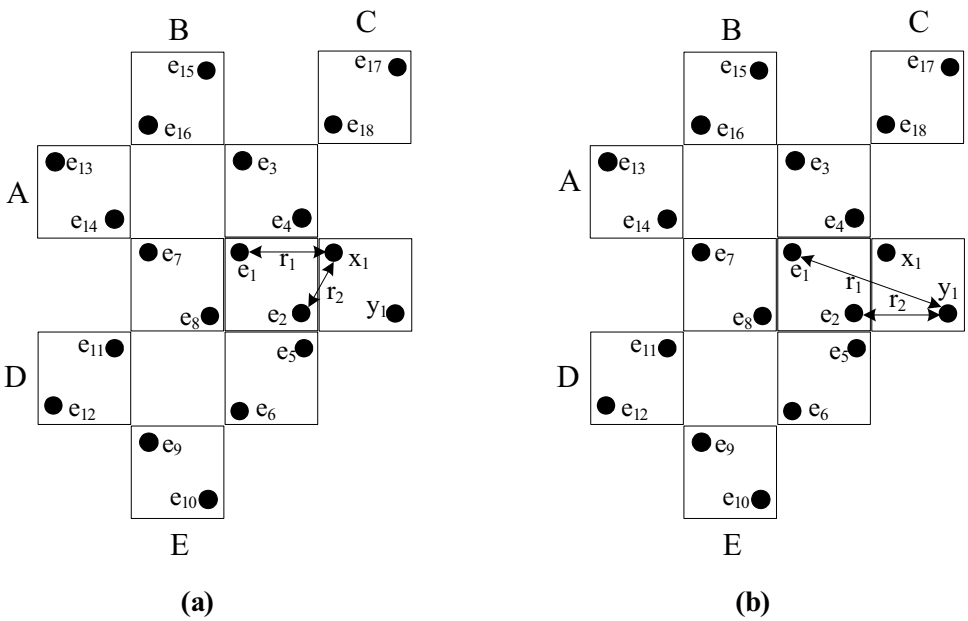

Fig. 5 First structure of cell position '0' where **a** electron x and **b** electron y

$$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} \approx 1.272 \times 10^{-20} J,$$

$$U_3 = \frac{A}{r_3} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} \approx 0.815 \times 10^{-20} J,$$

$$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{2.83 \times 10^{-9}} \approx 8.146 \times 10^{-20} J,$$

$$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{20.1 \times 10^{-9}} \approx 1.146 \times 10^{-20} J,$$

$$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{42.94 \times 10^{-9}} \approx 0.537 \times 10^{-20} J,$$

$$U_7 = \frac{A}{r_7} = \frac{23.04 \times 10^{-29}}{40 \times 10^{-9}} \approx 0.576 \times 10^{-20} J,$$

$$U_8 = \frac{A}{r_8} = \frac{23.04 \times 10^{-29}}{28.43 \times 10^{-9}} \approx 0.811 \times 10^{-20} J,$$

$$U_9 = \frac{A}{r_9} = \frac{23.04 \times 10^{-29}}{56.57 \times 10^{-9}} \approx 0.407 \times 10^{-20} J,$$

$$U_{10} = \frac{A}{r_{10}} = \frac{23.04 \times 10^{-29}}{62.03 \times 10^{-9}} \approx 0.371 \times 10^{-20} J,$$

$$U_{11} = \frac{A}{r_{11}} = \frac{23.04 \times 10^{-29}}{46.52 \times 10^{-9}} \approx 0.495 \times 10^{-20} J,$$

$$U_{12} = \frac{A}{r_{12}} = \frac{23.04 \times 10^{-29}}{71.02 \times 10^{-9}} \approx 0.324 \times 10^{-20} J,$$

$$U_{13} = \frac{A}{r_{13}} = \frac{23.04 \times 10^{-29}}{63.25 \times 10^{-9}} \approx 0.364 \times 10^{-20} J,$$

$$U_{14} = \frac{A}{r_{14}} = \frac{23.04 \times 10^{-29}}{42.05 \times 10^{-9}} \approx 0.548 \times 10^{-20} J,$$

$$U_{15} = \frac{A}{r_{15}} = \frac{23.04 \times 10^{-29}}{45.65 \times 10^{-9}} \approx 0.505 \times 10^{-20} J,$$

$$U_{16} = \frac{A}{r_{16}} = \frac{23.04 \times 10^{-29}}{45.65 \times 10^{-9}} \approx 0.505 \times 10^{-20} J,$$

$$U_{17} = \frac{A}{r_{17}} = \frac{23.04 \times 10^{-29}}{43.86 \times 10^{-9}} \approx 0.525 \times 10^{-20} J,$$

$$U_{18} = \frac{A}{r_{18}} = \frac{23.04 \times 10^{-29}}{22.00 \times 10^{-9}} \approx 1.047 \times 10^{-20} J,$$

$$U_{T_{X1}} = \sum_{i=1}^{18} U_i = 19.547 \times 10^{-20} J.$$

For Y electron,

$$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{42.05 \times 10^{-9}} \approx 0.548 \times 10^{-20} J,$$

$$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{20 \times 10^{-9}} \approx 1.152 \times 10^{-20} J,$$

$$U_3 = \frac{A}{r_3} = \frac{23.04 \times 10^{-29}}{53.74 \times 10^{-9}} \approx 0.429 \times 10^{-20} J,$$

$$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} \approx 0.815 \times 10^{-20} J,$$

$$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{20.1 \times 10^{-9}} \approx 1.146 \times 10^{-20} J,$$

$$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{42.94 \times 10^{-9}} \approx 0.537 \times 10^{-20} J,$$

$$U_7 = \frac{A}{r_7} = \frac{23.04 \times 10^{-29}}{60.73 \times 10^{-9}} \approx 0.379 \times 10^{-20} J,$$

$$U_8 = \frac{A}{r_8} = \frac{23.04 \times 10^{-29}}{40.00 \times 10^{-9}} \approx 0.576 \times 10^{-20} J,$$

$$U_9 = \frac{A}{r_9} = \frac{23.04 \times 10^{-29}}{62.03 \times 10^{-9}} \approx 0.371 \times 10^{-20} J,$$

$$U_{10} = \frac{A}{r_{10}} = \frac{23.04 \times 10^{-29}}{56.57 \times 10^{-9}} \approx 0.407 \times 10^{-20} J,$$

$$U_{11} = \frac{A}{r_{11}} = \frac{23.04 \times 10^{-29}}{60.03 \times 10^{-9}} \approx 0.384 \times 10^{-20} J,$$

$$U_{12} = \frac{A}{r_{12}} = \frac{23.04 \times 10^{-29}}{80.52 \times 10^{-9}} \approx 0.286 \times 10^{-20} J,$$

$$U_{13} = \frac{A}{r_{13}} = \frac{23.04 \times 10^{-29}}{86.76 \times 10^{-9}} \approx 0.266 \times 10^{-20} J,$$

$$U_{14} = \frac{A}{r_{14}} = \frac{23.04 \times 10^{-29}}{63.25 \times 10^{-9}} \approx 0.364 \times 10^{-20} J,$$

$$U_{15} = \frac{A}{r_{15}} = \frac{23.04 \times 10^{-29}}{70.46 \times 10^{-9}} \approx 0.327 \times 10^{-20} J,$$

$$U_{16} = \frac{A}{r_{16}} = \frac{23.04 \times 10^{-29}}{70.46 \times 10^{-9}} \approx 0.327 \times 10^{-20} J,$$

$$U_{17} = \frac{A}{r_{17}} = \frac{23.04 \times 10^{-29}}{58.00 \times 10^{-9}} \approx 0.397 \times 10^{-20} J,$$

$$U_{18} = \frac{A}{r_{18}} = \frac{23.04 \times 10^{-29}}{43.86 \times 10^{-9}} \approx 0.525 \times 10^{-20} J,$$

$$U_{T_{y1}} = \sum_{i=1}^{18} U_i = 9.236 \times 10^{-20} J,$$

$$U_{T_1} = 28.783 \times 10^{-20} J.$$

The same approach can be utilized to find the potential energy from a different state. We have considered another position of the design to find the energy, as presented in Fig. 6:

$$U_{T_{X2}} = \sum_{i=1}^{18} U_i = 9.430 \times 10^{-20} J,$$

$$U_{T_{y2}} = \sum_{i=1}^{18} U_i = 29.068 \times 10^{-20} J.$$

Total potential energy for< structure 2,

$$U_{T_2} = 38.498 \times 10^{-20} J.$$

For the complete latent energy of both *x* and *y*, regarding electrons in both positions are estimated using the mentioned equations. It is noticed that the position in structure 1 is steadier.

Physical investigation

The outlined majority voter contains 12 QCA cells where five cells are inputs, five cells are middle cells, and one output. An extra cell is used with the output block, which inverts the charge of the operations. The proposed gate has a significance that it is occupied in a single layer; thus, simple to contact the cells with no extra crossing in the gate. The outlined architecture is expedient and pliable, contrasting existing designs. The middle cells are polarized by input cells, but the output is less polarized due to the adjacent cell of the output. These influences transmit the mainstream result of responses to the corresponding output and consequence a MV_5. The output and feedback blocks are not confined by other cells that defeat the limitation within the aforementioned gates. The designed majority gate is indicated in Fig. 7a, and to authenticate the gate, simulation outcome has been exhibited in Fig. 7b. The proposed design attains anticipated outcomes with sophisticated polarization. Underlying investigation of the outlined design with all accessible designs is organized in Table 1, where quite a few imperative factors like cellblock intricacy, ratio, area

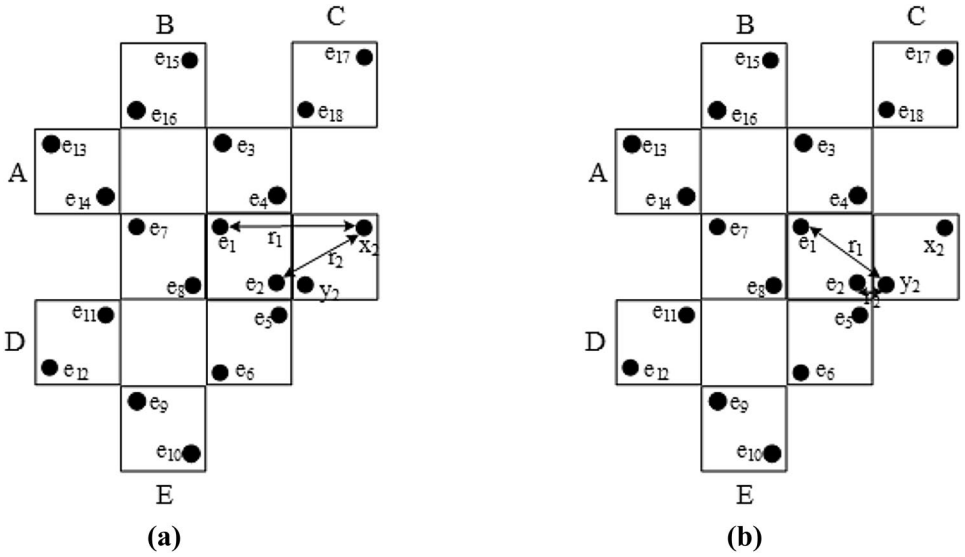

Fig. 6 The second structure of cell position '1' where **a** electron *x* and **b** electron y

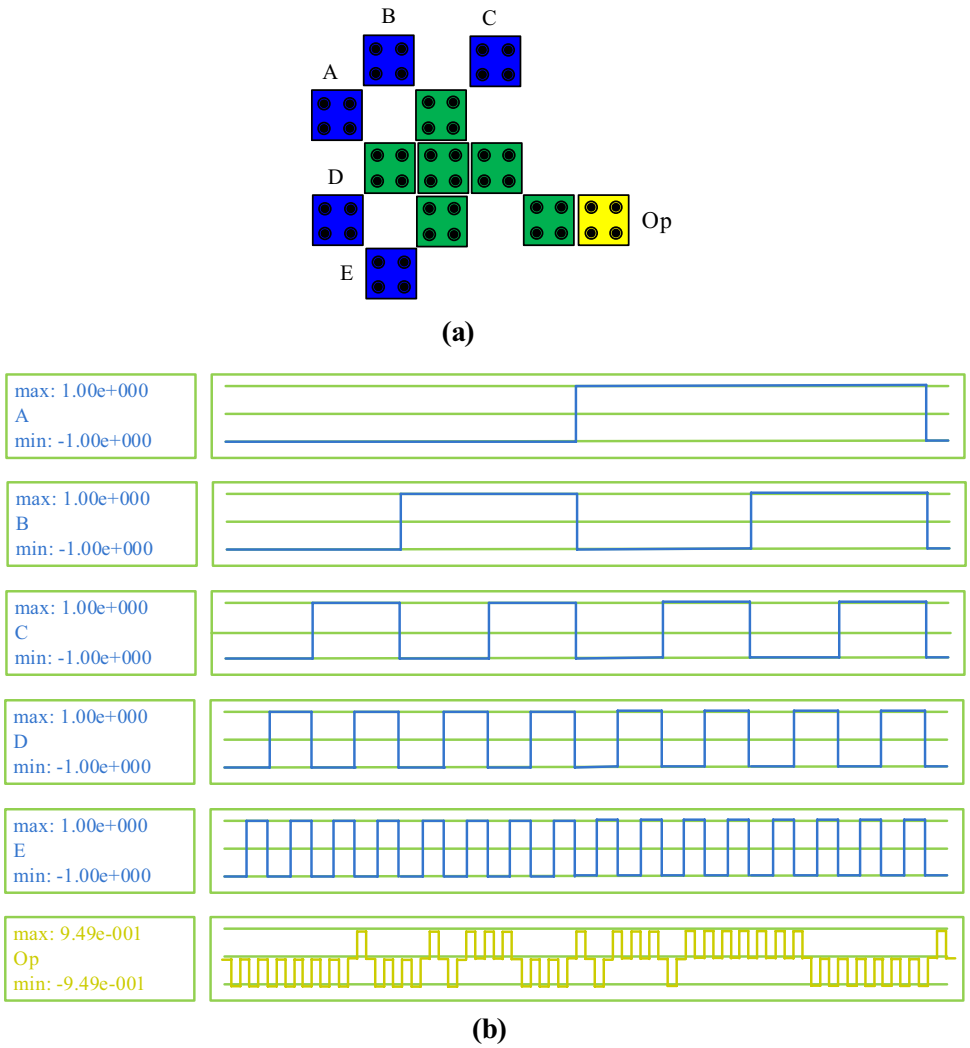

Fig. 7 The proposed structure of the majority gate (**a**) with simulation outcome (**b**)

Table 1 Investigation of the proposed and existing MV_5

Majority gate (MG) design	Cell intricacy	Ratio	Covered extent in (μm^2)	Cell area in (μm^2)	Polarization (e^{-001})	Ratio	Wire crossing
MG in [9]	10	0.83	0.004	0.0032	9.96	1.049	Multilayer
MG in [10]	10	0.83	0.007	0.0032	9.50	1.001	Multilayer
MG in [11]	18	1.50	0.016	0.0058	9.53	1.004	Single layer
MG in [12]	13	1.08	0.009	0.0042	8.24	0.868	Single layer
MG in [13]	23	1.92	0.024	0.0074	9.52	1.003	Single layer
MG in [14]	20	1.67	0.019	0.0064	–	–	Single layer
MG in [15]	13	1.08	0.009	0.0042	9.54	1.005	Multilayer
MG in [16]	17	1.41	0.018	0.0055	9.50	1.001	Single layer
MG in [16]	18	1.50	0.016	0.0058	9.50	1.001	Single layer
MG in [17]	11	0.91	0.009	0.0035	9.48	0.998	Single layer
MG in [18]	11	0.91	0.009	0.0035	9.49	1	Single layer
This study	12	1	0.010	0.0038	9.49	1	Single layer

engaged, polarization, and coplanar availability is considered. The designs in [9, 10, 17, 18] take fewer cells than the proposed one but take more extent for implementation moreover;, some designs are not entirely single layer accessible. The designed circuit indicates a noteworthy development concerning intricacy, polarization, ratio, the area covered, and coplanar availability in contrast to other layouts [9–18]. The outlined circuit relishes full availability to input and output cells.

Power analysis

To evaluate the overall energy dissipation of QCA circuits, a Hamiltonian matrix is focused. Hamiltonian matrix for a range of QCA cells can be determined with Hartree–Fock estimation and mean-field method interactivity [39] as presented in Eq. 3:

$$H = \begin{bmatrix} \frac{-E_k}{2}\sum_i X_i f_{i,j} & -\gamma \\ -\gamma & \frac{E_k}{2}\sum_i X_i f_{i,j} \end{bmatrix}. \quad (5)$$

In the above equation, X_i implies polarization of the ith adjoining cell, $f_{i,j}$ is the scientific aspect identifying the electrostatic line connecting cell i and j cells following the scientific plot, γ is the channeling potency connecting two logic positions of a cell and $\sum_i$ is the complete potential over the blocks.

The possible charge for a QCA cell energy at every single clock phase is estimated from the following equation:

$$E = \langle H \rangle = \frac{\hbar}{2}.\vec{\lambda}.\vec{\Gamma}. \quad (6)$$

In Eq. (4), $\hbar$ outlined as the Planck constant, $\vec{\Gamma}$ is the energy atmosphere vector, and $\vec{\lambda}$ is the coherence vector.

The power operations in a QCA cell are classified into four major points as P_{diss}, P_{clock}, P_{out}, and P_{in}. The operations of P_{out} and P_{in} are alike except P_{out} signifies the liquidated energy to the rightward cell, and P_{in} signifies the achieved energy from the leftward adjacent QCA cell [39]. Right through the switch stage, inter-dot cellblocks are steadily lifted, pointing to the transference of a suggestive degree of force to the cellblock, and in the release phase, the cellblocks are bit by bit lessened; therefore a part of the consuming force is folded back to the signaling level. Thus, there is a marginal energy lessening identified P_{diss}. The instantaneous comprehensive energy for a distinct cell can be assessed as:

$$P_s = \frac{dE}{dt} = \frac{\hbar}{2}\left[\vec{\lambda}.\frac{d\vec{\Gamma}}{dt}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\right]. \quad (7)$$

Two foremost factors implicated in Eq. (7): firstly, the enhancement of energy arrives at the variation of the feedback and output signal then afterward, assigned clocking signal or P_{clock} to the cellblock. The complete depleted power denoted by P_{diss}. The energy consumption of a cellblock in a particular cycle $T_{\text{ee}} = [-T, T]$ is attained in regard to Hamiltonian and Coherence vectors [40] as presented:

$$E_{diss} = \frac{\hbar}{2}\int_{-T}^{T} \vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\,dt = \frac{\hbar}{2}\left(\left[\vec{\lambda}.\vec{\Gamma}\right]_{-T}^{T} - \int_{-T}^{T} \vec{\lambda}.\frac{d\vec{\Gamma}}{dt}dt\right). \quad (8)$$

It is substantial to specify that even though the variation degree of $\vec{\Gamma}$ is uppermost, the highest energy will be dissipated. Weighing $\vec{\Gamma}_+$ and $\vec{\Gamma}_-$ separately, the energy depletion pattern of higher bound is acquired and presented in equation [9]:

$$P_{diss} = \frac{E_{diss}}{T_{ee}}\left\langle \frac{\hbar}{2T_{ee}}\vec{\Gamma}_+ \left[-\frac{\vec{\Gamma}_+}{\left|\vec{\Gamma}_+\right|}\tanh\left(\frac{\hbar\left|\vec{\Gamma}_+\right|}{K_z T}\right) + \frac{\vec{\Gamma}_-}{\left|\vec{\Gamma}_-\right|}\tanh\left(\frac{\hbar\left|\vec{\Gamma}_-\right|}{K_z T}\right)\right]\right\rangle. \quad (9)$$

In Eq. (9),$\vec{\Gamma}_+$ and $\vec{\Gamma}_-$ are the Hamiltonian assesses former and following the variation, T is the stable temperature, and K_z is the Boltzmann constant. A comparative study of the designed FAd with existing designs is presented in "Comparative analysis with energy consumption models".

Designed full adder circuit in quantum-dot cells

An immense significant arithmetic operation that arises in digital logic is the addition. Other mathematical functions like subtraction, multiplication, and division are fulfilled with adders. Thus, a constructive adder is indispensable being conniving the excessive performing arithmetic operations. A recent enhanced QCA FAd is organized in this part with an optimized five input majority voter.

The graphical representation of the outlined FAd is directed in Fig. 8a with the QCA circuit diagram in b, respectively. The outcomes of a FAd can be figured as presented:

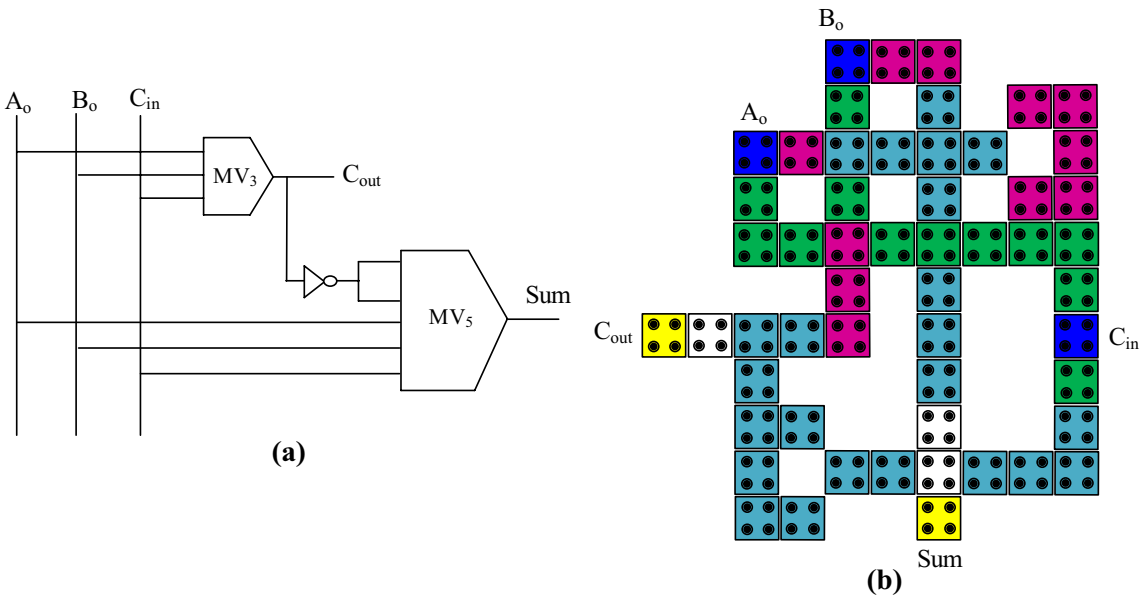

Fig. 8 Proposed FAd in schematic layout (**a**) QCA layout (**b**)

$$\text{Sum} = A \oplus B \oplus C_{\text{in}} = MG5(\bar{C_{\text{out}}}, \bar{C_{\text{out}}}, A, B, C_{\text{in}}), \tag{10}$$

$$C_{\text{out}} = AB + BC_{\text{in}} + AC_{\text{in}}. \tag{11}$$

As shown in Fig. 8, the logical layout for realizing the FAd is constituted of four key building blocks covering two basic inverters, one 3-in MV and MV_5. In the proposed circuit, a usual form of QCA cells is utilized, which has a well-organized outline for fabricating. Various research on FAd has been done so far [10, 14, 19–22], but maximum layouts are confined to 3-in MV.

Simulation tools

Walus et al. [32] proposed a competent software for QCA-based circuit design, QCADesigner, which is a widespread simulation engine for circuit design. This tool permits clients to draw as well as to authenticate a variety of assignments in QCA. The principle of this simulation tool is to form an expedient model and design that can be accessible spontaneously to the researchers. A significant design parameter is that other designers should be capable of integrating their own functionalities into QCADesigner [41]. In addition, simulation tools can be added into QCADesigner with a harmonized convening technique with data types. The existing copy of QCADesigner involves three modeling tools. The primary is a digital simulant that counts cellblocks to be either null or entirely diverged [32]. The next one is a nonlinear estimation approach that applies the nonlinear cell response method to state the persistent status of the cellblocks inside a layout [42]. The last one organizes an estimation of the extensive quantum automated paradigm of correspondent a system. Architecture might be distinct or multi-layered. In a single crossing outline, usual cellblocks rotated cells as well firm polarity cells can be occupied. Once a clock changes from one particular level to next, it passes over perpendicular cells. Afterward, at the top level, it transmits over crossover QCA cells. To conclude, it can go low to the core level over perpendicular cellblocks.

For energy depletion, QCAPro [40], a versatile engine for dissipated energy calculation, is utilized. QCAPro presently uses the design file produced from QCADesigner. With this design file, QCAPro can operate a rapid design assessment to check the value of outputs for all potential series of inputs. It originates the polarization probability of distinct cells in a circuit with an estimation technique. Therefore, the results acquired from this engine for polarization and energy depletion are a pessimistic estimation. This tool can be utilized to find out the average power deficiency, upper and lower power deficiency in a circuit through an input switching process [40].

Existing QCA FAd models

A number of full-adder circuits have been studied so far. In this part, the existing QCA adders are investigated. The design in [43] takes 95 QCA cells, 0.087 μm^2 area, delay 8 with quantum cost 0.1740. The design of Kianpour et al. [44] takes 69 cells, 0.07 μm^2 area, four clock phases with quantum cost 0.07. The design is coplanar. Roohi et al. [12] proposed a design with 58 cells, and the extent of 0.04 μm^2,

three clock phases, and cost are 0.03, but it is a multi-layer approach. In [14], a coplanar adder with 71 cell, 0.06 μm^2 extent, delay 3 and quantum cost 0.045 is proposed. Sen et al. [45] outlined a coplanar adder that incorporates 86 QCA cells, 0.08 μm^2 area, delay 4 with quantum cost 0.08. Mohammadi et al. [21] design an efficient adder with 38 cells, 0.02 μm^2 area, three clock phases with quantum cost 0.015, but the layout is a multi-layer. In [46, 47] two adders with 22 and 23 cell, 0.01 μm^2 area, delay 3 with quantum cost 0.007, respectively, is proposed. However, both designs are multi-layer. Another multi-layer adder design in [9] is proposed by Navi with 61 cells, 0.03 μm^2 area, clock phases 3 with quantum cost 0.0225. In [48], a design with 63 QCA cells, 0.05 μm^2 extent, delay 3, and quantum cost 0.0375 is proposed. Navi et al. [10] proposed another competent layout. But it was a multi-layer adder with 0.04 μm^2 extent, clock phases 3, 73 QCA cell with quantum cost 0.030. A coplanar design is proposed in [49] that contain 0.06 μm^2 extent, four clock phases, 60 QCA cell with quantum cost 0.060. Sonare et al. [50] design a layout with 95 cells, 0.12 μm^2 area, four clock phases, with quantum cost 0.120. A multi-layer adder in [51] with 0.06 μm^2 extent, four clock phases, 86 QCA cell, and quantum cost 0.060 is proposed by pudi. Besides, design with the XOR gate is presented in [19]. Most of the time, it is practicable to use a coplanar approach rather than multi-layers.

Outcome study

In recent, researches illustrate the rising demands for functional QCA-based circuits. A number of coplanar and multi-layer designs have been achieved so far. As clarified in Fig. 9, the simulation outcome of the proposed adder with three consecutive input. Intricacy, latency, and cost are measured as the major benefits of QCA design that outclass all the counterparts with significant supremacy.

The simulation outcome for all inputs A_o, B_o, and C_o are clarified in Fig. 9 and result indorse that the designed FAd performs well and specifies the opposite operation. In this design, A_o, B_o, and C_o are considered as inputs, and the output cells are considered as sum and C_{out}. For instance, the input combinations of $A_o = B_o = C_o = 1$, the precise outcomes combinations of $C_{\text{out}} = 1$ with sum = 1 are conceived, as illustrated in Fig. 9. The major significant waveshape attained commencing the carry-sum product, is formed following one clock cycle. For the input combination $\{A_o\ B_o\ C_o\} = \{000, 001, 010, 011, 100, 101, 110, 111\}$ all specific faulty results in the outcome sum are acquired: {01110001, 00001111, 11001100, 11010100, 01010101, 00101011, 10101010, 01001101, 00010111, 00110011}; moreover, each specific faulty results in C_{out} are acquired: {11101000, 00110011, 00001111, 01001101, 10001110}. The comparative investigation presents that the proposed structure has more compactness than the existing designs.

Comparative analysis with energy consumption models

A complete comparative study of designed and existing FAd is demonstrated in this section. Table 2 presents that the outlined QCA FAd expands the existing adders with regard to area, latency, cost as well as complexity. The comparison analysis organizes that the proposed adder is quite efficient compared to other coplanar and multi-layer adder circuits in [41, 43, 44, 14–16, 48, 49, 43–70]. Though fewer cells engaged in [15, 19, 21, 46, 47, 54, 60, 61], the outlined adder circuit in this study has enhanced performance. Moreover, the adder circuit designed in a single layer without using any rotating cell. It could be verified that extending the feedback and result appearances of the designed adder circuit indicates to further consistent response with the designed

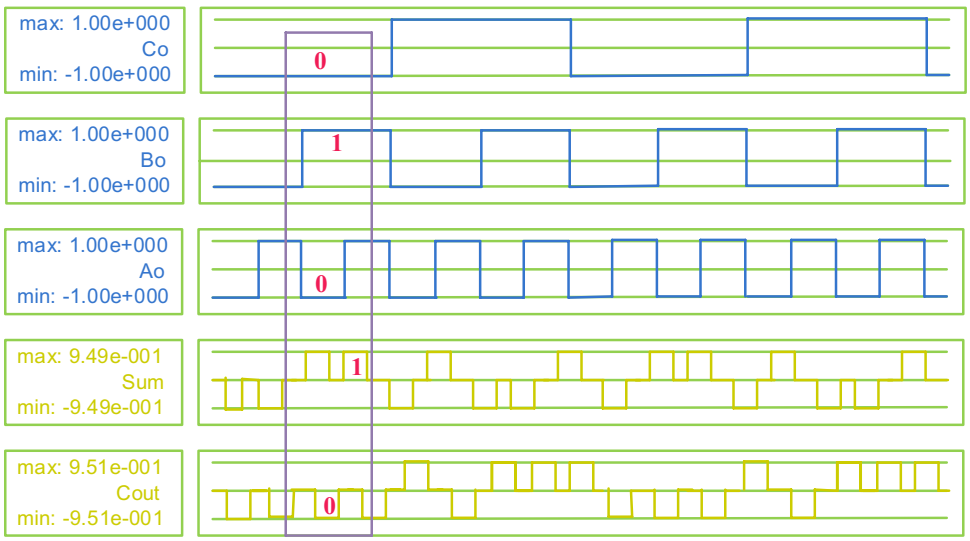

Fig. 9 Simulation outcome for outlined FAd

Table 2 Assessment of the QCA FAd circuits

Adders design	Covered extent in (μm^2)	Cell extent in (μm^2)	(%) of area utilization	Cell intricacy	Delay (clock phase)	Wire crossing	Cost	Ratio
In [9]	0.03	0.020	66.67	61	3	Multilayer	0.0225	0.75
In [10]	0.04	0.024	60.00	73	3	Multilayer	0.0300	1.00
In [12]	0.04	0.019	47.50	58	3	Multilayer	0.0300	1.00
In [14]	0.06	0.023	38.33	71	3	Coplanar	0.0450	1.50
In [15]	0.02	0.010	50.00	31	2	Multilayer	0.0100	0.33
In [16]	0.05	0.026	52.00	79	7	Multilayer	0.0375	1.25
In [19]	0.02	0.009	45.00	28	2	Coplanar	0.0100	0.33
In [21]	0.02	0.012	60.00	38	3	Multilayer	0.0150	0.50
In [22]	0.10	0.040	40.00	124	5	Coplanar	0.1250	4.17
In [23]	0.09	0.025	27.78	78	3	Coplanar	0.0675	2.25
In [24]	0.14	0.034	24.29	105	3	Multilayer	0.1050	3.50
In [41]	0.62	0.095	15.32	292	14	Coplanar	2.1700	72.33
In [43]	0.087	0.031	35.63	95	8	Coplanar	0.1740	5.80
In [44]	0.07	0.022	31.43	69	4	Coplanar	0.0700	2.33
In [45]	0.08	0.028	35.00	86	4	Coplanar	0.0800	2.67
In [46]	0.01	0.007	70.00	22	3	Multilayer	0.0075	0.25
In [47]	0.01	0.007	70.00	23	3	Multilayer	0.0075	0.25
In [48]	0.05	0.020	40.00	63	3	Coplanar	0.0375	1.25
In [49]	0.06	0.019	31.67	60	4	Coplanar	0.0600	2.00
In [50]	0.12	0.031	25.83	95	4	Coplanar	0.1200	4.00
In [51]	0.06	0.028	46.67	86	4	Multilayer	0.0600	2.00
In [52]	0.08	0.035	43.75	108	4	Coplanar	0.0800	2.67
In [53]	0.043	0.019	44.19	59	4	Coplanar	0.0430	1.43
In [54]	0.02	0.010	50.00	31	2	Multilayer	0.0100	0.33
In [55]	0.17	0.047	27.65	145	4	Coplanar	0.1700	5.67
In [56]	$>0.9\times2$	N/A	N/A	$>107\times2$	N/A	Coplanar	N/A	N/A
In [57]	0.10	0.035	35.00	108	4	Coplanar	0.1000	3.33
In [58]	0.36	0.071	19.72	220	3	Coplanar	0.2700	9.00
In [59]	0.20	0.062	31.00	192	N/A	Coplanar	N/A	N/A
In [60]	0.02	0.011	55.00	33	3	Multilayer	0.0150	0.50
In [61]	0.004	0.010	250.00	30	4	Multilayer	0.0040	0.13
In [62]	0.14	0.044	31.43	135	5	Multilayer	0.1750	5.83
In [63]	0.087	0.030	34.48	93	1	Multilayer	0.0217	0.72
In [64]	0.09	0.027	30.00	82	3	Multilayer	0.0675	2.25
In [65]	0.03	0.020	66.67	61	3	Multilayer	0.0225	0.75
In [66]	0.16	0.047	29.38	145	1	Coplanar	0.0400	1.33
In [67]	0.097	0.033	34.02	102	2	Coplanar	0.0485	1.62
In [68]	0.07	0.023	32.86	70	1	Multilayer	0.0175	0.58
In [69]	0.1008	0.038	37.70	118	3	Multilayer	0.0756	2.52
In [70]	0.10	0.031	31.00	96	2	Multilayer	0.0500	1.67
Proposed	0.04	0.017	–	54	3	Coplanar	0.0300	1.00

adder is beyond consistent around fluctuating the appearance shapes than the model. Besides, congruity with existing layouts, convenience to the feedbacks, and results with the pliability for modifying the size of the input and product appearances are other benefits of the outlined adder. The assessment between the designed adder outline and existing outlines are illustrated in Table 2. In Table 2, area utilization, cost, and ratio can be found using the following equations:

$$\text{Area usage} = [\text{Cell extent in } (\mu m^2) \,/\, \text{Covered extent in } (\mu m^2)] \times 100, \tag{12}$$

$$\text{Cost} = [\text{Covered extent} \times \text{Latency}], \tag{13}$$

$$\text{Ratio} = [\text{Referenced } cost \times \text{Proposed } cost]. \tag{14}$$

Relative improvement assessment

The proposed adder has a precise solid outline and an identical potential with the existing preeminent models. Besides, the design encompasses a minimum number of inverters and majority gates. The proposed design has 33, 27, 24, and 33% progress regarding the enclosed extent, cell area, cell intricacy with cost, separately, in contrast with [14]. In contrast with the designed adder in [16], our design has 20, 35, 32, 58, and 20% enhancements in extent, cell extent, cell count, delay, and cost parameters, correspondingly. Similarly, designed FAd received improvements of 60, 58, 57, 40, and 76% in terms of area, cell area, cell count, delay, and cost parameters compared with [22]. Compared to [55], the proposed design obtained an enhancement of 76, 64, 63, 25, and 82% in terms of area, cell area, cell count, delay, and cost parameters. In contrast with the designed FAd in [58], our design obtains an extreme improvement. It has 88, 76, 75, 58, and 88% enhancements in extent, cell extent, cell count, and cost parameters, correspondingly. Maximum improvements are achieved with [41], where almost 93, 82, 81, 78, and 98% improvements are attained in terms of area, cell area, cell count, delay, and cost parameters, respectively. Besides, our proposed adder has the convenience of output cells. Other improvements with corresponding parameters are presented in Figs. 10 and 11. Though some design enclosed the same or less area than the proposed design [9, 10, 12, 15, 19, 21, 46, 47, 60, 65]. Likewise, design [15, 19, 21, 46, 47, 61] has less cell area, design [19, 21, 46, 47, 54, 60, 61] consumed less cell, design [9, 10, 12, 14, 15, 19, 21, 23, 24, 46–48, 54, 58, 63–70] has equal or less delay, and design [9, 10, 12, 15, 21, 46, 47, 54, 60, 61, 63, 68] has fewer quantum cost than the proposed design. But all the mentioned adder circuits are designed in a multi-layer approach. Thus, these circuits have some design sophistication.

The proposed adder takes a minimal cell with lower latency, area, and quantum cost. Moreover, it is designed for avoiding a multi-layer approach. A comprehensive analysis concerning the extent, cell extent, cell complication, delay, and cost are presented in Fig. 11. From Fig. 11a, it is

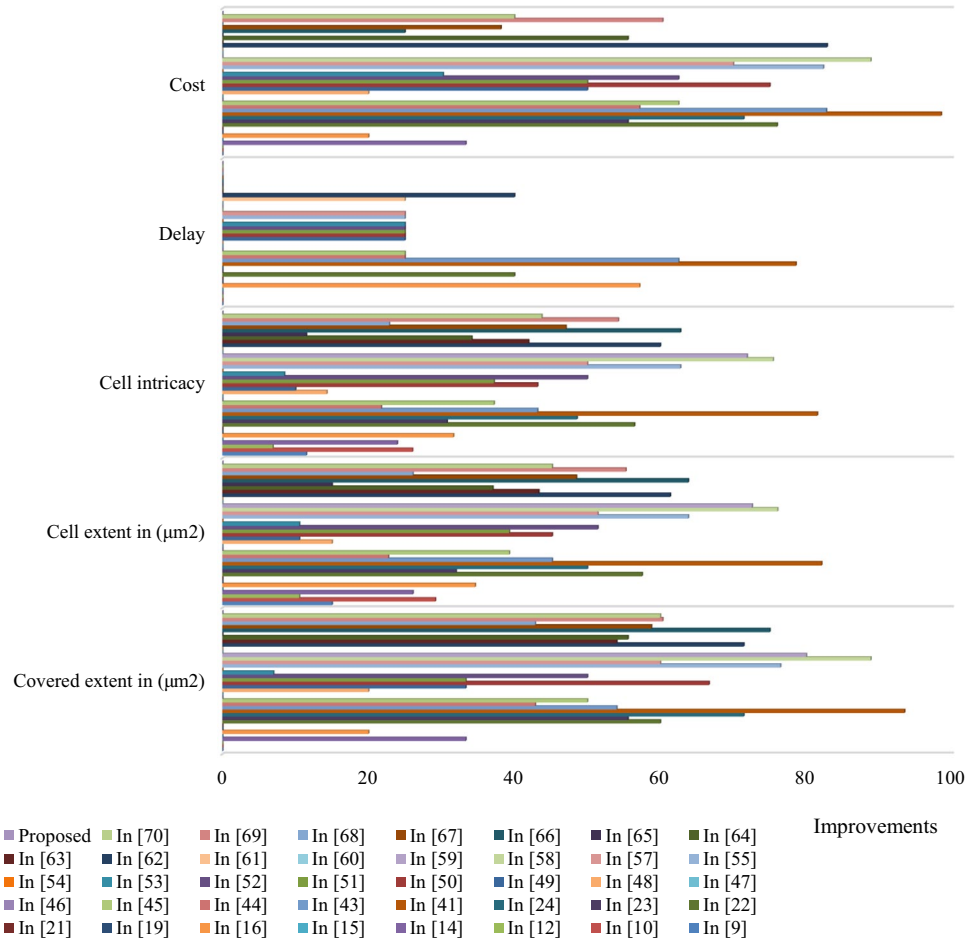

Fig. 10 Improvement assessment for proposed adder with existing

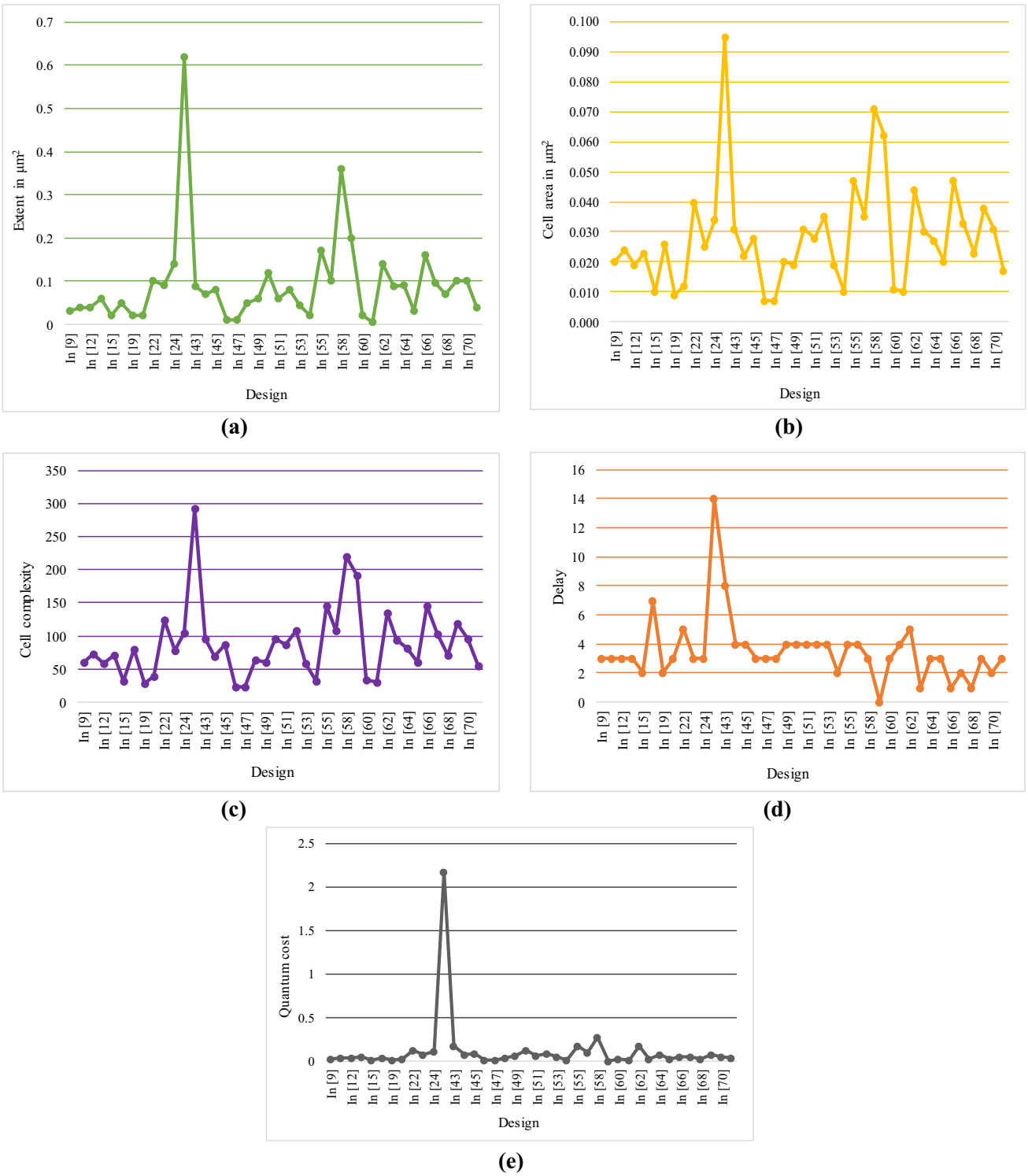

Fig. 11 Assessment of the proposed adder to existing adders regarding **a** extent, **b** cell area, **c** cell complexity, **d** delay and (e) quantum cost

perceived that the proposed FAd contains a minimal extent. As in [14] and [23], these designs have an extent of 0.06 μm^2 and 0.09 μm^2, respectively, where the extent of the proposed design is 0.04 μm^2. Similarly, the proposed design shows its improvements over the existing design. Though some design consumes less extent, like [9, 15, 46]; however, those designs are multilayered circuits.

The maximum extent of 0.62 μm^2 in [41] shows the highest peak of the figure. Figure 11b illustrates the cell extent of the presented design, where the proposed FAd has a minimal cell extent of 0.017 μm^2 than existing. The highest cell extent is 0.0095 μm^2 designed in [41]. Cell complication is presented in Fig. 11c, where it shows the proposed FAd takes 54 cells. Most of the design presented in the figure contains more cells than the proposed. However, several designs like [15, 46, 47, 60, 61] take a fewer cells, but these designs have multi-layer limitations. The delay of the layouts is presented in Fig. 11d where the highest delay is 14 for the design in [41], and the lowest is 1 for [63, 66, 68]. The delay of our design is three clock phases, and compared to [63, 66, 68], the design in [63, 68] is both multi-layer and [66] contains more extent and cell extent than proposed design. Figure 11e shows the quantum cost, where the highest cost is 2.17 for design [41]. The proposed FAd has a cost of 0.03, which is quite beneficial than the existing design.

Energy dissipation study

For measuring the overall energy depletion of the proposed majority voter and FAd, QCAPro [40] has been utilized as an energy assessor tool. This simulation engine mainly used to find out thorough dissipated energy [71]. Though others approach like Hamming distance [72], QCADesigner-Energy [19] is used in many researches. For estimation, three distinct channeling energies are acquired (0.5 E_k, 1.0 E_k, 1.5 E_k) at 2 K temperature. Figure 12 illustrates the energy depletion charts of the proposed majority voter and FA circuit with directing the energy of 1.0 E_k. Cells with extreme energy deletion are signified by more dark colors in thermal hotspot plots. A relative evaluation of energy depletion of designed majority voter and FAd circuit is represented in Tables 3 and 4 correspondingly, where outflow and switching energies influence to overall power depletion. From Tables 3 and 4, it is perceived that designed circuits reach minor energy depletion in contrast to all standing coplanar MV_5 and FAds.

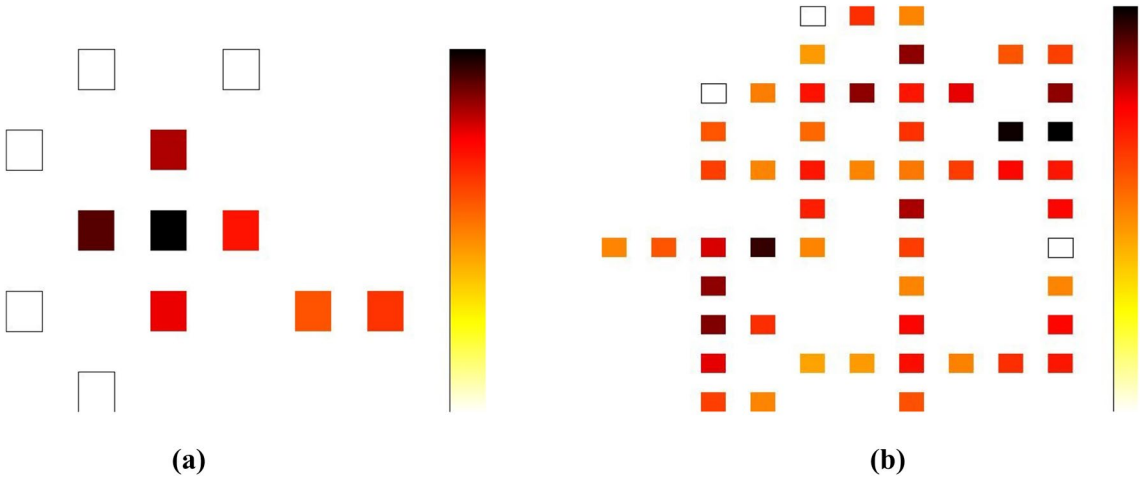

Fig. 12 Energy consumption plots for designed **a** MV_5 and **b** full adder at 2 K temperature and channeling energy of 1.0 E_k

Table 3 Energy consumption analysis of MV_5

Majority gate layout	Average leakage energy in (meV)			Average switching energy in (meV)			Total energy in (meV)		
	0.5 E_k	1.0 E_k	1.5 E_k	0.5 E_k	1.0 E_k	1.5 E_k	0.5 E_k	1.0 E_k	1.5 E_k
Layout in [9]	1.35	4.25	7.8	10.94	9.84	8.7	12.29	14.09	16.5
Layout in [10]	1.28	4.14	7.69	11.53	10.37	9.16	12.81	14.51	16.85
Layout in [11]	3.44	10.67	19.52	32.66	29.89	27.01	36.1	40.56	46.53
Layout in [12]	3.38	8.95	15.03	9.23	7.7	6.41	12.61	16.65	21.44
Layout in [13]	4.44	14.25	26.61	45.51	41.59	37.29	49.96	55.84	63.90
Layout in [14]	4.41	13.55	24.73	31.24	28.31	25.21	35.66	41.85	49.94
Layout in [17]	2.99	7.73	12.35	3.69	2.77	2.15	6.68	10.5	14.5
Layout in [18]	2.00	5.53	9.41	5.9	4.80	3.90	7.90	10.34	13.31
This work	3.17e − 9	8.19e − 9	1.35e − 8	7.05e − 9	5.72e − 9	4.7e − 9	1.02e − 8	1.39e − 8	1.82e − 8

Table 4 Energy consumption analysis of FAd circuits

FAd layout	Leakage energy in (meV)			Switching energy in (meV)			Total energy in (meV)		
	0.5 E_k	1.0 E_k	1.5 E_k	0.5 E_k	1.0 E_k	1.5 E_k	0.5 E_k	1.0 E_k	1.5 E_k
Layout in [44]	32.4	94.31	165.27	111.12	96	81.65	143.52	190.31	246.92
Layout in [53]	4.00e − 8	1.18e − 7	2.08e − 7	1.81e − 7	1.53e − 7	1.28e − 7	2.21e − 7	2.72e − 7	3.37e − 7
Layout in [55]	9.00e − 8	2.40e − 7	4.02e − 7	1.66e − 7	1.32e − 7	1.07e − − 7	2.56e − 7	3.73e − 7	5.09e − 7
Layout in [59]	1.07e − 7	2.90e − 7	4.95e − 7	2.02e − 7	1.70e − 7	1.42e − 7	3.09e − 7	4.60e − 7	6.38e − 7
Layout in [63]	244.50			164.56			409.05		
Layout in [65]	2.65e − 8	8.13e − 8	1.47e − 7	1.59e − 7	1.40e − 7	1.21e − 7	1.85e − 7	2.21e − 7	2.69e − 7
Layout in [67]	160.06			87.89			247.95		
Layout in [69]	34.80	105.84	190.63	210.97	185.36	160.00	245.78	291.20	350.62
Layout in [70]	26.14	80.98	147.47	112.37	99.16	85.91	138.51	180.14	233.38
Layout in [73]	10.66	31.57	55.44	54.19	46.19	40.18	64.85	78.36	95.63
Layout in [74]	31.2	83.79	140.62	65.84	60.83	49.51	97.04	144.62	190.13
Layout in [75]	14.05	39.32	68.02	50.61	44.67	38.95	64.66	83.99	106.97
Layout in [76]	57.88	158.38	269.1	114.19	95.62	80.07	172.07	254.00	349.17
Layout in [77]	17.57	52.95	94.50	80.77	70.77	61.13	98.34	123.72	155.63
This work	15.4	45.7	82.79	92.12	76.87	65.21	107.52	122.57	148.00

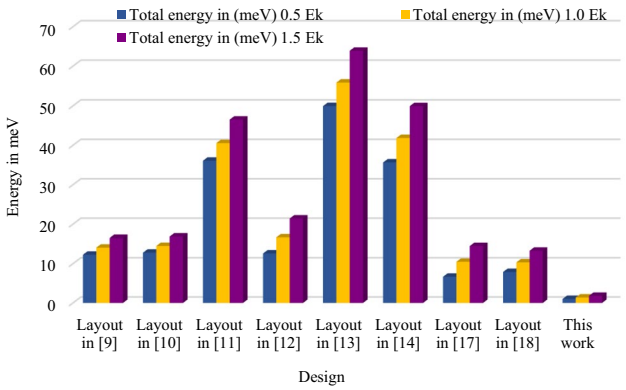

Fig. 13 Assessment of dissipated energy under different tunneling energy for MV_5

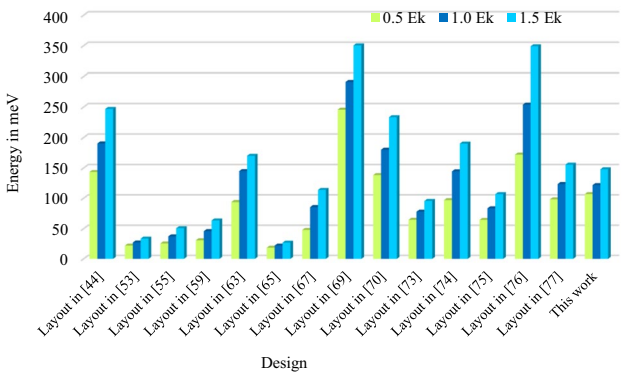

Fig. 14 Assessment of dissipated energy below different tunneling energy for FAds

Figures 13 and 14 are presented for entire energy depletion for all proposed designs to enhanced readability. From Fig. 13, it is obvious that the proposed majority voter energy depletion performance is superior over the design in [9–14, 17, 18]. As compared with [11], total depleted energy at 0.5 E_k, 1.0 E_k, 1.5 E_k channeling energy is 36.1 meV, 40.56 meV and 46.53 meV, correspondingly but in the proposed design the overall depletion rate is very low e.g. 1.02e − 8 meV, 1.39e − 8 meV and 1.82e − 8 meV correspondingly. The proposed design is very beneficial as compared with design in [18]. The design in [18] takes 7.90 meV, 10.34 meV and 13.31 meV energy from three distinct energy levels at 2 K temperature. Similarly, assess with its best counterpart in [13], the design consume huge energy at different channeling energy e.g. 49.96 meV, 55.84 meV and 63.90 meV correspondingly but the proposed design shows incredible performance by consuming minimal energy. Other comparisons for majority voter are effected in Fig. 13. In Fig. 14, it is noticeable that proposed design FAd is exceeding over the design in [44, 53, 55, 59, 63, 65, 67, 69, 70, 73–77].

Comparing to adder in [44], the design consumes 143.52 meV, 190.31 meV and 246.92 meV energy at three different energy levels of 0.5 E_k, 1.0 E_k, 1.5 E_k while in the proposed design, it takes 107.52 meV, 122.57 meV and 148.00 meV, respectively. The design in [70], consumes 138.51 meV, 180.14 meV and 233.38 meV energy which is quite high than the proposed design. In [76], the design dissipates huge energy 172.07 meV, 254.00 meV and 349.17 meV at three different energy levels at 2 K temperature. However, the designed FAd dissipates minimal energy at the same temperature. Though the design in [53, 55, 59,

65, 67, 75] dissipates minimal energy although these design has several intrications for instance, area utilization, total number of cell, delay, cell extent and wire crossing. The proposed FAd shows improved performance regards these issues. It is significant observing that the overall energy depletion of the outlined circuits is quite reduced associated to the remaining designs. This low energy and reduced extent aspects allow designers to comprehend complex and low power QCA circuits. The temperature position on the result polarization of proposed designs is comprehended at various temperatures by QCADesigner software [78]. The average or standard output polarization (AOP) for all QCA block is estimated as of [79, 80]. Both designs operate capably in the temperature range of 1–12 K, with the AOP for each QCA cellblock, which is distorted quite small to this extent.

Conclusion

In this study, a modified proficient MV_5 has been designed with substantial proofs. To sustenance this, a thorough assessment of structures and energy concerns of all previous designs and proposed MV_5 were performed. QCADesigner 2.0.3, a widely used simulation engine was applied to evaluate the circuits and power is assessed through QCAPro tool. Next, a refurbished low energy depleted FAd circuit is proposed to represent the effectiveness of the proposed MV_5. The designed FAd focuses on the coplanar layout; besides, it is practical that this coplanar configuration is efficient for significant adaptation in temperature with concedes more solid digital circuits respecting existing coplanar models. The simulation outcomes verified that the proposed circuits have overtaken all aforementioned layouts with regard to the cost function and indicated noteworthy enhancements in terms of cell intricacy, the area covered, energy depletion, and input–output clock delay in assessment to most of the multi-layer and coplanar designs. The outlined preeminent structures can make it possible for designing more composite and high-functioning nanoscale QCA circuits in the future.

Compliance with ethical standards

Conflict of interest The authors declare no potential conflict of interest in the manuscript.

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