J. Inst. Eng. India Ser. B (October 2023) 104(5):1023–1033
https://doi.org/10.1007/s40031-023-00910-2

ORIGINAL CONTRIBUTION

A High-Q Floating Active Inductor Based VCO for L-Band and Lower C-Band Applications in 180 nm CMOS Technology

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Received: 2 April 2023 / Accepted: 22 July 2023 / Published online: 8 August 2023

Abstract This paper presents a low power, wide-tuned Inductor-capacitor (LC) voltage-controlled oscillator (VCO). A floating active inductor (FAI) with a high-quality factor (Q) is used in the VCO design. The FAI is designed with a cascode transistor pair and a cross-coupled transistor pair to achieve a high Q value of up to 3290. The inductance value of the FAI ranges from 12.5 nH to 256.2 nH. The VCO has 164.8% of oscillation frequency tuning, from 235 MHz to 2.83 GHz with a phase noise of −85.3 dBc/Hz to −102.4 dBc/Hz at 1 MHz offset frequency. The FAI and VCO have 17.1×18 μm^2 and 58.6×64.6 μm^2 silicon area respectively. The power consumption ranges from 6.8 mW to 8.62 mW within the frequency tuning range. The FAI and VCO are designed in UMC 0.18 μm mixed-mode CMOS technology.

Keywords Accumulation mode metal oxide semiconductor transistor (AMOS) · Cross-coupled transistor pair (XCP) · Floating active inductor (FAI) · Voltage-controlled oscillator (VCO) · Quality factor (Q)

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Introduction

Today the world demands new technologies such as the Internet of Things (IoT), cognitive radio, etc. The connectivity among the devices in these technologies are mostly the very popular short-range wireless standards such as Bluetooth (IEEE 802.15.1), Wi-Fi (IEEE 802.11b/g/n), LTE (Long Term Evolution) in L Band and lower C Band in mobile phones and other devices. To support all these standards in one radio frequency integrated circuit (RFIC) [1], a device needs multiple fixed narrowband RF transceiver chips [2]. But this consumes more power and area, at a very high cost. The alternative solution is a single-chip reconfigurable RF transceiver supporting multiple wireless standards with more effective hardware sharing [3]. A voltage-controlled oscillator (VCO) is responsible for signal generation with different frequencies and reconfiguration in the context of frequency synthesis and clocking in the transceiver.

In the current scenario, the industry demands wideband, reconfigurable, low area, low power, and cost-effective VCO with reasonable phase noise. VCOs are classified as (i) ring (relaxation) VCO, well-known for their wide tuning range, low power, and low area, (ii) LC (harmonic) VCO [4] better known for its low phase noise. The tuning capability of the LC VCOs is enhanced using variable capacitors and tunable on-chip passive inductors [5]. Although the tunable passive inductors have a high Q value, they require isolation from the neighboring elements to avoid electromagnetic interference consuming much more area and it makes the chip

design complex and costly. Implementing active inductors (AIs) is the best way to get rid of these issues as they have tunable and high-valued quality factors and inductance. Both quantities are dependent on the transistor parameters, used for the realization of AI. The transistor parameters can be varied by changing the biasing conditions of the transistors which in turn tune the AI properties. At the same time, AIs suffer from noise, non-linearity, and power consumption issues. Nonlinearity and power consumption can be reduced to a greater extent with the proper design of the AI, but the noise needs to be compromised. So as a measure of performance generally the Figure of Merit (FoM) is calculated for the VCO which will be discussed later in this paper.

In this work, the design of a high-Q floating active inductor (FAI) and its use in a reconfigurable multiband VCO for a broad range of wireless applications is presented. The subsequent sections are presented as follows: Section II highlights the basic principles of the AI and the VCO using AI. Section III presents the proposed design of FAI and the design of VCO. The post-layout simulation results are discussed in Section IV, and the entire work is concluded in Section V.

Basics of Active Inductor and VCO

The current trend in RFIC is to make smaller ICs without compromising their performance. In this way, the active components are replaced by their passive on-chip counterparts. Here we address the fundamentals of AI and VCO using the active elements.

Active Inductor

AIs are basically of self-biased type [6], boot-strapped type [7], and gyrator-C type [8, 9] as shown in Fig. 1. The self-biased type of AI (Fig. 1a) has low- Q but provides a high voltage swing with the least area and power consumption. It suffers from voltage headroom issues. The boot-strapped AI (Fig. 1b) has a transformer for its realization making it bulky. It exploits the current amplification between two spirals of the integrated transformer and enhances the equivalent inductance value as seen from the input of AI as well as the Q-value. The inductance is proportional to the amplification of the transconductance stage. It is suitable for very high frequency, such as millimeter-wave applications. The most popular one is the gyrator-C AI (Fig. 1c), due to its high Q value, high inductance value, and wide frequency range. It consists of two transconductors, one positive and one negative, connected back-to-back.

The equivalent circuit of AI consists of a parallel R-L-C network, comprising the parasitic resistances and capacitances of the active devices. These parasitics reduce the Q-value of the AI. Different circuit topologies, namely, cascode structures [10], feedback structures [11–14], and negative resistance structures [15, 16] are incorporated in the basic gyrator-C AI circuit to improve the Q-value.

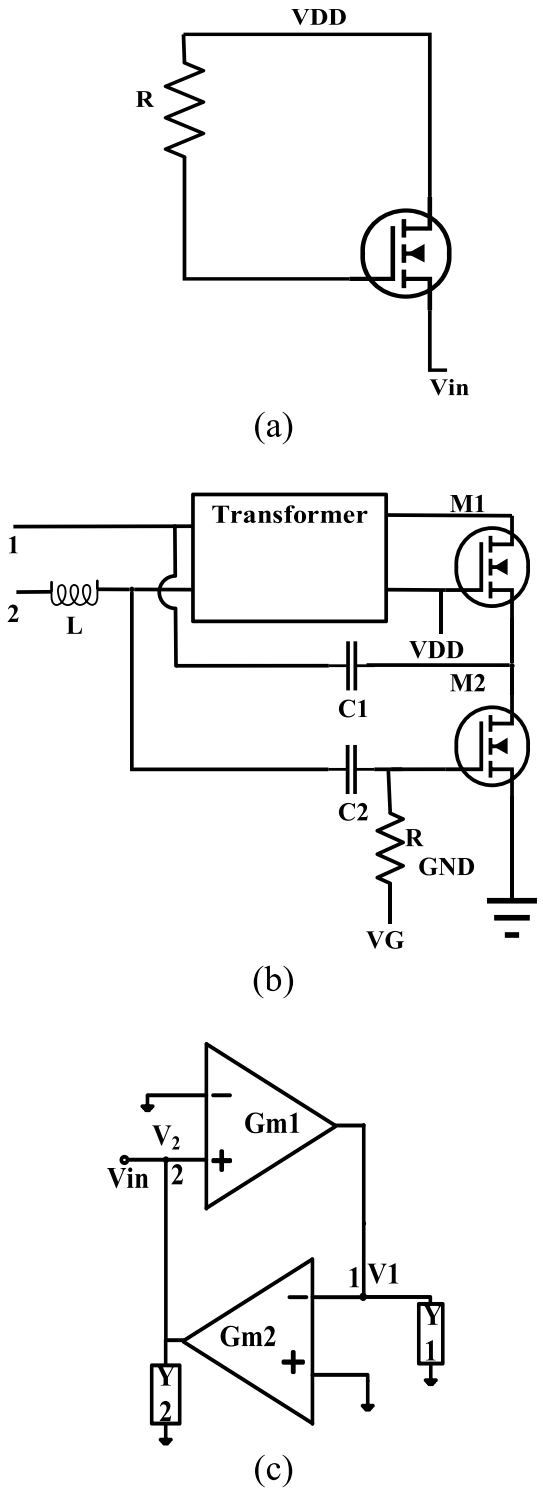


Fig. 1 Types of active inductors; **a** self-biased, **b** bootstrapped and **c** gyrator-C

AIs are categorized into single-ended AI (SAI) [16] and floating AI (FAI) [10, 17, 18]. The FAI has certain advantages over SAI like the voltage swing can be made double that in SAI and if the FAI has a symmetrical structure, it can reject the common-mode disturbances and becomes more suitable to be used in the VCOs. The SAI [16] has a cascode structure and a cross-coupled structure that provide negative resistance to compensate for the parasitic losses in the circuit, thereby improving its Q value.

Low power, wideband, differential input differential output operational transconductance amplifiers (OTAs) have been used in [10] to realize the FAI. The FAI [12, 19] has an additive capacitor technique with the transistors operating in the sub-threshold region by reducing the operating currents and so the power consumption. But it affects the frequency tuning range and the frequency of oscillation. A regulated cascode structure in addition to resistive feedback configuration is used to implement the FAI [20]. The regulated cascode structure reduces the series resistance loss to improve the quality factor of the FAI. But the use of the feedback resistance introduces thermal noise in the circuit.

Voltage Controlled Oscillator

The most popular LC VCOs used in the RFICs are Hartley VCO [21], Colpitts VCO [22], and cross-coupled VCO [11]. Cross-coupled VCOs are focused in this paper. Figure 2 shows the conventional top-biased cross-coupled LC VCO [23]. It consists of an LC tank and a core (a cross-coupled pair of nMOS transistors) which provides negative resistance to compensate for the loss introduced by the LC tank circuit.

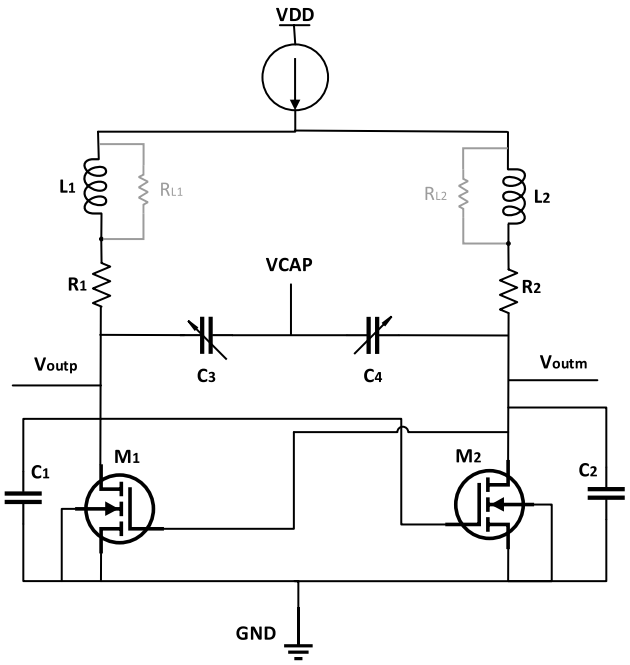


Fig. 2 Circuit diagram of a conventional VCO

The current trend in RFICs is the massive use of active elements to save die area. The passive capacitors are replaced by MOS varactors such as inversion mode MOS transistors (IMOS) or accumulation mode MOS transistors (AMOS) [24] or capacitor banks [25]. One of the major problems of using a passive inductor in VCO (Fig. 2) is that it is very difficult to predict the resistances associated with passive inductors like R_{L1} and R_{L2}, and so to design the negative resistance circuit (M_1, M_2). One of the possible solutions is to replace the passive inductors with active inductors.

In [17], SAI is used in the VCO design which is connected to the supply. But this type of design introduces the noise from the supply in the circuit. To avoid this, the current source is placed in between the inductor and the supply. FAI is used in the VCO design [19] along with AMOS as the varactor. A wider transistor of the AMOS can result in higher frequency tuning. The voltage swing of the oscillator is maintained by the circuit itself as the increase in controlled voltage of the FAI is taken care of by the voltage headroom of the constituent transistors. In addition to the buffer, the circuits can also be used at the VCO outputs for a better output.

Design of Proposed FAI and VCO

Proposed FAI

The proposed FAI as shown in Fig. 3 is used for a bandpass filter realization in sub-GHz applications [26]. A cascode transistor structure and a cross-coupled transistor pair [27] are used for its realization. The widths of transistors are also modified for high-frequency applications. Here, compensation of parasitic resistance present in the FAI is discussed through a more detailed analysis of the half symmetry small-signal equivalent circuit of FAI as shown in Fig. 4. In this case, C_{gsi}, C_{gdi}, and g_{mi} are the gate to source capacitance, the gate to drain capacitance, and the transconductance of transistors M_i (i = 1, 2, 3, 4), respectively. The derived input impedance from the small-signal equivalent circuit between the terminals LP/LM and the ground is given in (1).

$$Z_{in-L} = \frac{s^2 C_{gs3}\left(C_{gs1} + C_{gs4}\right) + sC_{gs3}g_{m4}}{s^2 C_{gs2}C_{gs3}g_{m4} + sC_{gs3}g_{m2}\left(g_{m4} - g_{m1}\right) + g_{m2}g_{m3}g_{m4}} \quad (1)$$

The (1) can be represented in the form of (2) to match the equivalent circuit of the FAI as shown in Fig. 5.

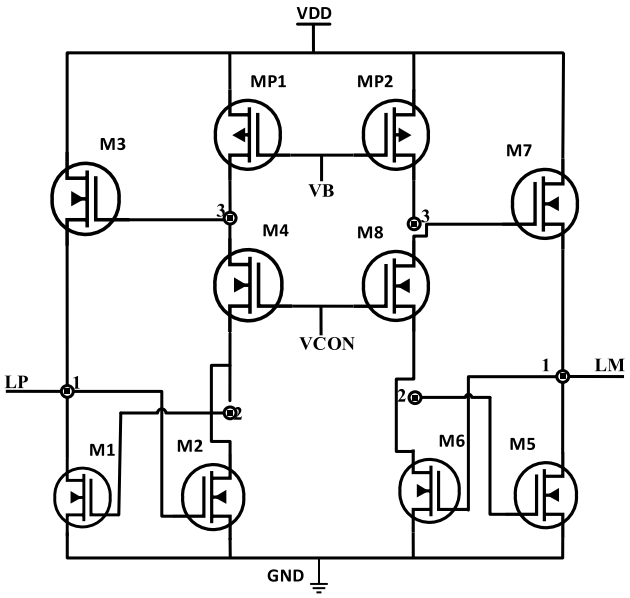


Fig. 3 Circuit diagram of the proposed FAI

$$Z(s) = \frac{s^2 R_{se} + s\frac{1}{C_{pl}}}{s^2 + s\frac{1}{R_{npl}C_{pl}} + \frac{1}{L_{se}C_{pl}}} \tag{2}$$

Different parameters of the FAI such as inductance (L_{se}), negative parallel resistance in the circuit due to the cross-coupled transistor structure (R_{npl}), parallel capacitance (C_{pl}), equivalent parallel resistance of R_S (R_{eq}), self-resonant frequency (ω_0) and Q are derived from (1), in-line with [8] and [28], also presented in (3) to (9).

$$L_{se} = \frac{C_{gs3}}{g_{m2}g_{m3}} \tag{3}$$

$$R_{se} = \frac{C_{gs1}+C_{gs4}}{g_{m4}C_{gs2}} \tag{4}$$

$$C_{pl} = C_{gs2} \tag{5}$$

$$R_{npl} = -\frac{g_{m4}}{g_{m2}(g_{m1}-g_{m4})} \tag{6}$$

$$R_{eq} = \frac{L_{se}}{C_{pl}R_{se}} = \frac{g_{m4}C_{gs3}}{g_{m2}g_{m3}(C_{gs1}+C_{gs4})} \tag{7}$$

$$\omega_0^2 = \frac{g_{m2}g_{m3}}{C_{gs3}C_{gs2}} \tag{8}$$

$$Q_{eff} = \frac{\omega_0 C_{pl}}{\frac{1}{R_{eq}} + \frac{1}{R_{pl}}} = \frac{\omega_0 g_{m4} C_{gs2} C_{gs3}}{g_{m2}g_{m3}g_{m4}(C_{gs1}+C_{gs4}) + g_{m2}g_{m4}(g_{m1}-g_{m4})C_{gs3}} \tag{9}$$

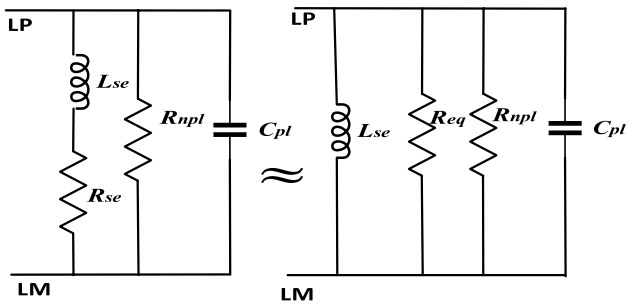


Fig. 5 RLC equivalent circuit of proposed FAI

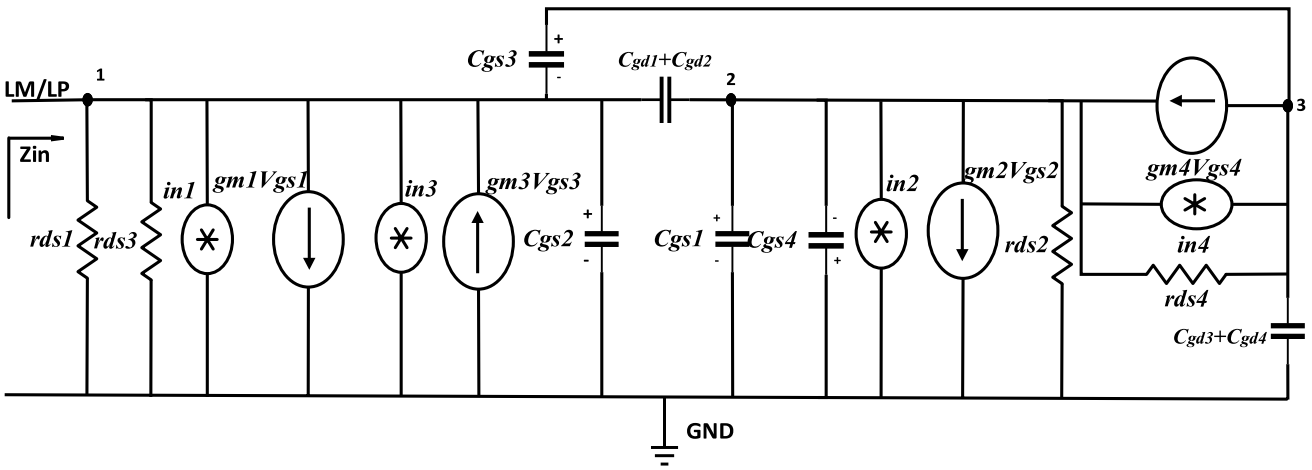


Fig. 4 Small-signal equivalent circuit of half symmetry of proposed FAI

When R_{npl} is equal to R_{eq} there is no loss in the FAI. So the condition for the FAI to be lossless is

$$g_{m3}\left(C_{gs1}+C_{gs4}\right)=C_{gs3}\left(g_{m4}-g_{m1}\right) \tag{10}$$

Taking $C_{gs3}=5.22$ fF, $C_{gs1}=5.35$ fF, $C_{gs4}=7.15$ fF, $g_{m3}=0.476$ mS, $g_{m1}=0.466$ mS, and, $g_{m4}=1.517$ mS for VB = 1.2 V and VCON = 847 mV, it may be noted that the left-hand side and right-hand side of (10) are almost equal. This shows the nullification of parasitic resistance associated with the FAI. Further, the channel noise (both thermal and Flicker noise) of the transistors (as shown in Fig. 4) is only considered to calculate the input-referred noise spectral density of the FAI. The small signal analysis leads to the following set of equations

$$DV=i_1, DV=i_2, DV=i_3, DV=i_4 \tag{11}$$

where

$$D=\begin{bmatrix} B & -\left(g_{m1}+sC_3\right) & g_{m3}+sCgs_3 \\ g_{m2}-sC_3 & A & -g_{ds4} \\ -sC_{gs3} & -\left(g_{m4}+g_{ds4}\right) & g_{ds4}+sC_4 \end{bmatrix},$$

$$V=\begin{bmatrix} V_{n1} \\ V_{n2} \\ V_{n3} \end{bmatrix}, \quad i_1=\begin{bmatrix} i_{n1} \\ 0 \\ 0 \end{bmatrix}, \quad i_2=\begin{bmatrix} 0 \\ i_{n2} \\ 0 \end{bmatrix},$$

$$i_3=\begin{bmatrix} i_{n3} \\ 0 \\ 0 \end{bmatrix}, \quad i_4=\begin{bmatrix} 0 \\ i_{n4} \\ -i_{n4} \end{bmatrix},$$

$$A=g_{m4}+g_{ds2}+g_{ds4}+sC_1,$$

$$B=g_{m3}+g_{ds1}+g_{ds3}+sC_2,$$

$$C_1=C_{gs1}+C_{gs4}+C_{gs1}+C_{gs2},$$

$$C_2=C_{gs2}+C_{gs3}+C_{gd1}+C_{gd2},$$

$$C_3=C_{gd1}+C_{gd2},$$

$$C_4=C_{gs3}+C_{gd3}+C_{gd4}.$$

If V_n is the input-referred noise voltage at the terminal LP (LM) then it can be expressed as

$$V_n^2=\sum V_{ni}^2, \quad i=1,\ 2,\ 3,\ 4 \tag{12}$$

where V_{ni} is the input-referred noise spectral density due to the individual transistor given as:

$$V_{ni}=\frac{N|_{i_{ni}}}{|D|}$$

where i_{ni} is the channel noise of the transistor M_i, consisting of thermal noise and flicker noise, represented as

$$i_{ni}^2=\left[8kT\gamma g_{di0}+\frac{K_f I_{Di}^{AF}}{C_{oxi}L_{effi}^2 f^{EF}}\right]\Delta f \tag{13}$$

where k = Boltzmann's constant, T = absolute temperature, γ is technology-dependent constant, C_{ox} is gate oxide capacitance, K_f is flicker noise co-efficient, AF is the flicker noise exponent, and g_{d0} is the drain-source conductance at zero V_{ds}. Thus,

Proposed VCO

The flicker noise minimization using a top-biased approach is presented to improve the VCO phase noise [29]. Based on this design, Fig. 6 shows the proposed VCO, in which the passive inductors are replaced by the proposed FAI (Fig. 3). The variable capacitors (C_3, C_4) are designed with the accumulation MOS Transistor pair (AMOS) varactors, and the current source is implemented by a current mirror. In the proposed VCO, the transistor M_{11} acts as a resistor and is solely responsible for the current flow in the VCO. The capacitance C is used to cancel the noise raised from the higher-order harmonics. The small resistances R_1 and R_2 are used for biasing the FAIs. The top-biased approach [30] is followed here to improve the VCO phase noise. By doing so, less flicker noise is upconverted to phase noise as compared to other techniques. But the amplitude of the VCO output is less due to the loss arising from the resonator loading.

$$N|_{i_{n1}}=i_{n1}\left[A\cdot\left(g_{ds4}+sC_4\right)-g_{ds4}\left(g_{m4}+g_{ds4}\right)\right]$$

$$N|_{i_{n2}}=i_{n2}\left[\left(g_{m4}+g_{ds4}\right)\left(g_{m3}+sC_{gs3}\right)-\left(g_{m1}-sC_3\right)\left(g_{ds4}+sC_4\right)\right]$$

$$N|_{i_{n3}}=i_{n3}\left[A\cdot sC_5+g_{ds1}\left(g_{ds2}+sC_1\right)\right]$$

$$N|_{i_{n4}}=i_{n4}\left[\left(g_{m1}+sC_3\right)\left(g_{m2}-s(C_3+C_{gs3})-B\left(A+\left(g_{m4}+g_{ds4}\right)\right)\right)\right]$$

$$\begin{aligned}|D|=&A\left[sC_{gs3}\left(g_{m3}+sC_{gs3}\right)-BsC_4\right)]\\&-B\left(g_{ds2}g_{ds4}+s^2C_3C_4\right)-\left(g_{m1}-sC_3\right)\\&\left[g_{ds4}sC_{gs3}+\left(g_{m2}-sC_3\right)\left(g_{ds4}+sC_2\right)\right]\\&-\left(g_{m2}-sC_3\right)\left(g_{m4}+g_{ds4}\right)\left(g_{m3}+sC_{s3}\right)\end{aligned}$$

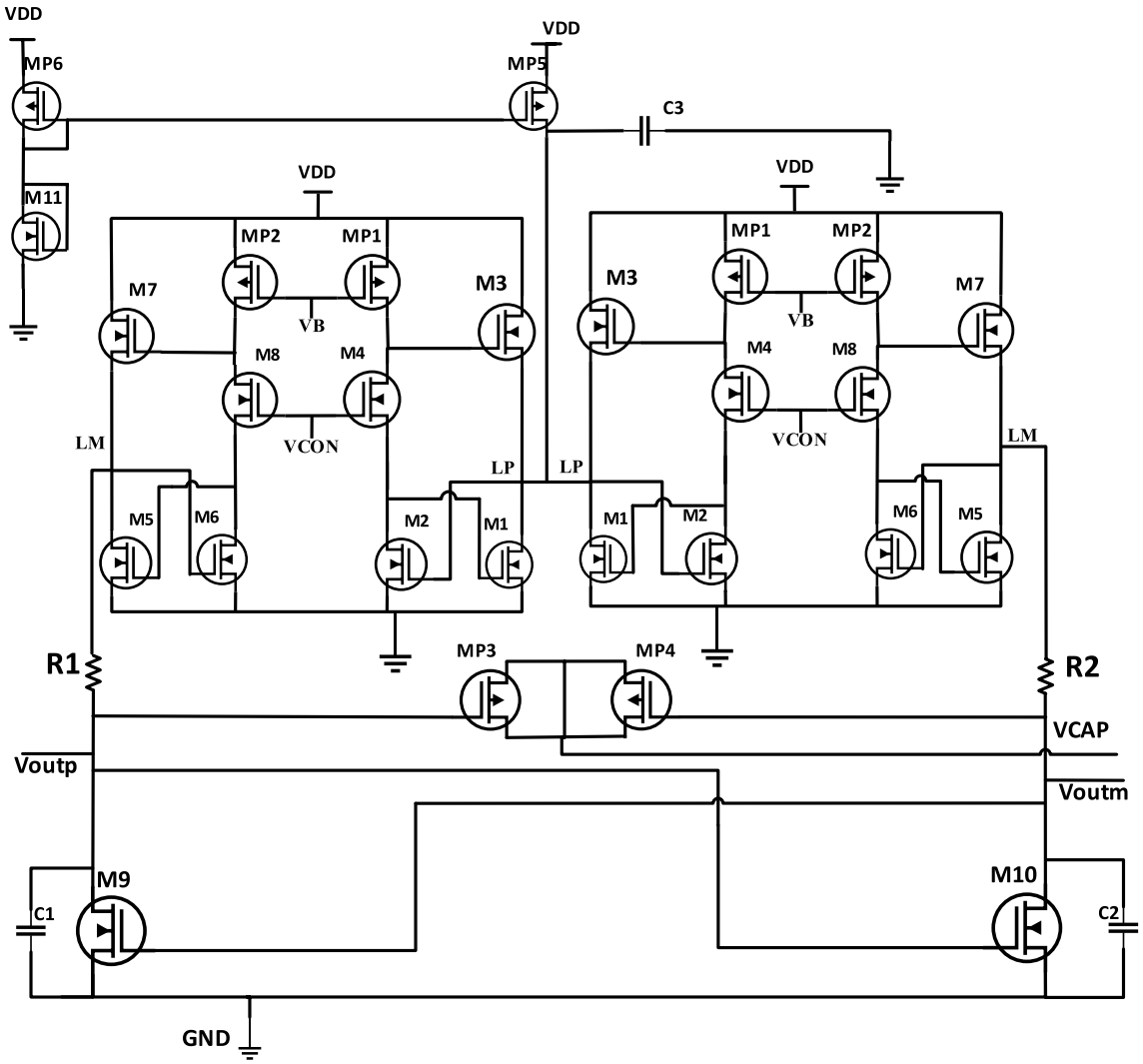


Fig. 6 Circuit diagram of the proposed VCO

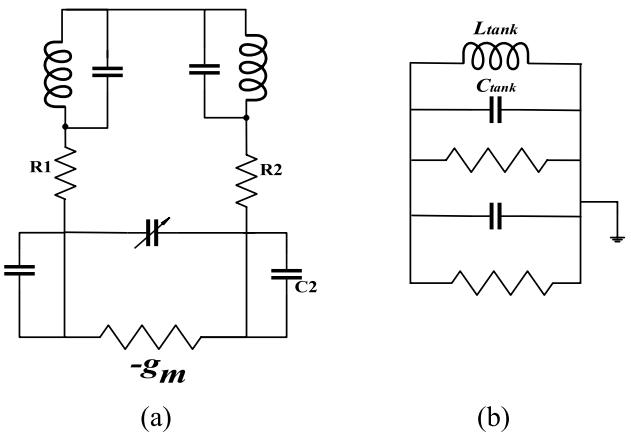


Fig. 7 Equivalent diagram of the proposed VCO

Figure 7a shows the equivalent R-L-C circuit of the proposed VCO. The equivalent half circuit of Fig. 7a with the negative resistance of the core is shown in Fig. 7b. The VCO resonant frequency can be presented as

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{tank}C_{tank}}} \tag{14}$$

where $L_{tank} = 2L_{se}\left(1 + {}^{1}\!/\!_{Q_{eff}^2}\right)$ and $C_{tank} = (2C \parallel CC_1 \parallel C_{pl} \parallel C_{xcp})$. C_{xcp} is the equivalent capacitance due to the cross-coupled circuit as seen from the tank circuit. The quality factor of the LC tank is represented as

$$Q_{tank} = \frac{1}{2\pi f_{osc} L_{tank} g_{tank}} \tag{15}$$

Here, g_{tank} (conductance of the tank circuit) is the reciprocal of R_1 or R_2 as FAI has negligible parasitic resistance and I_{tail} is the current through the transistor MP5. The coarse tuning of the oscillation frequency is obtained by varying the value of the control voltages VB and VCON of the FAI, whereas fine-tuning of the oscillation frequency is achieved by capacitance variation of AMOS varactors through VCAP voltage variation. The calculated values of the resistances and capacitances of the proposed VCO are $R_1 = R_2 = 16\ \Omega$, $C_1 = C_2 = 250$ fF, and $C_3 = 32$ fF.

Table 1 presents the calculated width of all transistors keeping the minimum length of the transistors at 0.18 µm. The phase noise in an LC VCO arises normally due to the tank circuit. In this case, the incorporation of the FAI in VCO added extra phase noise to the circuit. So, the total phase noise can be presented as

$$L(\Delta\omega) = 10\log\left(\frac{2kT}{Pcarrier}\cdot\frac{\omega_{osc}}{2Q_{tot}\Delta\omega}\right) + 10\log\left[\frac{(i_n^2/\Delta f)\Gamma_{rms}^2}{2q_{max}^2\Delta\omega^2}\right] \quad (16)$$

The first term in (16) is due to the tank circuit, which is based on the well-known Leeson's Formula. The second term is contributed by the FAI where Γ_{rms}^2 is the impulse sensitivity function of the VCO and $(i_n^2/\Delta f)$ is the sum of the current noises of the active parts of the FAI. It can be noted that the incorporation of FAI in VCO results in area reduction and reduction of the up-converted 1/f noise of the cross-coupled structure, due to the highly symmetric nature of FAI. The 1/f noise can be further reduced by switching the transistors between inversion and accumulator regions at regular intervals of time [30].

Post Layout Simulation Results and Discussion

The proposed FAI and VCO are simulated in spectre-RF simulator of Cadence (IC6.1.6) software, using UMC 0.18 µm mixed-mode CMOS technology. The corresponding layout, as shown in Fig. 8, consumes an area of $58.6 \times 64.6\ \mu m^2$, with each of the FAIs occupying an area of $17.1 \times 18\ \mu m^2$. The XCP in the layout represents the cross-coupled transistor pair.

Table 1 Size of transistors in the proposed FAI

Transistor	Width (µm)	Transistor	Width (µm)
M1, M5	7	M9	21
M2, M6	10		21
M3, M7	7	M11	16
M4, M8	6	MP3, MP4	35
MP1, MP2	5	MP5, MP6	32

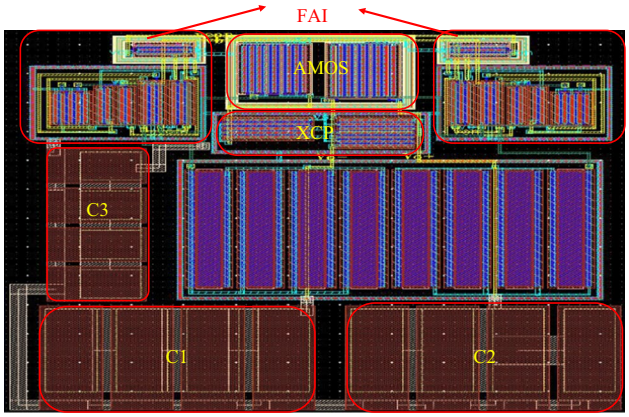


Fig. 8 Layout of proposed VCO

For all nMOS transistors, the substrates are connected to the ground and for all pMOS transistors, the substrates are connected to the supply. Metal–Insulator-Metal capacitors (MIM-CAP) are used in the VCO design to avoid the mutual inductance between the plates. As poly resistors contribute less noise as compared to other on-chip resistors, they are also used in this design.

Figure 9 indicates that the simulated inductance value of FAI ranges from 12.5 nH to 256.2 nH and the self-resonance frequency from 3 GHz to 7.18 GHz. These values correspond to a range of control voltage VB from 1.2 V to 1.45 V and VCON from 760 mV to 1 V. The straight-line portion of the curves indicates that the AI is completely stable, frequency-independent with a constant inductance value, and after that, it is marginally stable and frequency-dependent up to the resonant frequency. After the resonating frequency, the structure does not behave as an inductor rather it shows a capacitive behavior.

Figure 10 shows the maximum Q value of FAI as 3290. The maximum Q values at 1.9 GHz and 2.4 GHz are nearly 1900. The above values are obtained by biasing the two control voltages VB = 1.2 V and VCON = 905 mV for 1.9 GHz and VB = 1.2 V and VCON = 847 mV for 2.4 GHz. The Q-values at a particular frequency can be varied by changing

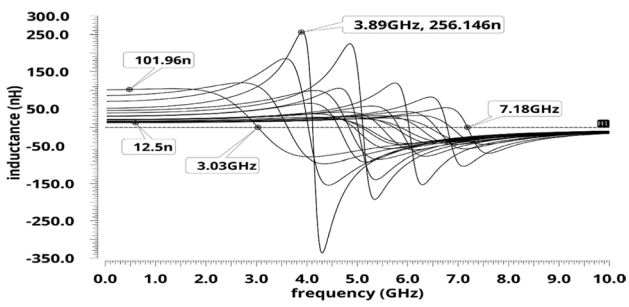


Fig. 9 Plot of inductance and self-resonant frequency of the FAI

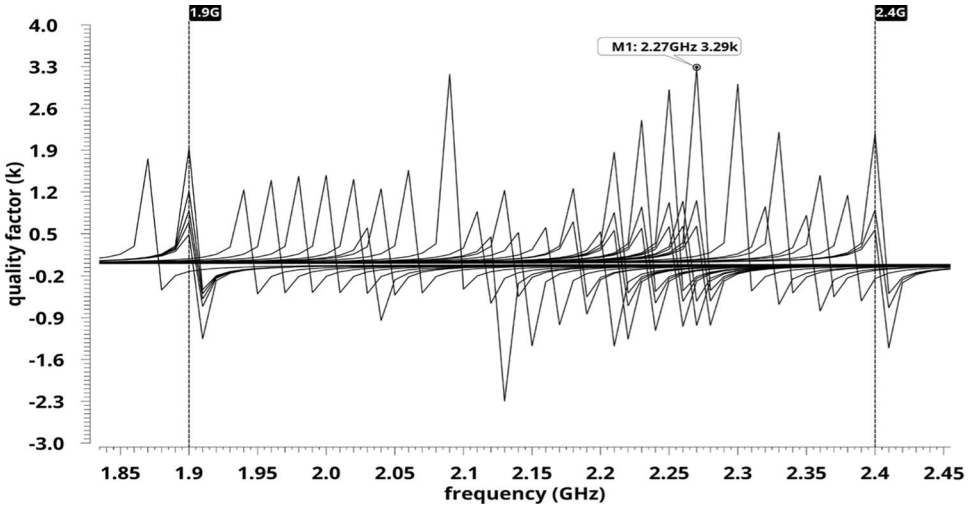


Fig. 10 Plot of Q vs frequency of the FAI

Table 2 Characteristics of the proposed FAI

Parameters	Q	L (nH)	VCON (V)	VB (V)
1.9 GHz	427	24.2	0.905	1.45
2.4 GHz	742	19.4	0.847	1.45

the current through the FAI. Table 2 summarizes the simulated inference of the proposed FAI.

The coarse tuning of the frequency of oscillation of VCO is shown in Fig. 11a. The tuning range for which the frequency varies linearly is found to be 235 MHz to 2.83 GHz corresponding to VCON value 830 mV to 1.08 V. It is observed that the frequency of oscillation reduces as VCON increases. Figure 11b shows the fine-tuning curves for the frequency of the two popular bands of 1.9 GHz and 2.4 GHz. It is noticed that the frequency of oscillation increases in proportion to voltage VCAP in the range of 1.09 V to 1.3 V beyond which the curve is non-linear. The VCO gain (KVCO) is found to be 646 MHz/V concerning the voltage VCAP.

The noise characteristics curve of FAI is shown in Fig. 12. The input-referred noise of the FAI is found to be 7.9 nV/Hz at 2.4 GHz frequency and the noise corner frequency is less than 200 Hz. The best phase noise of the proposed VCO varies from −85.3 dBc/Hz to −102.4 dBc/Hz at 1 MHz offset frequency (Fig. 13) for a center frequency range of 1.7G to 2.6 GHz. The phase noise is found to be −93.7 dBc/Hz and −92.4 dBc/Hz at center frequencies of 1.9 GHz and 2.4 GHz respectively.

Figure 14a shows the effect of process and temperature variation on the frequency of oscillation. It is observed that for the FNSP and SNFP process corners, the frequency difference is more than 40%. Figure 14b shows the phase noise plot with the process and temperature variation at 1 MHz offset frequency for a center frequency

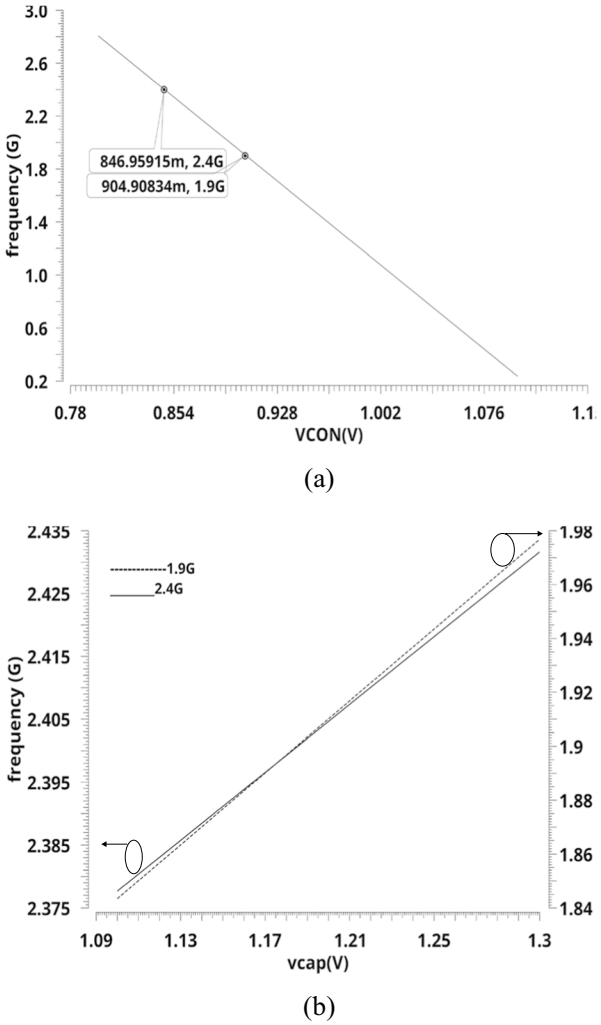


Fig. 11 **a** Coarse and **b** fine-tuning curve for frequency of oscillation

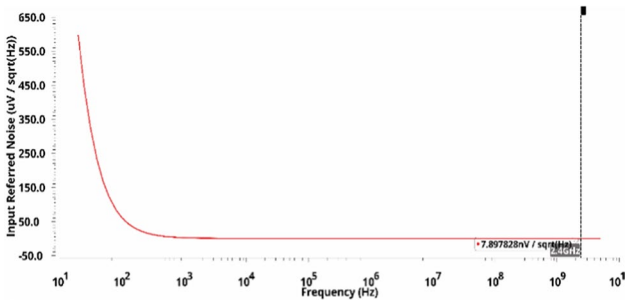


Fig. 12 Input referred noise plot of the FAI

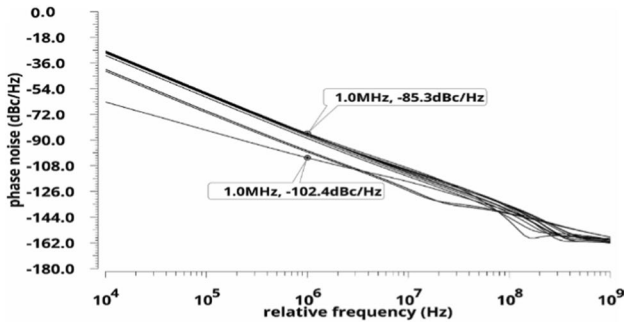


Fig. 13 Phase noise of the VCO at different frequencies of oscillation

of 2.4 GHz. The difference between the extreme corners FNSP and SNFP is around 8 dBc/Hz with 5.1% variation throughout the temperature range of −40 °C to 125 °C. Due to both process tolerance and component mismatch, there is quite a high difference in the frequency result. Hence, the Monte-Carlo simulation is further performed for the stability issue.

Figure 15a and b show the Monte-Carlo simulation results for the two frequency bands 1.9 GHz and 2.4 GHz. The simulation is performed by taking 1000 samples with σ = 3 and taking VCON as the global parameter of values 905 mV and 847 mV respectively. The mean frequencies are found to be 2.02 GHz and 2.41 GHz with the Gaussian distribution for the band 1.9 GHz and 2.4 GHz respectively.

The total power consumed by the VCO for different values of the control voltages VB and VCON is shown in Fig. 16. The minimum power consumed for VB = 1.2 V, VCON = 1 V, which is 6.28 mW, and the maximum power consumed for VB = 1.45 V, VCON = 760 mV, which is 8.62 mW. Table 3 presents the comparison of the proposed work with related works.

The proposed VCO requires an area of 0.0038 mm.^{2} in 0.18 µm technology without the I/O pads. It has the lowest gain of 646 MHz/V and has a phase noise of -102.4 dBc/Hz

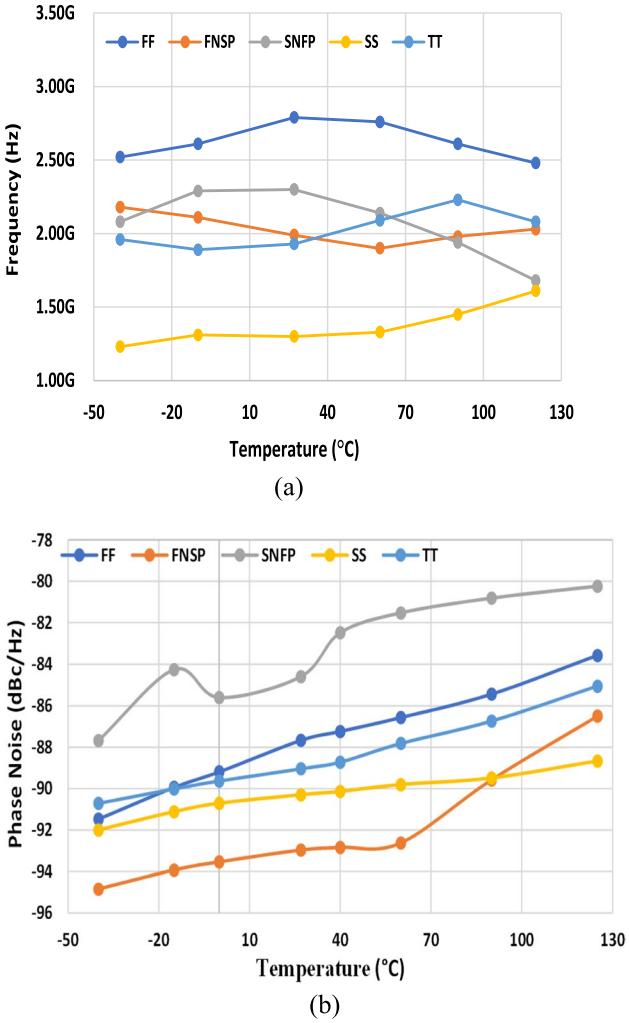


Fig. 14 **a** Frequency vs. temperature and process variation at a center frequency of 1.9 GHz and **b** phase noise plot for temperature and process variation

for a center frequency of 2.47 GHz at an offset frequency of 1 MHz. The Figure of merit (FoM) of the VCO can be calculated by [3]

$$FoM = L\{\Delta f\} + 10log\left(P_{DC}(mW)\right) - 20log\left(f_{osc}/f_{offset}\right) \quad (17)$$

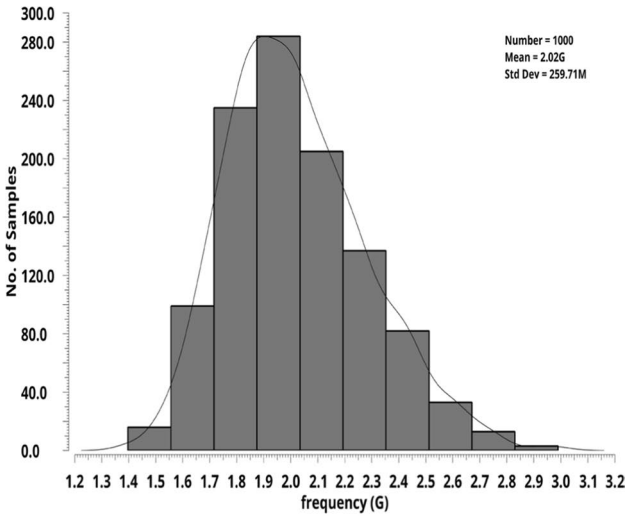
where L is the phase noise, P_{DC} is the power consumption, f_{osc} is the frequency of oscillation, and f_{offset} is the offset frequency at which the phase noise is measured. Using (17) the FOM is calculated to be −160.64.

It may be noted that in comparison to other designs reported in Table 3, the proposed design has better phase noise and VCO gain performance. Considering the overall performance of all designs from FOM it is found that our proposed VCO is more promising as compared to others.

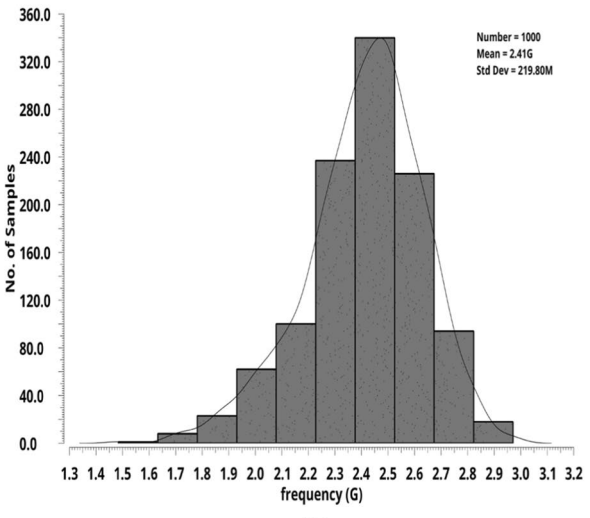
Table 3 Comparison and performance summary

Parameter	[20]*	[3]*	[12]*	[13]*	[21]*	[22]**	This work*
Tech. (nm)	90	130	180	180	180	180	180
Power (mW)	1.83–3.84	3.6–4.3	28	7	29.1	13.8	6.3–8.62
Frequency range (GHz)	1.93–6.22	1.22–2.6	1.325–2.15	0.1–2	3.8–7.4	0.5–2	0.23–2.83
Phase noise (dBc/Hz)	−81.32 to −76.89	−82 to −87	−86	−80 to −90	−92.5	−78 to −90	−85.3 to −102.4
KVCO (MHz/V)	–	–	2350	2171	2400	–	646
FoM	−144.4 to −149.3	−138.22 to −149.79	−133.97 to −138.17	−111.55 to −147.57	−149.46 to −154.75	−120.58 to −144.63	−124.53 to −160.5
Area (mm^2)	–	0.0031	–	–	0.09	0.09	0.0038

*Simulation result, **Measured result



(a)



(b)

Fig. 15 Monte-Carlo simulation for frequency of oscillation for **a** 1.9 GHz and **b** 2.4 GHz

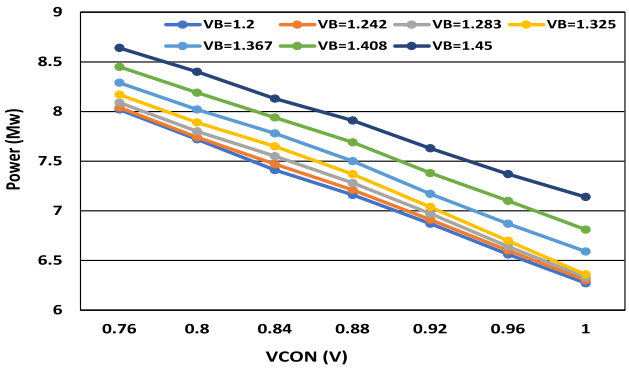


Fig. 16 Total power variation concerning the control voltages

Conclusions

A low-power wideband cross-coupled LC VCO is designed with the proposed high-Q FAI. The maximum power consumed by the VCO is 8.6 mW with a reasonable phase noise of −92.4 dBc/Hz for 1.9 GHz and −93.7 dBc/Hz for 2.4 GHz at an offset frequency of 1 MHz. The proposed VCO has a tuning range of 235 MHz to 2.83 GHz, that covers the whole L-band and lower C-band. It can be used in DECT, advanced wireless services (AWS-2), fixed microwave services, Bluetooth™, Wi-Fi, and unlicensed part 15 devices. This research work is part of a frequency synthesizer using a phase lock loop (PLL) of a transceiver architecture. After completion of the entire design, we will go for real-world implementation after due fabrication and subsequent testing.

Author contribution All authors contributed equally to the study conception and design. All authors read and approved the final manuscript.

Funding No funds, grants, or other support was received.

Declarations

Conflict of interest The authors have no conflict of interest to declare that are relevant to the content of this article.

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