



Modifications in CMOS Dynamic Logic Style: A Review Paper

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Abstract Dynamic logic style is used in high performance circuit design because of its fast speed and less transistors requirement as compared to CMOS logic style. But it is not widely accepted for all types of circuit implementations due to its less noise tolerance and charge sharing problems. A small noise at the input of the dynamic logic can change the desired output. Domino logic uses one static CMOS inverter at the output of dynamic node which is more noise immune and consuming very less power as compared to other proposed circuit. In this paper, an overview and classification of these techniques are first presented and then compared according to their performance.

Keywords Dynamic logic · Domino logic · Delay · Noise tolerance · Power consumption · Robustness · Technology scaling

Introduction

The rapid advancement of VLSI circuit is due to the increased use of portable and wireless systems with low power budgets and microprocessors with higher speed. To achieve this, the size of transistors and supply voltages are scaled with technology. Due to larger number of devices per chip the interconnection density increases. The interconnection density along with high clock frequency increases capacitive coupling of the circuit. Therefore, noise pulses known as cross-talk can be generated leading

to logic failure and delay of the circuit [1]. Again, when supply voltage is scaled, the threshold voltage of the device requires to be scaled to preserve the circuit performance, which leads to increase in the leakage current of the device.

Due to high speed and low device count, especially compared to complementary CMOS, dynamic-logic circuits are used in a wide variety of applications including microprocessors, digital signal processors and dynamic memory [2]. Dynamic circuit contains a pull-down network (PDN), which realizes the desired logic functions. According to the basic theory, the dynamic logic circuit will precharge at every clock cycle. As the clock signal frequency is high, the circuit is introduced with a lot of noise which consume extra power and slows the circuit.

Problem Statement

Figure 1 is an example of footless domino gate. During the precharge phase when the clock is LOW, the pre-charging PMOS gets ON and the dynamic node is connected to the VDD and gets pre-charged to VDD. When clock goes high, the evaluation phase starts and the output gets evaluated with the pull-down network and conditionally gets discharged if any one of the input is at logic 1. At the evaluation period when all the inputs are at logic 0, the dynamic node should be at logic 1. But the wide fan-in NMOS pull-down leaks the charge stored in the capacitance at the dynamic node due to the subthreshold leakage. This is again compensated by the PMOS keeper, which aims to restore the voltage of the dynamic node. When a noise voltage impulse occurs at the gate input, the keeper may not be able to restore the voltage level of the dynamic node. The subthreshold leakage current is exponentially dependent upon V_{GS} . So in the presence of noise impulse

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the gate voltage increases, which leads to increase in V_{GS} and the dynamic node gets wrongly discharged.

As noise of domino gates is now more important than the area, energy dissipation and delay issues, recently several techniques have been proposed [3, 4] to reduce the noise of dynamic circuits. All the techniques have reduced the noise sensitivity, but there are many drawbacks with area, power dissipation and delay.

Dynamic Logic Techniques

Digital integrated circuit noise has become one of the foremost issues in the design of very deep submicron VLSI chips [1, 2]. In the past two decades, a number of circuit techniques have been developed with a view to improve the noise immunity of dynamic CMOS logic gates. While it is impractical to include every technique in the literature, in this section, an overview of some significant techniques has been presented and classified into four main categories based on the principle of their operations.

- (i) Employing keeper
- (ii) Precharging internal nodes
- (iii) Raising source voltage
- (iv) Constructing complementary p-network

Employing Keeper

Perhaps the simplest way to enhance the noise tolerance of dynamic CMOS logic gates is to employ a weak transistor, known as keeper, at the dynamic node as shown in Fig. 2. The keeper transistor provides a strong '1' to the dynamic node so that the stored charge of the dynamic node is maintained. In the original dynamic logic network [5], the gate of the PMOS keeper is tied to the ground, as shown in Fig. 3a. Therefore, the keeper is always on. Later, feedback keepers, illustrated in Fig. 3b, became more widely used because they eliminate the potential dc power consumption problem using the always-on keeper in the evaluation phase of domino gates [6].

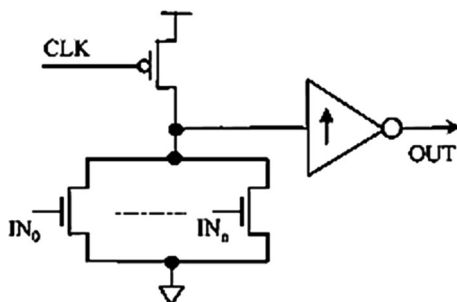


Fig. 1 A typical footless Domino OR gate

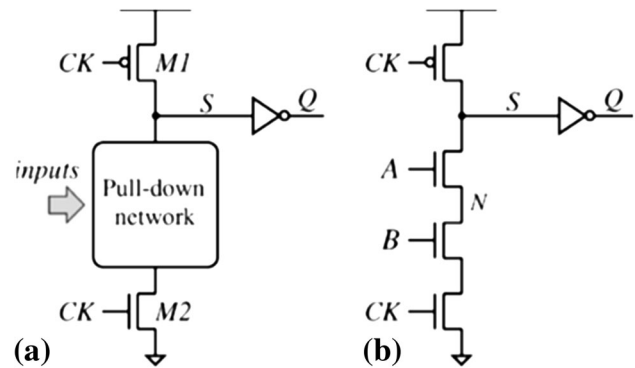


Fig. 2 A domino logic gate **a** circuit schematic, **b** two-input AND gate

The use of keeper causes contention when the pull-down network is ON during the evaluation phase, resulting in slower overall gate performance. In wide fan-in gates designed using very deep submicron process technology; the large leakage current through the n-network necessitates a very strong keeper to retain the voltage at the dynamic node. To reduce the serious contention problem associated with the strong keeper, new keeper design techniques have been proposed by Anis et al. [3, 7] (Fig. 3c) and Alvandpour et al. [4, 8] (Fig. 3d). Both techniques share the same basic principle, that is, to temporarily disable the keeper during the small time window when the dynamic gate switches. These two techniques have been shown to be very effective in enhancing the noise tolerance of dynamic gates against gate internal noises like leakage noise. However, dynamic gates with those keepers are still susceptible to external noise glitches because the dynamic node is not adequately protected during the gate switching time window.

To reduce the internal and external noise Ding and Mazumder [9] (Fig. 4a, b) designed a noise-tolerant design technique using circuitry exhibiting a negative differential resistance effect. A weak CMOS inverter is employed to generate the feedback signal instead of directly connecting gate output Q to the gate node of transistor M_0 ; by which the response time of the feedback process is independent of external gate load. This independently optimizes the feedback inverter without having to worry about the gate output.

Precharging Internal Nodes

In complex dynamic logic gates with large pull-down network, charge sharing between the dynamic node and the internal nodes in the pull-down network often results in false gate switching. A simple yet effective way to prevent the charge sharing problem is to precharge the internal nodes in the pull-down network along with precharging the

Fig. 3 Improving noise immunity of dynamic logic gates using keeper
 a weak always-on keeper [5],
 b feedback keeper [6],
 c HS feedback keeper [7],
 d conditional feedback keeper [4]

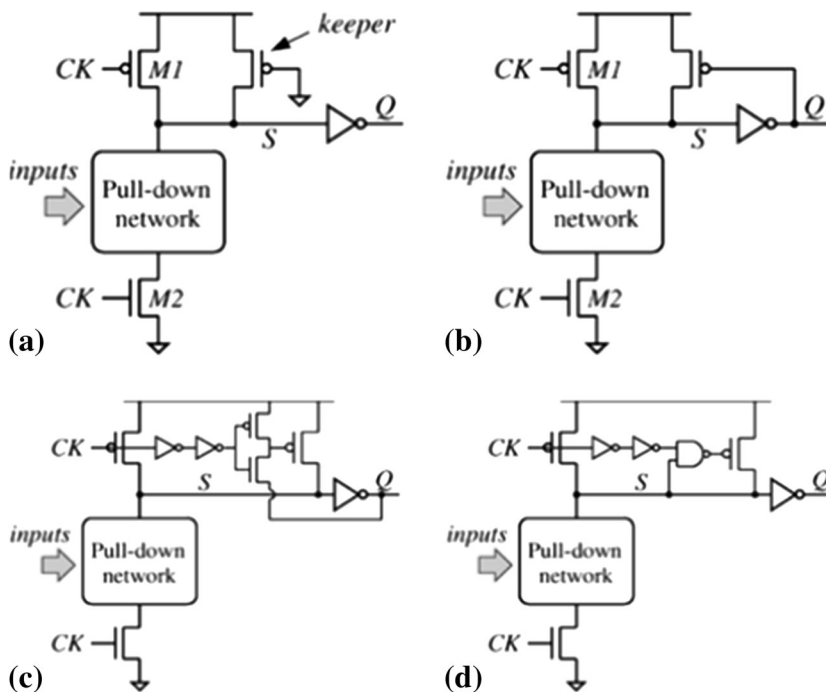
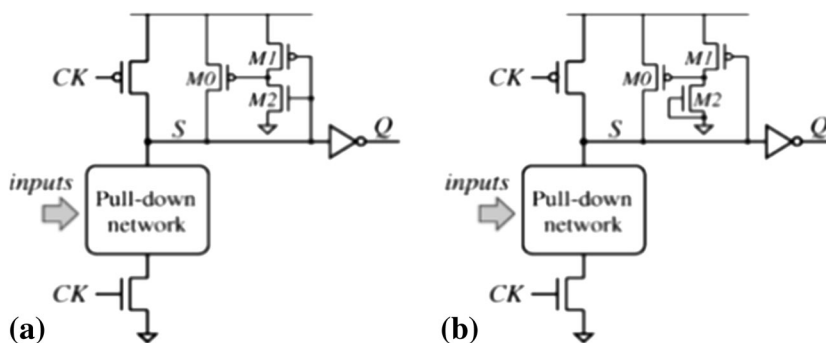


Fig. 4 Domino logic gate with optimized feedback keeper
 a CMOS inverter feedback,
 b pseudo-PMOS inverter feedback



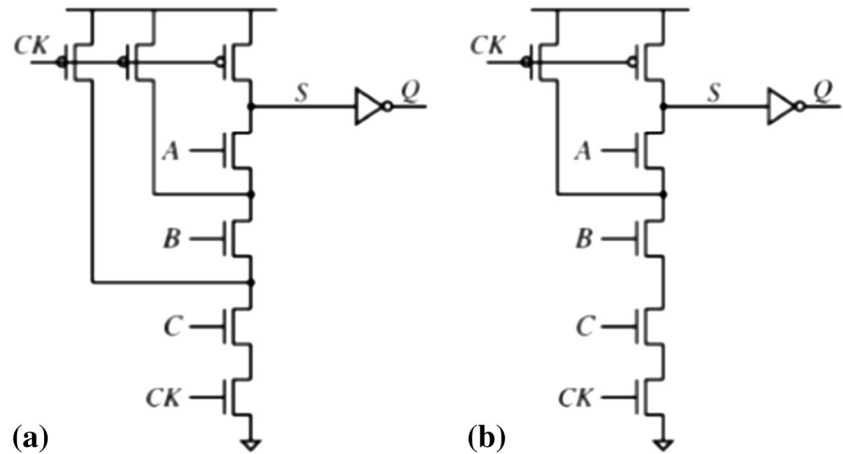
dynamic node S [10, 11]. An example dynamic 3-input AND gate using this technique is illustrated in Fig. 5a. When all internal nodes are precharged, this technique is able to eliminate the charge sharing problem at the cost of using a large number of precharge transistors and the increased load capacitance on the clock net. Partial precharge, as shown in Fig. 5b, has also been used in design practice as a trade-off between noise immunity and overheads in chip area and in clock load. NMOS transistors can also be used to precharge the internal nodes if the cost of an inverter to generate the complementary clock signal can be justified. Since the internal nodes are only precharged to, dynamic logic gates using NMOS precharge transistors have reduced discharging time and decreased dynamic power consumption. Finally, it is noted that techniques based on precharging internal nodes alone are not very effective against external noises.

Raising Source Voltage

One effective way to improve noise tolerance against both internal and external noises is to increase the source voltage of the transistors in the pull-down network. Since the gate voltage has to be greater than the sum of the source voltage and the transistor threshold voltage when a transistor is turned on, higher source voltage directly leads to increased gate turn-on voltage. Furthermore, due to the body effect, transistor threshold voltage is increased when the source voltage rises. This also contributes improving gate turn-on voltage.

The PMOS pull-up technique [12], shown in Fig. 6a, employs a PMOS transistor at node N_2 forming a resistive voltage divider with the bottom clock controlled transistor. The voltage at node N_2 , which determines the switching threshold voltage of the dynamic logic gate, can be

Fig. 5 Precharging internal nodes (3-input AND gate) **a** precharge all internal nodes [10], **b** partial precharge [11]



adjusted by changing the relative size of the PMOS pull-up transistor. One major drawback of this technique is the dc power consumption in the resistive voltage divider. Furthermore, since the voltage level at the dynamic node S can never get lower than the voltage at node N_2 , the voltage swing at node S is not rail-to-rail. When the size of the PMOS pull-up transistor is large in an effort to aggressively raise gate noise immunity, the gate output may also not have a rail-to-rail swing.

An improved method, shown in Fig. 6b, employs a pull-up transistor with feedback control [13]. Here an NMOS transistor M_1 is used to pull up the voltage of an internal node. The gate of the pull-up transistor is connected to the dynamic node of the domino gate. This design allows the pull-up transistor to be shut off when the voltage of the dynamic node goes low; therefore, the dynamic node S undergoes rail-to-rail voltage swing. Also, the dc power consumption problem is partially solved. It occurs only under certain input combinations that do not turn on the pull-down network. Note that a PMOS transistor can similarly be used in this technique provided that the gate of the PMOS transistor is connected to the output of the dynamic logic gate.

The mirror technique [14, 15] employs a feedback controlled NMOS transistor similar to the NMOS pull-up technique. In addition, it duplicates the pull-down network in an effort to further reduce dc power consumption and to further improve gate noise tolerance. A 2-input dynamic AND gate designed using the mirror technique is shown in Fig. 6c. Whenever the pull-down network is OFF, the mirror network is also OFF, hence, cutting off the potential dc conducting path from the NMOS pull-up transistor through the bottom clock controlled transistor. Therefore, the dc power consumption problem is completely solved. However, this technique significantly lengthens the discharge path in the pull-down network, which potentially leads to slower circuit or considerably increased circuit active area when the transistors are aggressively sized.

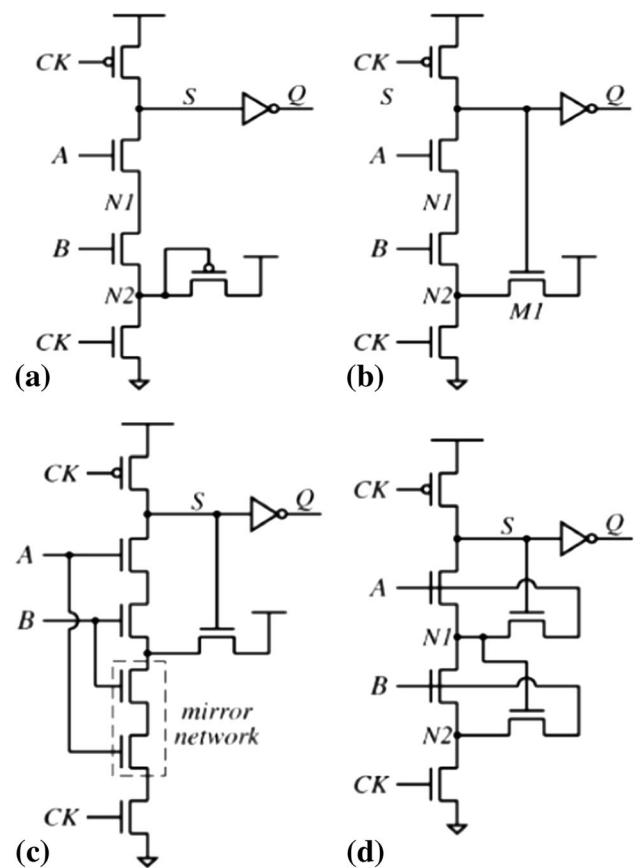


Fig. 6 Raising source voltage (2-input AND gate) **a** pMOS pull-up technique [12], **b** NMOS pull-up (with feedback) [13], **c** mirror technique [14], **d** twin transistor technique [16]

The twin transistor technique [16, 17] adopts NMOS pull-up transistors at all internal nodes to further improve dynamic gate noise immunity. In addition, the drain nodes of the pull-up NMOS transistors are connected to the inputs instead of to the power-supply network, as illustrated in Fig. 6d. By doing so, unnecessary injection of current by

Fig. 7 Possible short circuit problem using twin transistor technique **a** A 3-input OR-AND gate, **b** direct conducting path

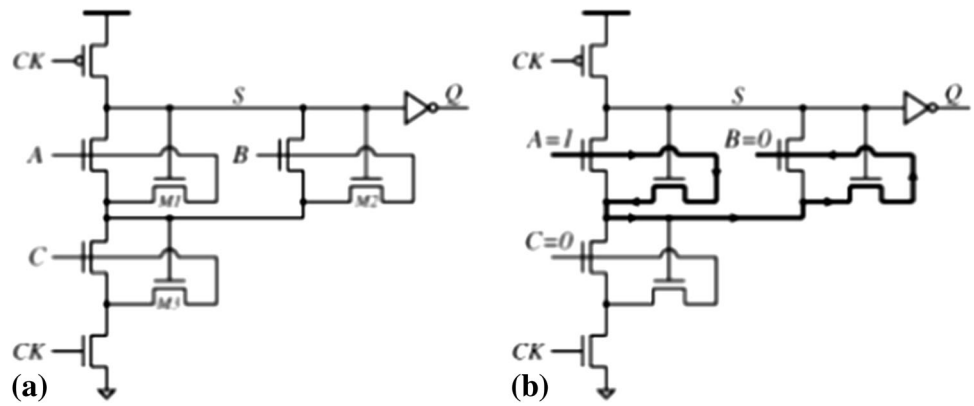
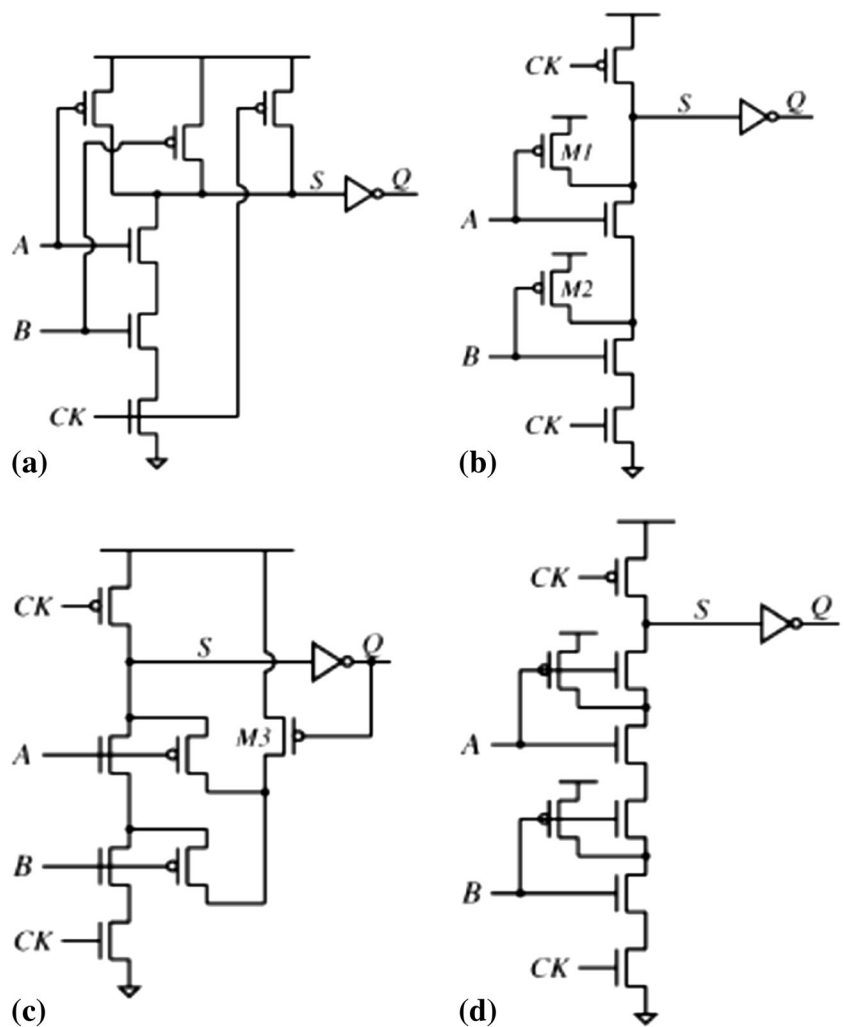


Fig. 8 Constructing complementary PFET network (2-input AND gate) **a** complementary p network technique [18], **b** CMOS inverter technique [20], **c** gated CMOS inverter technique [21], **d** triple transistor technique [22]



the pull-up transistors is avoided, resulting in lower gate power consumption. However, this technique leads to increased gate input capacitance which may slow down the switching of the gates in the previous stage. Further, this technique is not suitable for certain logic functions because it may short input nodes. As an example, in Fig. 7a, a 3-input OR-AND gate implementing the logic function of

$(A + B)C$ is shown. Assume input A is high while inputs B and C are low. The dynamic node S stays high because C is low and there is no discharging path to the ground. Under such scenario, there is a dc conducting path between the two inputs A and B, as illustrated in Fig. 7b. Therefore, the logic states at node A or node B are unclear. Note that the resulting damage can go far beyond the single dynamic

Fig. 9 Possible short circuit problem using CMOS inverter technique **a** A 3-input OR-AND gate, **b** direct conducting path

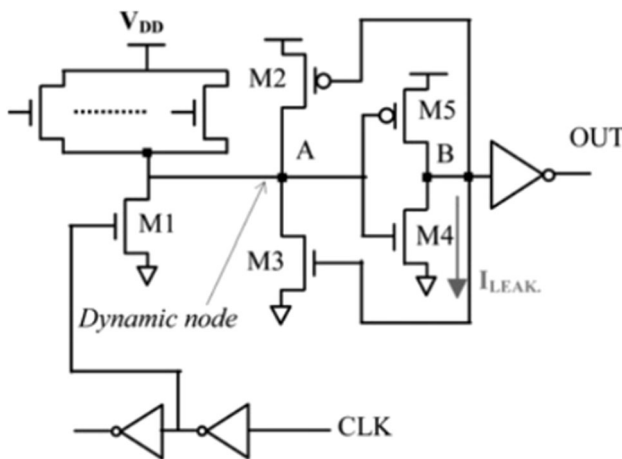
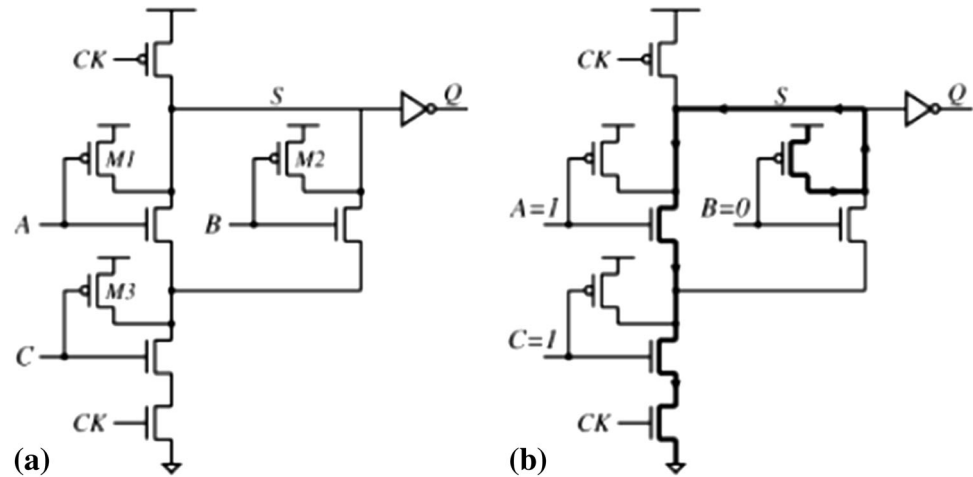


Fig. 10 SFEG dynamic logic circuit design [23, 24]

gate under study if these ambiguous nodes feed to a large number of other gates.

Constructing Complementary p-Network

The basic principle of this class of techniques is to construct a weak complementary p-network to prevent the dynamic node from floating in the evaluation phase. One such technique [18, 19] is illustrated in Fig. 8a. The gate operates in a similar way as a normal domino gate in the precharge phase. In the evaluation phase, the logic gate behaves as a skewed CMOS logic gate. Therefore, the switching threshold voltage of the dynamic logic gate is equivalent to that of a skewed CMOS logic gate. In addition to the silicon area overhead associated with the pull-up network, a major drawback of this technique in practice is its ineffectiveness in dealing with very wide logic gates, for example, wide OR gates, where dynamic logic styles really outshine static CMOS logic gates in performance.

PMOS transistors can also be employed at a per transistor level, as shown in Fig. 8b. This technique is known

as CMOS inverter technique [20]. The relative size of the PMOS transistors can be varied to adjust the switching threshold of the dynamic logic gate. One advantage of this technique is that it can be selectively applied to a subset of inputs if they can be identified as noisy in advance. The main drawback of this technique is that it is not suitable for OR type logic gates because of possible serious dc currents under certain input combinations. Again the simple 3-input OR-AND gate is used as an example. When inputs A and C are high and input B is low, there is a direct conducting path between the power-supply network and the ground node, as shown in Fig. 9b. More hazardous than the obvious problem of dc power consumption, the voltage at node S is determined by the relative strength of the pull-up transistor M_2 and that of the transistors in the discharge path. The gate may fail to switch when the pull-up transistor is sized relatively strong in an effort to aggressively improve gate noise tolerance.

The dynamic node can be false reset with certain input combinations using either of the two above techniques. In Fig. 8b, for example, if input A stays high and input B falls from high to low during the evaluation phase, the dynamic node may be reset to high by the pull-up PMOS transistor M_2 . With a view to solve this false reset problem, Evans in [21] used an additional transistor M_3 , shown in Fig. 8c. M_3 is ON when the gate output remains low. When the evaluation is executed and the output rises, M_3 is turned off disconnecting the pull-up transistors from the power-supply network. Similar tactic can also be applied to improve the simple complementary p-network technique. It is noted that this gated CMOS inverter technique does not completely solve the dc conducting problem for certain logic circuits.

Figure 8d illustrates a noise-tolerant 2-input AND gate using a triple transistor technique [22], where each NMOS transistor in the pull-down network of a simple dynamic logic gate is replaced by three transistors. The technique

Fig. 11 Two-input dynamic AND-gate implemented with proposed noise-tolerant dynamic circuit technique [25] **a** gate can be domino [static output inverter (OI)] or TSPC (NC2MOS output inverter), **b** timing diagram

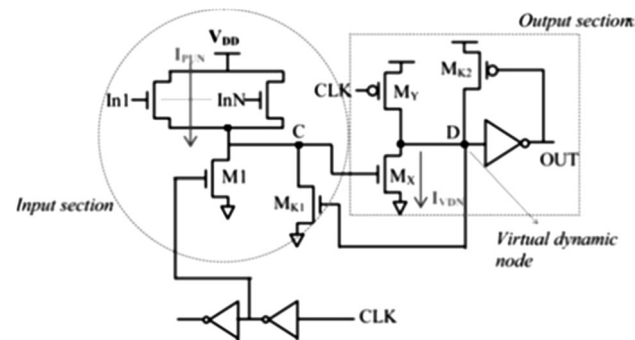
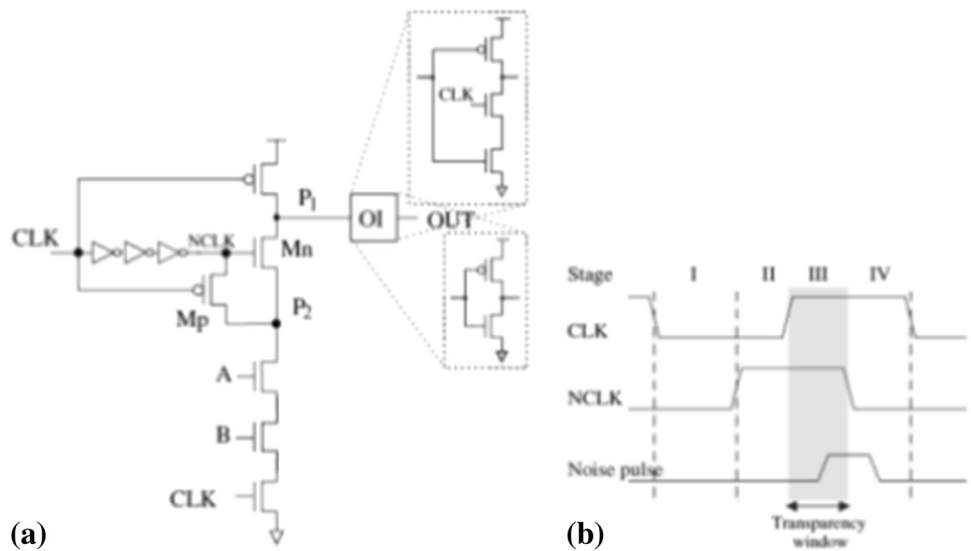


Fig. 12 Proposed dynamic logic circuit design [29]

can be considered as a variation of the CMOS inverter technique where an additional NMOS transistor is used to prevent the possible dc conducting path problem in the evaluation phase. Similar to the mirror technique, this technique significantly lengthens discharge paths in the pull-down network. While it can be useful for certain logic gates like wide-OR gates, it is not practical to be applied to general pull-down NMOS network because of its overhead in circuit area and performance.

Other Modifications

SFEG Technique

The so-called source following the evaluation gate (SFEG) technique, independently demonstrated in [23, 24], is depicted in Fig. 10. The noise immunity of the gate is increased by implementing the logic function by means of an NMOS pull-up network. The leakage currents flowing through the evaluation network aim to charge the dynamic node (the node A). This event reduces the V_{GS} of the NMOS transistors and, as a consequence, the leakage currents are

exponentially decreased. Furthermore, in the SFEG scheme, the critical node driving the final static inverter (comprising of transistors M_n and M_p) does not coincide with the dynamic node and, thus, the critical node leakage current (I_{LEAK}) is only because of the NMOS (M_4). The drawback of such a technique is that the NMOS pull-up network is able to charge the dynamic node only up to $V_{DD}-V_{TH}$ during an actual switching of the gate. The threshold voltage drop is compensated by the pull-up PMOS transistor M_2 . However, the transistor M_2 is not immediately turned on because of the finite delay of the feedback loop that drives M_2 itself. For this reason, the short-circuit current, flowing through the path M_4 – M_5 during the gate switching, causes an increased dynamic energy dissipation.

Mendoza’s Domino Logic

To increase the noise immunity of domino logic Mendoza in [25] depicted in Fig. 11, inserted an NMOS transistor M_n between the precharge node P_1 and the PDN. A delay stage, which can be constructed with three cascaded static inverters, was used to locally generate the NCLK signal from the clock CLK, and a PMOS transistor M_p is added between the node NCLK and the node P_2 . The inputs have not been used to precharge any internal node in the PDN. This is advantageous because the capacitive loads at the inputs remain the same. However, the drawback exists with area and propagation delay. Due to the presence of the inverters M_n and M_p the propagation delay is more making the circuit slower.

Modified SFEG

To increase noise tolerance modified SFEG was proposed by Frustaci in [26] depicted in Fig. 12. This scheme is

Table 1 Comparison of existing dynamic circuit noise tolerance enhancing techniques

Class	Technique	References	Illustration	Number of Transistor	I/P Load	Clock Load	Discharge Path	dc Current	All Noises	All Logic
1	Always ON Keeper	[5]	Fig. 3a	N	0	0	0	X	0	0
	Feedback Keeper	[6]	Fig. 3b	N	0	0	0	0	0	0
	HS Feedback Keeper	[7]	Fig. 3c	N	0	0	0	0	X	0
	Conditional Feedback Keeper	[4]	Fig. 3d	N	0	0	0	0	X	0
	Inverter Keeper	[9]	Fig. 4a, b	N	0	0	0	0	0	0
2	Precharge Internal Node	[10]	Fig. 5a	2N	0	X	0	0	X	0
	Partial Precharge	[11]	Fig. 5b	N	0	X	0	0	X	0
3	PMOS Pull-up	[12]	Fig. 6a	N	0	0	0	X	0	0
	NMOS Pull-up	[13]	Fig. 6b	N	0	0	0	X	0	0
	Mirror Technique	[14]	Fig. 6d	2N	X	0	X	0	0	0
4	Twin Transistor	[16]	Fig. 6c	2N	X	0	0	0	0	X
	Complementary P Network	[18]	Fig. 8a	2N	X	0	0	0	0	0
	CMOS Inverter	[20]	Fig. 8b	2N	X	0	0	0	0	X
	Gated CMOS Inverter	[21]	Fig. 8c	2N	X	0	0	0	0	X
	Triple	[22]	Fig. 8d	2N	X	0	0	0	0	0

Symbol '0' represents 'good', 'X' represents 'not-good' and 'N' is the number of transistors in the pull-down network of the original dynamic logic gate

significantly different from the SFEG technique in having high values of input noise tolerance that the previous designs could not reach, and it is suitable for an effective trade-off between noise robustness energy dissipation. This circuit is having NMOS-based pull-up evaluation network; which exploits the principle of dynamic logic style. Its delay-UNG performances show below average results.

Comparison of Techniques

In this section, the noise-tolerant design techniques are compared described in the previous sections. It begins with listing of set of basic requirements that a desirable noise-tolerant design technique should meet.

- (i) It improves gate noise tolerance against all types of noises.
- (ii) It is suitable for all logic functions.
- (iii) It has minimal circuit area overhead.
- (iv) It has minimal circuit speed overhead.
- (v) It consumes no dc power and has minimal ac power consumption overhead.

Dynamic circuit noise enhancing techniques discussed in this section are compared in Table 1. The first four columns are self-explanatory. The fifth column is the approximate number of transistors needed in a large dynamic logic gate, where N is the number of transistors in the pull-down network of the original dynamic logic gate. The sixth and seventh columns indicate whether the input

load capacitance and clock load capacitance are unchanged when a noise-tolerant design technique is used.

The eighth column shows whether the length of the discharge paths in the pull-down network is intact. The ninth column indicates whether the dynamic gate maintains the zero dc power consumption property. The tenth column shows whether the technique enhances noise tolerance against both internal and external noises. Finally, the last column shows whether the technique can be applied to all logic gates.

Conclusion

It is shown in Table 1, that the twin transistor technique and CMOS inverter based techniques are not suitable for all logic functions. Techniques based on precharging internal nodes as well as the two new feedback keeper techniques only improve gate noise immunity against certain types of noises. Both the PMOS pull-up technique and the NMOS pull-up (with feedback) technique consumes dc power. The Mirror technique and the triple transistor technique increase the length of gate discharge path. Techniques based on raising source voltage usually either have dc power consumption or require significantly larger silicon area. Techniques based on constructing complementary p-network often require larger silicon area and they increase the previous stage gate delay due to greater gate input capacitance. Summing up, simple feedback

keeper is the only general-purpose technique that improves dynamic logic gate noise immunity against all types of noise without significant increase in silicon area (device count), speed, and power consumption.

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