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Analysis and minimization of crosstalk noise in copper interconnects for high-speed VLSI circuits

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Abstract Due to the rapid advances of technologies, the scaling of parameters are decreasing. In VLSI (Very Large Scale Integration) technology, the feature size of integrated circuits (IC) has driving reduced in terms of power, speed, area and cost characteristics. The decreasing the sizes in sub-quarter microns, spacing between the components on-chip VLSI design and the signal switching time in terms of pico seconds or even less. As a result, the signal integrity (SI) issues are occurring at higher frequencies and high data rates. The evaluation of crosstalk noise between the coupled interconnect is one of the prominent issue in designing of high-speed ICs. In this paper, investigated the crosstalk noise of coupled copper (Cu) interconnect models with analytically at 32 nm technology nodes. Also, investigated the crosstalk reduction with shield insertion technique and increasing physical spacing between the coupled lines. For the low power VLSI applications, the shield insertion technique is preferable for reducing the crosstalk effects in coupled interconnects.

Keywords Crosstalk noise · High-speed integrated circuit · Interconnect · RLC interconnects · Shield insertion · Signal integrity

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1 Introduction

The rapid advances in technology has been resulted in miniaturized feature size to sub-microns and the signal switching time in pico-seconds or even less. As a result, the degradation of high-speed ICs performance due to its signal integrity (SI) effects. The SI effects such as, ringing, coupling effects, crosstalk noise, and signal delays and uncertainty noise [1–3]. In deep sub-micron technology, the crosstalk noise of an interconnect between coupled (aggressor and victim) lines has become a pre-eminent design issue. The aggressive technology scaling for local level interconnect has become additional capacitive and resistive. The global level interconnect has been became too inductive. The Capacitive and inductive coupling effects between the interconnect lines have become a significant design concern in global level interconnect models [3–5].

The characteristic impedance and crosstalk noise is the most effectively considered parameters on-chip VLSI digital design. As trends towards faster and smaller systems has drive increased crosstalk between the coupled interconnects. As an continuous increasing of clock frequencies in state-of-the-art digital ICs, the crosstalk effects between the coupled interconnects are significant SI problems. To achieve such high- speed and high data rates, the design of an accurate interconnect models are required. [6, 7].

At higher frequencies, an interconnects are not transparent. The behavior of an electrical properties of an interconnect models plays a key role in determining the performance of ICs [8]. The signal is established between two (or more) conductors when a signal generates along with an interconnect. When the spacing between coupled interconnects are decreasing (close proximity), the electromagnetic fields from the signal has fringe and interface

with adjacent interconnects. The transact of fields induces the coupling of energy and exchanges between the coupled Interconnect when an input signal is applied to Aggressor line [9].

Since, in high-speed ICs uses a signaling interfaces when a large numbers of interconnects are routed in parallel through packages, connectors, and PCBs [10]. Towards the future, the decreasing of size and increasing of data rates has been driven in increased crosstalk noise resulting in two primary impacts. First, crosstalk is affect the SI and timing by changing the signal propagation characteristics of the interconnects. Another one is, coupled crosstalk noise between the interconnect lines, which harms SI and reduces noise margins [11]. Crosstalk is induced by mutual coupling of inductance and capacitance between coupled interconnects. As a consequence of mutual coupling, energy exchanges between interconnects via the magnetic and electric fields (due to mutual Inductance, L_M and coupling capacitance C_M. C_M and L_M induces voltage noise and current from a driven line (Aggressor) onto a quiet line (victim) by means of electromagnetic field [11, 12].

The crosstalk noise on the victim line is proportion to the rate of change of the current on the aggressor line according to [11] as,

$$\Delta V_L = L_M \frac{\mathrm{di}}{\mathrm{d}t} \quad (1)$$

The current is induced on the victim line is proportion to the rate of change of voltage on the driven line: [9, 11, 12].

$$\Delta i_C = C_M \frac{\mathrm{dv}}{\mathrm{d}t} \quad (2)$$

In general, there are various types of analysis has been used for evaluating the characteristic impedance of Interconnect and crosstalk noise between coupled Interconnects of digital ICs. [13, 14]. An electromagnetic 2D field solver tool models the electromagnetic fields between coupled interconnects in a multi-conductor system. Filed solver gives an equivalent electrical RLC parameters of interconnect models. Reduction of crosstalk noise in interconnect has become significant for high-speed digital applications [15]. In this paper, investigated the analytical model of the coupled interconnects. Also evaluated the crosstalk noise reduction by using shield insertion and increasing the physical spacing between coupled interconnects.

Further, the rest of paper is organized as follows, the analytical model for coupled interconnects in 2. In Sect. 3, the crosstalk reduction of coupled interconnects with shield insertion and increasing physical spacing techniques.In Sect. 4, investigation of simulation results for design interconnect model with varying the interconnect lengths. In Sect. 5, conclusion of the paper.

2 Analytical model of coupled Cu interconnect

The coupled Interconnect model in cross-section and equivalent lumped circuit model of one section of an n-section coupled Interconnect model shown in Fig. 1. Where C_S, L_S are self-capacitance and self-inductance per unit length, C_C and L_m are mutual capacitance and mutual inductance. Z_O is the termination impedance.

The minimum number of segments are depending on the required bandwidth and the time delay, given by

$$n = \frac{l}{\Delta z} = \frac{10 l \sqrt{\varepsilon_r}}{t_r . C} \quad (3)$$

here n is the minimum number of lumped segments for an accurate model, t_r is rise (fall) time, l is length of an interconnect and C is the velocity of light. ε_r is dielectric constant.

Generalize equation for the lumped equivalent circuit of one-segment of an n-segment coupled interconnect lines, the voltage change caused by the inductance and the current change by the capacitance of coupled lines one and two is given by

$$V_1(z) - V_1(z + \Delta z) = -j\omega L_S i_1(z).\Delta z - j\omega L_m i_2(z).\Delta z \quad (4)$$

$$V_1(z) - V_1(z + \Delta z) = -j\omega [L_S i_1(z) + L_m i_2(z)].\Delta z \quad (5)$$

$$V_2(z) - V_2(z + \Delta z) = -j\omega [L_S i_2(z) + L_m i_1(z)].\Delta z \quad (6)$$

$$i_1(z) - i_1(z + \Delta z) = -j\omega (C_S + C_C) V_1(z) \Delta z + j\omega C_C V_2(z) \Delta z \quad (7)$$

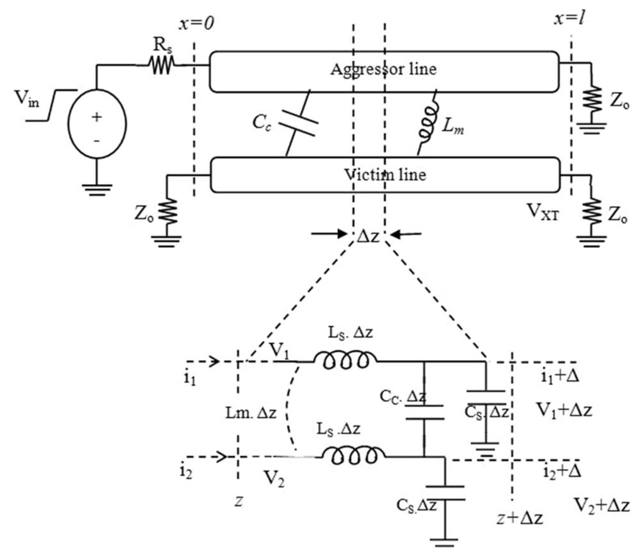

Fig. 1 The coupled distributed interconnect lines and lumped equivalent one-segment coupled interconnect model

$$i_1(z) - i_1(z+\Delta z) = -j\omega[(C_S + C_C)V_1(z) - C_C V_2(z)]\Delta z \quad (8)$$

$$i_2(z) - i_2(z+\Delta z) = -j\omega[(C_S + C_C)V_2(z) - C_C V_1(z)]\Delta z \quad (9)$$

The voltage and current relation of the coupled lumped circuit described in matrix form from (5) and (6) as,

$$\frac{d}{dz}\begin{bmatrix} V_1(z) - V_1(z+\Delta z) \\ V_2(z) - V_2(z+\Delta z) \end{bmatrix} = -j\omega \begin{bmatrix} L_S & L_m \\ L_m & L_S \end{bmatrix} \begin{bmatrix} i_1(z) \\ i_2(z) \end{bmatrix} \quad (10)$$

where inductance matrix, L= $\begin{bmatrix} L_S & L_m \\ L_m & L_S \end{bmatrix} H/m$. From equation (8) and (9) written as,

$$\frac{d}{dz}\begin{bmatrix} i_1(z) - i_1(z+\Delta z) \\ i_2(z) - i_2(z+\Delta z) \end{bmatrix} = -j\omega \begin{bmatrix} C_S & -C_C \\ -C_C & C_S \end{bmatrix} \begin{bmatrix} V_1(z) \\ V_2(z) \end{bmatrix} \quad (11)$$

For analyzing the multi-conductor transmission line, the crosstalk noise effects induced and changes of velocity has on SI issues. The effective Z_o and propagation velocity (V_P) is calculated by, $Z_0 = \sqrt{\frac{L_S}{C_S + C_C}}$ and $V_P = \frac{1}{\sqrt{L_S(C_S + C_C)}}$.

The mutual inductance and coupled capacitance causes Crosstalk noise at receiver end (V_{XT}) on the victim line when input signal is applied to an aggressor line. The noise effects has been different at receiver end and transmitter end on victim line. The crosstalk noise at receiver end on victim line is related to the difference between the inductive and capacitive coupled currents. Capacitive coupling effect is a short-range phenomenon and which exists only between coupled interconnects [9, 10]. The crosstalk noise at V_{XT} on victim line can be calculated as follow [11],

The voltages at receiver and transmitter end of victim line to get the amplitude of the crosstalk noise by applying ohm's law (for Fig. 1. lumped segment), Voltage at transmitter end on Victim line,

$$\Delta V_t = i_n Z_o \quad (12)$$

Voltage at V_{XT} (receiver end) on Victim line,

$$\Delta V_r = i_f Z_o \quad (13)$$

The coupled current from aggressor line to victim line through the C_C is,

$$i_C = C_m \Delta z \frac{\Delta V_1}{dt} \quad (14)$$

The Coupled current (i_C) splits into transmitter and receiver ends on victim line in both directions,

$$i_C = i_t + i_r \quad (15)$$

By combing the equation (12) and (14) thus the voltage created by the mutual capacitance,

$$\frac{\Delta V_t}{Z_O} + \frac{\Delta V_r}{Z_0} = C_m \Delta z \frac{\Delta V_1}{dt} \quad (16)$$

$$\Delta V_t + \Delta V_r = Z_o C_m \Delta z \frac{\Delta V_1}{dt} \quad (17)$$

The Coupling capacitance coefficient,

$$K_C \equiv \frac{The\ Mutual\ capacitance}{The\ total\ capacitance} \equiv \frac{C_C}{C_S + C_C} \quad (18)$$

By substituting Z_O in Eq. (17) we get,

$$\Delta V_t + \Delta V_r = \sqrt{\frac{L_S C_m^2}{C_S + C_m}} \Delta z \frac{\Delta V_1}{dt} \quad (19)$$

By substituting equation V_P in (19), we get sum of $\Delta V_t + \Delta V_r$ crosstalk noise by mutual capacitance,

$$\Delta V_t + \Delta V_r = \frac{1}{V_P} K_C \Delta z \frac{\Delta V_1}{dt} \quad (20)$$

The coupled current from aggressor to victim line through the mutually coupled Inductance is splits into transmitter and receiver ends on victim line in opposite directions,

$$\Delta V_t - \Delta V_r = L_m \Delta z \frac{\Delta V_1}{dt} \quad (21)$$

The Inductance coupling coefficient,

$$K_L \equiv \frac{The\ Mutual\ Inductance}{The\ Self - inductance} \equiv \frac{L_m}{L_S} \quad (22)$$

By applying of Ohm's law at transmitter end on victim line ($i_1 = \frac{V_1}{Z_0}$),

$$\Delta V_t - \Delta V_r = \Delta z \frac{L_m}{Z_O} \frac{\Delta V_1}{dt} \quad (23)$$

$$\Delta V_t - \Delta V_r = \Delta z \sqrt{L_m^2 (C_S + C_C)} \frac{L_m}{Z_O} \frac{\Delta V_1}{dt} \quad (24)$$

By solving equation (21) and (24),

$$\frac{\Delta V_r}{\Delta z} = \frac{K_C - K_L}{2V_P} \frac{\Delta V_1}{dt} \quad (25)$$

$$\frac{\Delta V_t}{\Delta z} = \frac{K_C + K_L}{2V_P} \frac{\Delta V_1}{dt} \quad (26)$$

Crosstalk noise at V_{XT} on victim line from $Z = 0$ to $Z = l$ gives the crosstalk noise,

$$V_r = \frac{1}{2}(K_C - K_L)\frac{1}{V_P}\frac{\Delta V_1}{dt} \quad (27)$$

By approximating $\frac{\Delta V_1}{dt}$ as 10% to 90% rise time t_r, then the final crosstalk noise is,

$$V_r = \frac{1}{2}(K_C - K_L)\frac{1}{V_P}\frac{V}{t_r} \quad (28)$$

The crosstalk noise is calculated on victim line by using Eq. (28).

3 Design of Cu interconnect model

The key factors in determining the performance of interconnect models are the characteristic impedance, delays and crosstalk noise. The design parameters of the copper (Cu) Interconnect model are given in [16, 17] at 32 nm technology node. The parameters specification for Cu interconnect model with 32 nm Technology node are given in Table. 1.

The design circuit parameters are extracted by using Electromagnetic 2D field solver for 32 nm Technology nodes [16] for the global interconnect model parameters tabulated in Table. 1. The rise and fall time is 10 ps with the clock frequency 10 Ghz. The supply voltage is 0.9 V and termination resistance (z_o) assumed as 50Ω. The extracted Resistance (R), capacitance (C) and inductance (C) matrix for 1 mm Cu interconnect length are,

$$R = \begin{bmatrix} 150 & 0 \\ 0 & 150 \end{bmatrix} \Omega/\text{mm}$$

$$L = \begin{bmatrix} 1.663 & 1.4220 \\ 1.422 & 1.663 \end{bmatrix} \text{nH/mm}$$

$$C = \begin{bmatrix} 26.487 & -59.629 \\ -59.629 & 26.487 \end{bmatrix} \text{fF/mm}$$

3.1 Shielding and physical spacing technique

For mitigating of crosstalk noise between coupled interconnects in IC, several techniques can be used. Increasing physical spacing and shield line insertion between coupled lines [18, 19]. Figure 2 illustrate an increasing of physical spacing between the coupled interconnects. The Increasing the physical spacing can reduce the crosstalk of coupling capacitance and mutual inductance between the aggressor

Table 1 Design of global level Cu Interconnect model parameters at 32 nm technology node [16, 17]

Tech. node (nm)	W (μm)	S (μm)	T (μm)	H (μm)	ε_r
32	0.30	0.30	0.504	0.504	2.2

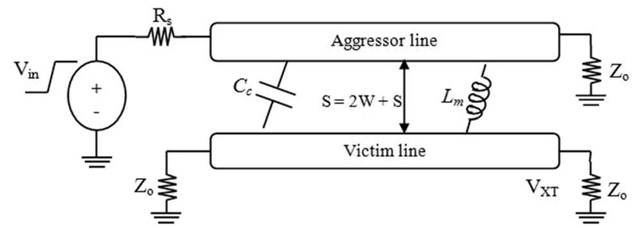

Fig. 2 Structure of crosstalk reduction with physical spacing between two coupled lines

and victim line. The reduction of crosstalk is approximately inversely proportional to the distance between coupled interconnects. The coupling capacitance can reduce significantly with increasing spacing. But, the mutual inductance is not significant reduced and it required additional return path to reduce the crosstalk. It's a long distance phenomenon. Shield line insertion can significantly reduce the crosstalk noise between the coupled interconnects [20]. The shield insertion between the coupled interconnects are shown in Fig. 3. The coupling capacitance significantly reduces crosstalk with shield line insertion between the aggressor and victim lines since it's a short distance phenomenon. The mutual inductance can moderately reduce crosstalk because of an inserted shield line formed as the current return path for both aggressor and victim line [19]. The shield insertion techniques is an effective method for minimizing crosstalk effects [21]. In this method, the Shield lines inserted between the signal lines. Shielding technique has two types: active shielding and passive shielding [18]. The active shielding line switches in the same direction of signal lines pattern, whereas, passive shielding both sides of the lines are grounded. Although active shielding reduces capacitive (inductive) coupling when shield line switches in the same (opposite) direction same as the signal line pattern [22]. Due to the high switching, power consumption is increasing in active shielding method [21]. To overcome these issues, passive shielding method plays an essential role in modern high-speed energy-efficient chips. Analysis has

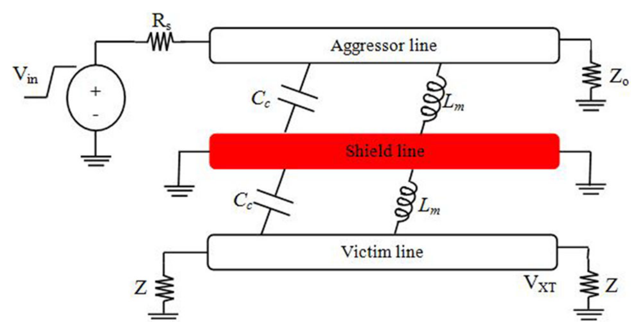

Fig. 3 Structure of shielded line insertion between the coupled interconnects

been carried out for design model with passive shielding technique for minimization of crosstalk and compared with increasing physical spacing between the coupled interconnects.

4 Simulation results and discussion

The design interconnect model was investigated at 32 nm technology nodes for different Cu Interconnect lengths. With the design parameters applied the input as step signal to aggressor line (in Fig. 1) of coupled interconnect model. In Fig. 4 shows crosstalk noise on victim line with and without shield insertion line technique with source resistances 5 at 32 nm technology node. It's monotonically increasing with increase of interconnect length for both technique. It is observed that, the crosstalk noise has been reduced significant with passive shield insertion technique compare to without shield insertion line.

With another crosstalk reduction method, which is an increasing the physical spacing between the coupled interconnects. The simulated results shown in Fig. 5. In both conditions, S = W and S = 2W + S are monotonically increase with increasing of Cu Interconnect length. From Fig. 5, it is observed that, as increasing the physical spacing between coupled lines, the crosstalk noise on victim line has reducing. In Fig. 6. shows that the comparison of shield insertion line and increasing physical spacing techniques between the coupled interconnects. It is observed that, an Insertion of shield line between coupled lines is having less crosstalk noise on victim line for high-speed digital ICs as compared with increasing the physical spacing.

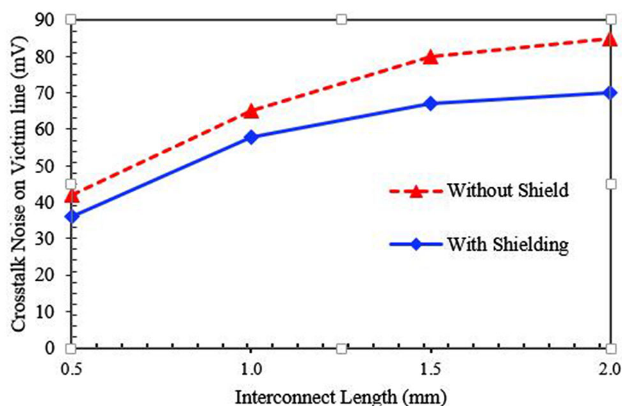

Fig. 4 Crosstalk noise on victim line for different Interconnect lengths with and without shield insertion technique

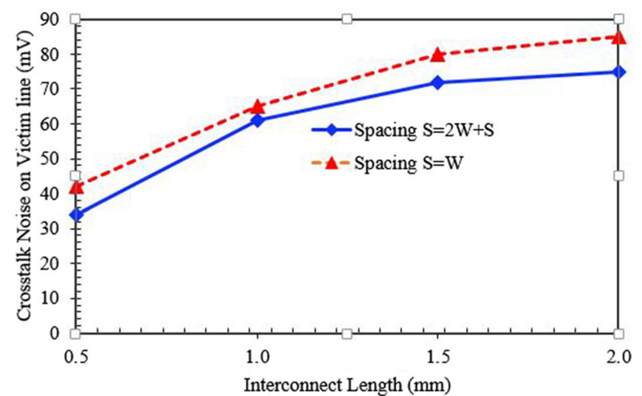

Fig. 5 Crosstalk noise on victim line for different interconnect lengths with increasing physical spacing

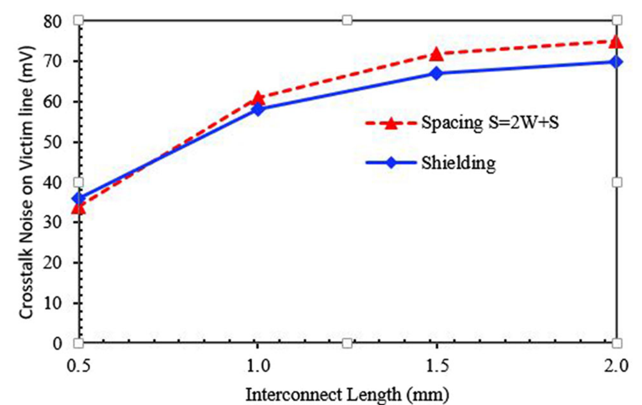

Fig. 6 Comparison of crosstalk noise on victim line for different interconnect lengths with increasing physical spacing and shield insertion techniques for coupled lines

5 Conclusion

For reduction of crosstalk effects in coupled Cu interconnects, the shield insertion technique and increasing the physical spacing method has been used. The analysis has been carried out at 32 nm technology node. At higher frequencies, the crosstalk noise is one of the dominant factor on-chip VLSI design. An accurate design of an interconnect model is required for avoiding the crosstalk effects. In this paper, analyzed the analytical model of coupled Cu Interconnect. For the reduction of of crosstalk noise with increasing the physical spacing and shield insertion techniques has been investigated comprehensively. The shield insertion technique has been preferable for minimization of crosstalk effects in coupled interconnects as compare to increasing the physical spacing between the coupled interconnects.

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References

1. Zhang XJ, Jiang W, Gao L, li H (2016) Impact of cross talk on signal integrity of high speed density ceramic package for IC. In: IEEE international conference on electronic packaging technology
2. Paul CR (2006) Introduction to electromagnetic compatibility. Wiley, New York, 1992, (2nd ed)
3. Paul CR (2008) Analysis of multiconductor transmission lines. Wiley, Hoboken, 1994, (2nd ed)
4. Catt I (1967) Crosstalk (noise) in digital systems. IEEE Trans Electron Comput 16(6):743–763
5. Vittal A, Sadowska M (1997) Crosstalk reduction for VLSI. IEEE Trans Comput-Aided Des Integr Circuits Syst 16(3):290–298
6. Zhang J, Friedman EG (2006) Crosstalk modeling for coupled RLC interconnects with application to shield insertion. IEEE Trans Very Large Scale Integr (VLSI) Circuits 14(6):641–646
7. Wu TL, Buesink F, Canavero F (2013) Overview of signal integrity and EMC design technologies on PCB: fundamentals and latest progress. IEEE Trans Electromagn Compat 55(4):624–638
8. Nakhla M, Achar R (2001) Simulation of high-speed interconnects. Proc IEEE 89(5):693–728
9. Bogatin E Signal and power integrity-simplified, Second edition, Prentice Hall Modern Semiconductor Design Series
10. Ullah MS, Chowdhury MH (2017) Analytical models of high-speed RLC interconnect delay for complex and real poles. IEEE Trans Very Large Scale Integr (VLSI) Syst 25(6):1831–1841
11. Hall SH, Heck HL (2009) Advanced signal integrity for high-speed digital designs. Wiley, Hoboken
12. Hedari P, Abbaspour S, Pedram M Interconnect energy in high speed ULSI circuits. Dept of EE and CS, University of California, Irvine, CA 92697
13. Yuan CP, Trick TN (1982) A simple formula for the estimation of the capacitance of two-dimensional interconnects in VLSI circuits. IEEE Electron Device Lett 3:391–393
14. Delorme N, Belleville M, Chilo J (1996) Inductance and capacitance analytic formulas for VLSI interconnection. Electron Lett 32:996–997
15. Hall SH, Hall GW, McCall JA (2000) High-speed digital system design. Wiley, Hoboken
16. Kose S, Salman E, Friedman EG (2011) Shielding methodologies in the presence of power/ground noise. IEEE Trans VLSI Syst 19(8):1458–1468
17. Wong SC, Lee GY, Ma D-J (2000) Modeling of interconnect capacitance, delay, and crosstalk in VLSI. IEEE Trans Semicond Manuf 13(1):108–111
18. Zhang J, Friedman EG (2006) Crosstalk modeling for coupled RLC interconnects with application to shield insertion. IEEE Trans Very Large Scale Integr Syst 14(6):641–646
19. Zhang J, Friedman EG (2004) Effect of shield insertion on reducing crosstalk noise between coupled interconnects. 2004 IEEE international symposium on circuits and systems (IEEE Cat. No.04CH37512), vol 2, pp II-529–32
20. Zhang J, Friedman EG (2004) Mutual inductance modeling for multiple RLC interconnects with application to shield insertion. IEEE International SOC Conference proceedings
21. Ghoneima M, Ismail YI, Khellah MM, Tschanz JW, De V (2006) Formal derivation of optimal active shielding for. Comput Des 25(5):821–836
22. Kaul H, Sylvester D, Blaauw D (2002) Active shielding of RLC global interconnects, Proceedings of the 8th ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems - TAU