Electronic Materials Letters (2024) 20:122–130
https://doi.org/10.1007/s13391-023-00444-1

ORIGINAL ARTICLE - ELECTRONICS, MAGNETICS AND PHOTONICS

Vertical Pattern of Interconnects to Bypass High Strain Near a Hard Die on a Flexible Substrate Under Mechanical Bending

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Received: 16 March 2023 / Accepted: 4 June 2023 / Published online: 19 June 2023
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Abstract
The distinguishing feature of a flexible electronic device is that it maintains its function even when the shape changes repeatedly. As the degree of integration of flexible devices increases, revealing failure mechanisms and extending the lifetime of the flexible devices are getting more difficult. One of the potential damage zones is the interface of heterogeneous material components, where strain can be localized due to the mismatch of mechanical properties. In this study, we investigate the mechanically reliable interconnect design of the flexible printed circuit board (FPCB) system in which the packaging chip is integrated. When the FPCB was bent, folding occurred at the edge of the packaging chip due to the high bending rigidity compared with the plastic substrate and resulted in high strain concentration. By introducing interconnect architecture that bypassed the strain concentration area around the packaging chip, mechanical damage of the interconnects was successfully reduced. Through finite element simulation, the strain applied to the interconnect crossing the strain-concentrated region was predicted to be 2 times larger than that bypassing the strain-concentrated region, from 8.32 to 4.64%. In addition, the strain gap of these two interconnects could be increased as the Young's modulus mismatch between the packaging chip and the substrate increased. This study is expected to improve the design guidelines to mechanically reliable interconnects in highly integrated flexible electronics.

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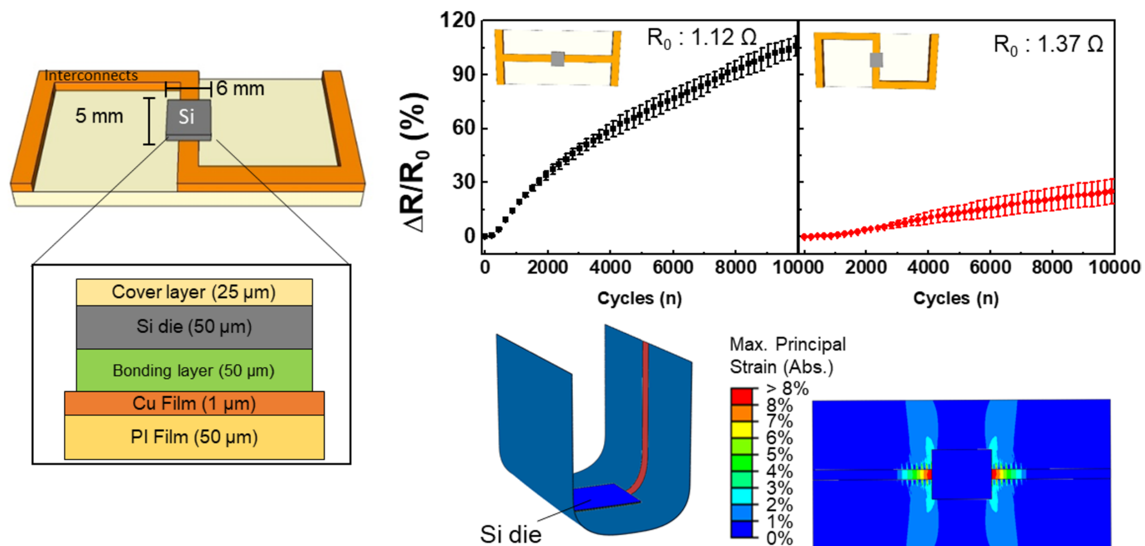
Graphical Abstract



Keywords Flexible · Reliability · Fatigue · Patterned interconnects · Chip bending

1 Introduction

With the advent of the internet of things, the demand for electronic devices that are compact and portable, flexible, and can be wearable for the human body is increasing in various fields, including flexible and stretchable interconnects [1], displays [2], batteries[3, 4], sensors [5], optics [6], and robotics [7]. Among the flexible device modules, interconnects are one of the most important component that determine the lifetime of the entire flexible device. Since the interconnects are deposited over the entire region of the device compared with others, they can be exposed to mechanical deformation and failures more easily during operation. To make the interconnects mechanically reliable, researchers have developed conductive materials that are intrinsically soft, such as conductive polymers [8, 9], gels [10], and liquid metals [11]. Strechable interconnects can also be realized by introducing micro/macrostructures that can accommodate large deformations without degradation, e.g., nanowires and nanofibers that can accommodate the strain from rotation and alignment of wires/fibers [12, 13], interconnects that are curved to to accommodate stretch without strain generation [3, 14, 15], and introducing voids and holes that can blunt crack propagations and further catastrophic failures [16].

Not only the innate mechanical properties of individual materials but also the mismatch of mechanical properties among individual materials that are physically contacted should be considered to guarantee the mechanical reliability of integrated devices. Previous literature reported that the high level of mechanical strain is localized at the interface between heterogeneous material components during the stretching or bending of a device, which can damage and degrade the whole device [15, 17]. In other words, even if a globally uniform deformation is applied to a device, the strain at local interfacial sites may not be uniform and the device can be broken sooner than expected.

In this study, we proposed a guideline of architectural design of interconnects in flexible devices that minimizes the mechanical strain through the investigation of failure mechanisms of flexible printed circuit boards (FPCBs). Experimental and numerical analysis provided the lifetime and the strain distribution of the deformed FPCBs according to the alignment and geometry of the metal interconnects under the presence of a rigid chip die. Since most flexible electronics are easily exposed to repetitive deformation, a bending fatigue reliability test was conducted on the FPCBs. By designing the architecture of the interconnects to bypass the strain-concentrated region, this study revealed a way of minimizing the level and controlling the localized area of strain on the interconnects and improved the mechanical reliability without additional follow-up treatments.

2 Experimental Design

Copper (Cu) interconnects are designed as three types: first is a parallel-type design, which has a straight line connecting both ends with the shortest distance; the other two types have a vertical line in the middle of parallel lines, which

connect the central die perpendicular to the bending direction with 10-mm and 15-mm lengths, respectively (Fig. 1a). The vertical line has proven to be a desirable alignment since it is aligned parallel to the bending axis so that it can avoid electrical degradation, even when mechanical cracks are formed (See the supplementary information and Fig. S1). We thermally deposited 1-μm-thick Cu interconnects on a 50 μm-thick polyimide (PI) substrate at 1×10^{-6} Torr. The deposition rate was 0.8 nm/s. A silicon (Si) chip die with a 50-μm-thick bonding layer was attached on the deposited Cu film and was followed by 25-μm-thick cover layer. The scale of the bonded Si chip die was 5 mm × 6 mm.

Figure 1b shows our U-bending fatigue test system, which can perform repeated folding and unfolding by pushing and pulling the rigid plates on both sides [18]. The bending radius was set to be 3 mm, with the Cu interconnects and Si chip die located at the inner side of curvature, where the compressive strain is approximately 0.83%. Bending frequency was set to be 1 Hz, and the number of bending cycles were 10^4. The edges of the samples were clamped with metal grips to form electrical contact. The electrical resistance of Cu interconnects was measured in situ (Keithley 2700 Multimeter) during the repeated deformation. After the fatigue test, the surface of the Cu interconnects was observed by field emission scanning electron microscope (SEM) and optical microscope.

To see the relationship between the orientation angle of Cu interconnects and bending direction, 1-mm-long Cu interconnects with 100-μm width were patterned with orientation angles varying: 0° (vertically aligned to the bending axis), 30°, 45°, 60°, and 90° (aligned parallel to the bending axis). The angle was defined as how much tilting was made to the Cu interconnects from the bending direction. The bending radius was 3 mm, and the Cu interconnects were placed facing inwards of the curvature so that compressive strain was applied.

Finite element (FE) simulation was conducted with ABAQUS (Dassault Systems, France) to figure out how the strain distributed when the specimens were deformed. Two different calculations were performed. First, we investigated the dependence of Young's modulus mismatch between chip packaging and substrate on strain level. Applying different modulus values to a chip, four types of packaging materials were assumed: anisotropic conductive films (ACF), PI,

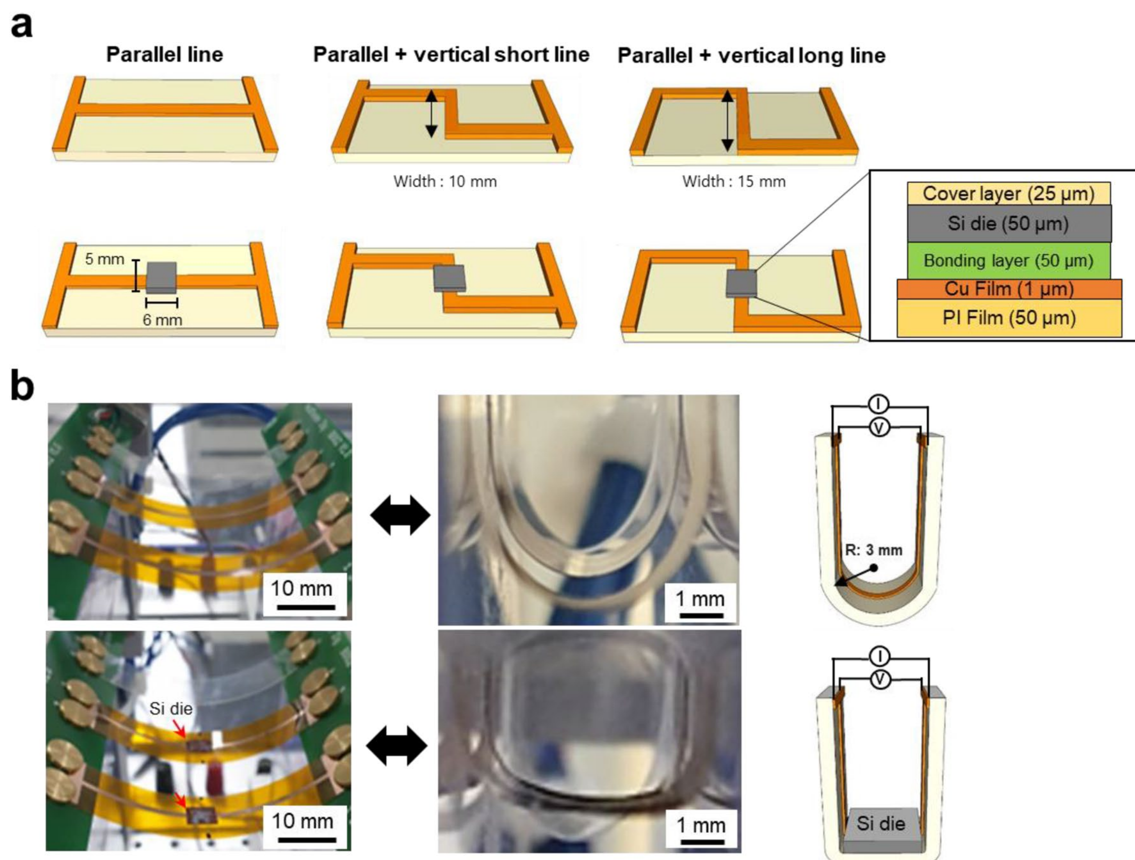


Fig. 1 **a** Schematic illustrations of FPCBs varying with the architecture of Cu interconnects and presence of Si chip die. **b** Photos and schematic illustrations of the FPCB samples loaded on U-bending fatigue test system with 3-mm bending radius

epoxy molding compound (EMC), and Si. The Young's modulus of ACF, PI, EMC, and Si were set to be 0.9, 2.8, 10, and 130 GPa, and the Poisson's ratio was set to be 0.5 0.34, 0.2, and 0.28, respectively [19–22]. Line profiles of maximum principal strain were obtained along the line crossing the substrate from center to edge of the substrate around the chip edge. Second, we conducted the simulation including Cu interconnects with the same geometries prepared in the experiments. Young's modulus and Poisson's ratio of Cu were set to be 130 GPa and 0.36, respectively, using a perfect plastic model whose yield stress was set to be 271 MPa [23]. C3D8 meshes were applied to each element. The bonding layer and cover layer were excluded to reduce the cost of computation. U-bending deformation was simulated by narrowing the interval of both sides of the PI edges that were confined to the rigid plate by displacement control to have a 4.5-mm bending radius with a 1.5-mm margin.

3 Results and Discussion

First, U-bending fatigue tests were conducted to investigate the dependence of the presence of a Si die on fatigue of the Cu interconnects, as well as tests varying the interconnect design. Without the Si die, the specimen was uniformly bent (Fig. 1b). On the other hand, when the specimen included the Si die, local folding of Cu/PI occurred around the edge of the Si die. Young's modulus and bending rigidity are 46 times larger for Si compared with PI substrate, making the substrate flat where the Si chip is placed. We hypothesized that the level of strain that would be generated at the locally folded sites would be higher than the strain derived by a uniform bending curvature, which would make the FPCB more vulnerable to the fatigue.

Electrical resistance of Cu interconnects was monitored in situ during repeated bending to compare the fatigue lifetime. The compressive strain applied to the Cu interconnects was calculated to be 0.83%, following thin film bending theory, which can be approximated by t/2R, where t and R are the thickness and bending radius, respectively [24]. When a Si die was not included, the change in electrical resistance of Cu the interconnects were negligible (Fig. 2a), while a gradual increase in resistance increase was observed in Cu interconnects with a Si die (Fig. 2b) during 10^4 cycles of repeated bending. The increase in electrical resistance of Cu interconnects was related to the formation of mechanical cracks that blocked the conduction path [25], indicating that mechanical damage occurred in Cu interconnects with a Si chip. In addition, from the resistance curve in Fig. 2b, we observed that when the length of the vertical interconnect line increased, the increment of resistance decreased. For example, the final resistance of the parallel-type interconnect design increased to 105% compared with the initial design, while those of the parallel type with a short vertical line and the parallel type with long vertical line increased 45% and 25%, respectively.

The SEM images in Fig. 3 shows the crack damage morphologies of Cu interconnects with a Si die. Extrusions and intrusions are found around the cracks, indicating that the mechanism of crack formation was derived by the slip of piled-up dislocations [24–27]. In all three cases, cracks were formed at the parallel lines of interconnects where folding occurred. From the SEM images, we observed that the crack densities decreased as the length of the vertical line

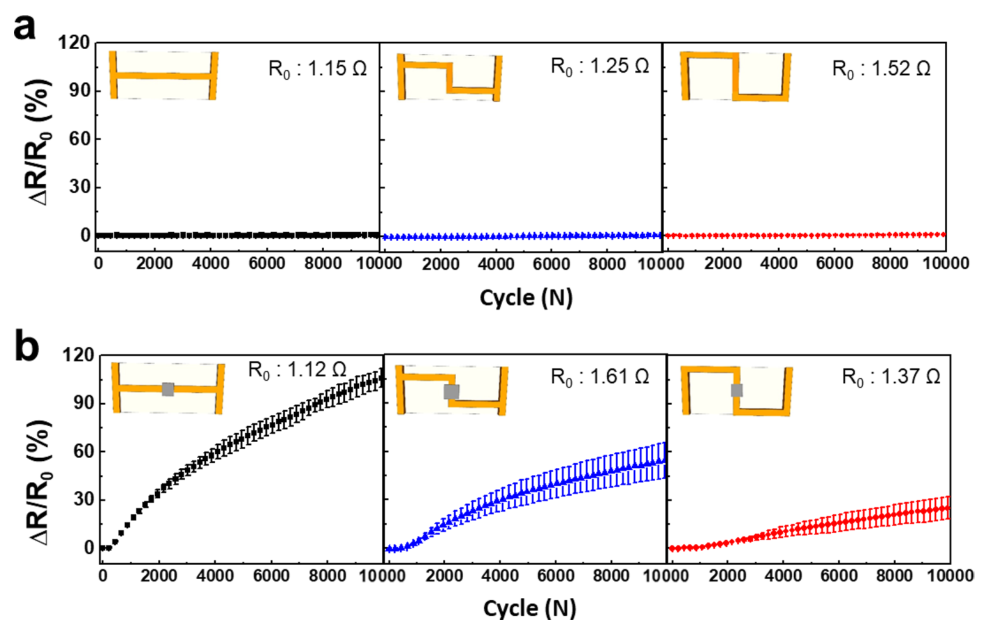


Fig. 2 Normalized electrical resistance curve of Cu interconnects **a** without a Si die and **b** with a die under repeated bending. Inset figures showed the architectures of Cu interconnects that were used for the tests

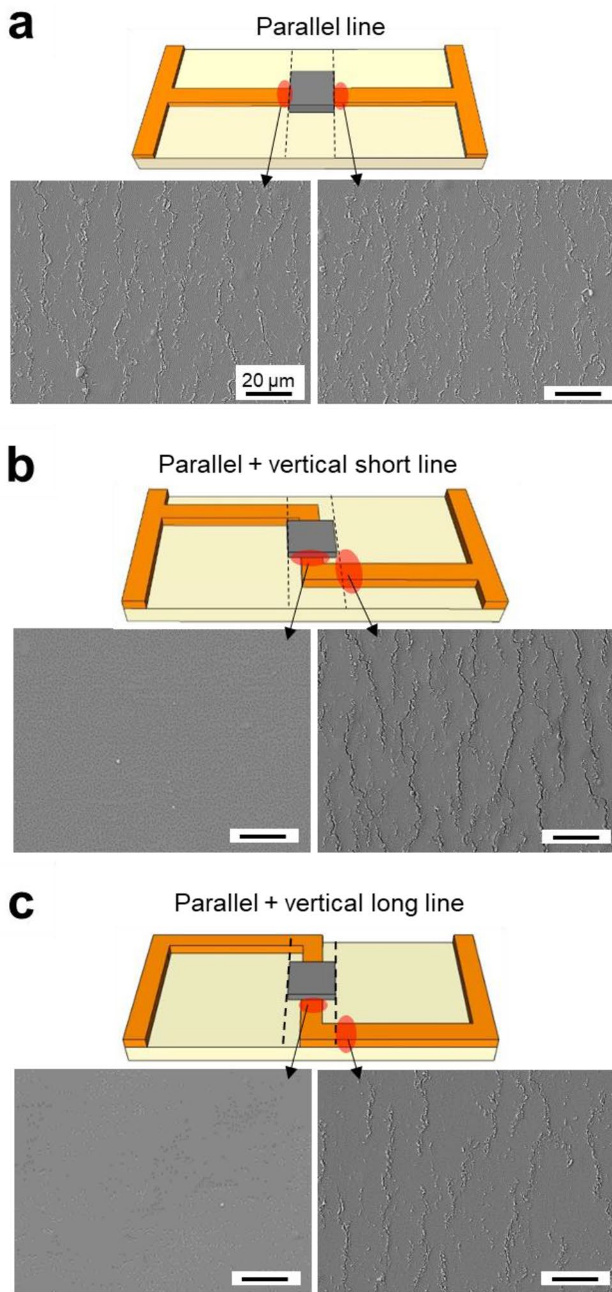


Fig. 3 FE-SEM images of the Cu interconnects of **a** parallel line **b** parallel with short vertical line, and **c** parallel with long vertical line after a fatigue test. Cracks were formed along the parallel line in all the cases. The density of cracks decreased as the parallel line was positioned closer to the edge of the substrate

increased, explaining the difference in the change of electrical resistance in Fig. 2b.

Figure 4a shows the interconnect pattern with different alignment angles to the bending axis. The line pattern was tilted from fully vertical to parallel to the bending axis to confirm that path pattern affected reliability of whole circuit. Figure 4b shows the electrical resistance changes of the Cu pattern after 10^4 cycles under a 1.67% bending strain calculated by the approximated bending theory of thin film on substrate [27]. As the tilting angle increased, the change in electrical resistance decreased. To understand the correlation between the alignment of the interconnect and the resistance, we established an analytic model that shows the relationship between resistance and crack length [28]:

$$R = R_0 + Cl_c^b \tag{1}$$

where R is the electrical resistance of the interconnect after the fatigue test, R_0 is the initial electrical resistance of the film, C is a constant, l_c is the crack length across the interconnect, and b is the exponent of crack length. If we define the angle between the bending direction and the interconnect as θ, then the Eq. (1) can be expressed as follows:

$$R(\theta) = R_0 + C\left(l_c cos\theta\right)^b \tag{2}$$

$$\Delta R(\theta) = \Delta R(0^\circ) + C(cos\theta)^b \tag{3}$$

where $R(\theta)$ is the electrical resistance of the film after fatigue test depending on the pattern angle. The exponent b has a value of 2.268 in the case of a conductive film [28], and in our case of a Cu line with 100-μm width was plotted by applying the value of 3.25 to the exponent in Fig. 4b. The resistance of vertically aligned interconnects increased 4000%, while the increase in resistance of parallel-aligned interconnects was negligible. Figure 4b shows that our established analytic model was well matched with the experimental results.

Figure 4c shows SEM images of fatigue cracks of the Cu interconnects that were aligned at 0° and 90° after 10^4 cycles of sliding bending. The crack density in both cases was similar. In the case of the 0° tilting angle, the cracks grew perpendicular to the conduction pathway so that they blocked the electrical conduction and caused severe increase in resistance [29]. In contrast, the cracks grew parallel to the direction of the conduction pathway so that they did not interfere with electrical conduction at the 90° tilting angle. This difference indicated that for a uniaxial bending, the interconnect should be aligned parallel to the bending axis to prevent electrical performance degradation. Furthermore, in the case of a pattern perpendicular to repeated strain, the degradation of electrical conduction is not affected, allowing this design rule to be applied for bypassing stress concentration under various form factors.

Figure 5 represents the FE simulation results of packaging die/Cu line/PI substrate when bent. The deformed shape and maximum principal strain contour of packaging die/Cu line/PI substrate are displayed in Fig. 4a, when the samples were bent, varying with the Young's modulus of chip die. Four different materials, ACF, PI, EMC, and Si,

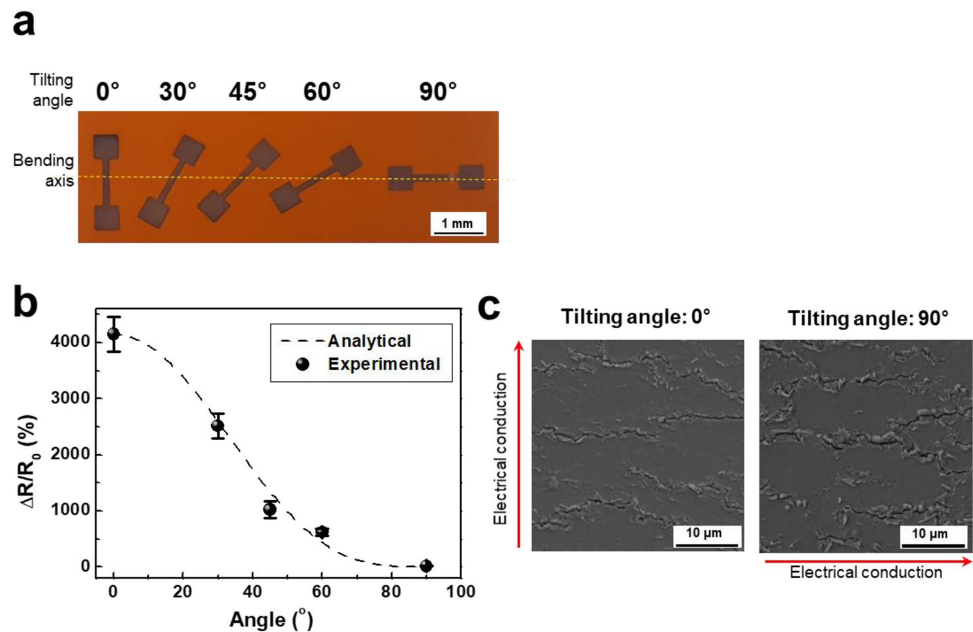


Fig. 4 **a** Cu interconnects with various alignment angle were loaded on the bending system. The alignment angle varied from 0° to 90°. **b** Analytic calculation and experimental data of normalized electrical resistance of Cu interconnects depending on alignment angle after fatigue. **c** Crack images of Cu interconnects with 0° (left) and 90° (right) alignment angles

were subjected to the packaging die. To clearly show the strain distribution, the strain contours are provided with the simulated model unfolded. As Young's modulus of the die increased, the substrate was folded more sharply and the strain level at the die edge/substrate interface increased due to the increase of the bending rigidity of the die. Figure 5b and c represent the line profiles of the maximum principal strain of parallel Cu line depending on Young's modulus of the chip die (following the white dashed line denoted in upper illustration). When a die was used, the maximum strain value at the parallel Cu line in Fig. 5b increased from 5.59 to 8.32% as the Young's modulus of the die increased. One more important thing to note is that the strain level was highest at the center of where the die was placed and decreased toward the longer side of the edge of the substrate. The maximum strain value at the parallel Cu line with a vertical long pattern in Fig. 5c increased from 4.09 to 4.64% as the Young's modulus of the die increased; however, the amount of increase was only a third of that compared with the parallel-only design. This reduction can be understood as substrate bending becomes more uniform the farther it moves away from the chip. (For example, as the width of the sample approaches infinity, the strain will converge to 0.97%.) For the Cu interconnect including Si die, the strain decreased from 8.32 to 4.64% as it went from center to edge. This implies that as the metal interconnects are designed to be farther from the die, the effective strain generated on the interconnects will decrease and thus the mechanical stability can be improved. The strain gap between the center and the edge of the substrate grew larger as the rigidity ratio of chip and the substrate increased, which suggested the importance of the location and geometry of metal interconnects when developing FPCBs including rigid chips.

Finally, bending simulation of FPCBs was conducted to include the Cu interconnects with three different geometries that were used in experiments. Figure 5d represents the maximum principal strain profile of Cu interconnects along the longitudinal direction of the specimen. The decreased strain level around 15 mm on the x-axis well describes the damage-free surface of the vertical lines of Cu interconnects in Fig. 3. The peak of strain was getting broader and lower as it went toward to the edge, implying that it would be desirable for metal interconnects to be designed as far away from the localized strain area as possible.

4 Conclusion

This paper reveals the mechanical reliability of metal interconnects of FPCBs with packaging components and suggests design guideline of interconnects for improving mechanical reliability under uniaxial bending. As a result of the repeated bending deformation of the Si/Cu/PI integrated module, we proved through experiments and calculations that (1) local folding occurred at the interface of the Si die edge due to the high bending rigidity of Si and (2) the Cu interconnects were mechanically damaged due to the localized strain at the die edge. The degree of folding or strain level at the edge can be determined by the mismatch of Young's modulus between the chip die and the substrate. For example, as the mismatch decreased, the strain level decreased. As the interconnect was located farther from the rigid die edge, the strain generated at the interconnect decreased and was able

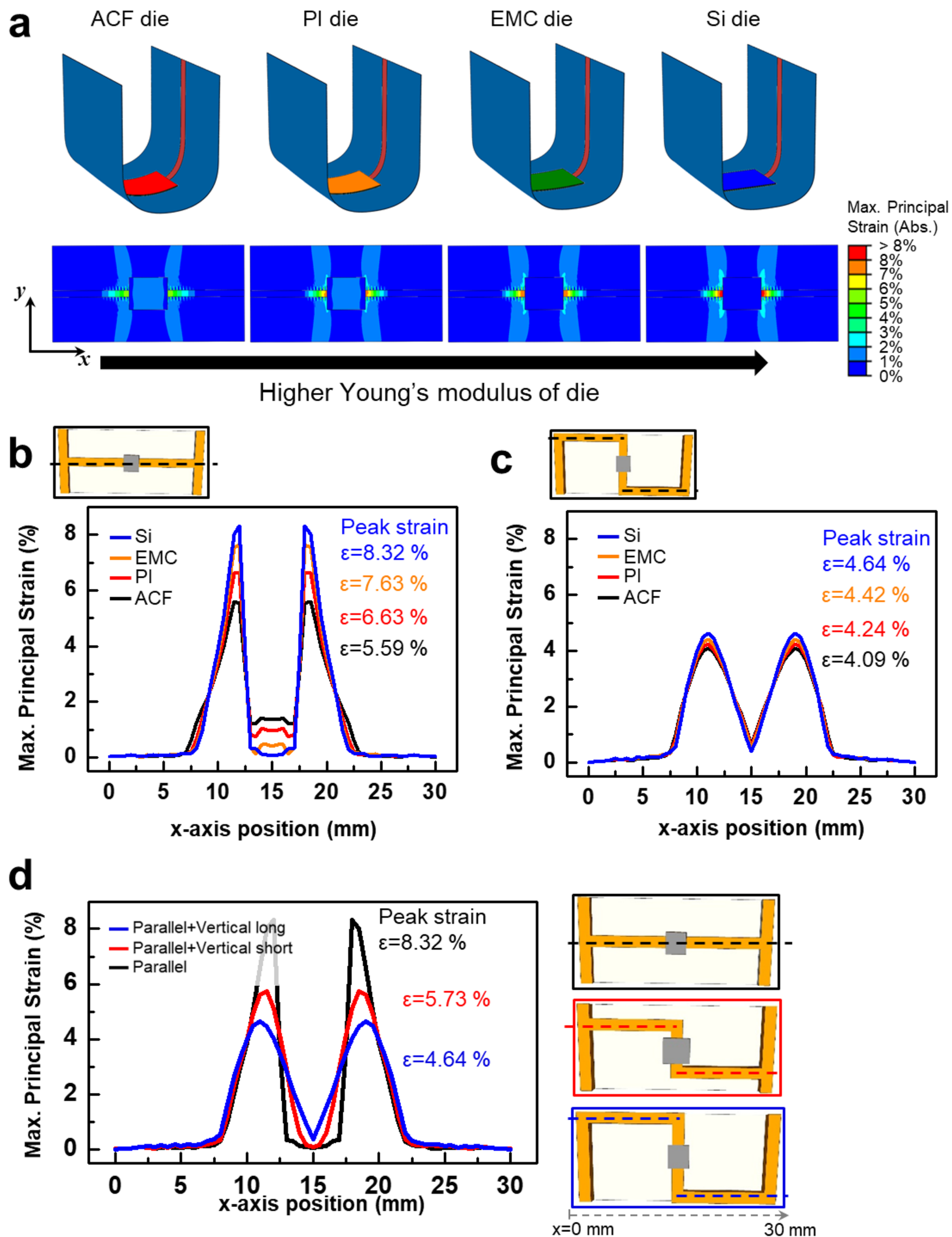


Fig. 5 FE simulation results. **a** Deformation shape and maximum principal strain contour of various die on PI substrate when bent with 4.5-mm bending radius. Maximum principal strain profile along the longitudinal Cu line depending on the y-axis position of **b** parallel line and **c** parallel line with long vertical pattern. The positions are denoted in the dashed lines in the schematic illustrations on the upper side of the strain profile. As Young's modulus mismatch of die and substrate increased, the strain gap between the center and the edge increased. **d** Maximum principal strain profile along the longitudinal Cu line of the substrate depending on the length of the vertical pattern. The positions are denoted in the dashed lines in the schematic illustrations on the right side of the strain profile

to delay mechanical deterioration. This research is expected to provide the design guidelines for the highly reliable interconnect architecture of flexible electronics.

Acknowledgements This work was supported by the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT (No. 2022R1A5A7000765), MOTIE(Ministry of Trade, Industry & Energy (20019469) and KSRC(Korea Semiconductor Research Consortium) (852) support program for the development of the future semiconductor device, and Technology Innovation Program (20011119) funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea).

Declarations

Conflict of interest The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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