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Size Effect on the Electromigration Characteristics of Flip Chip Pb-free Solder Bumps

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Abstract

To understand the size effect on electromigration (EM) behavior in flip chip Pb-free Sn-3.5Ag solder bumps, EM tests were performed with changes in the pad opening size and solder bump height at 140 °C and 4.6×10^4 A/cm². Additionally, to exclude extrinsic factors such as Joule heating, EM behavior was observed using a multi Sn96.5Ag3.0Cu0.5 solder line sample at 150 °C and $6-7.5 \times 10^4$ A/cm². The EM lifetime increased with decreasing pad opening size and bump height, and the EM critical current density (J_{th}) increased with decreasing line length. This result indicates that the EM resistance increases as the dimensions of the solder bump decreases, which can be understood by the EM jL product.

Graphical Abstract



Keywords Electromigration \cdot Joule heating \cdot Pb-free solder bump \cdot jL product \cdot Lifetime

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1 Introduction

In recent years, flip chip packaging technology has been adopted for high-density packaging due to its superior electrical performance, better heat dissipation performance and lower cost than other materials [1, 2]. There is a trend to require a higher performance of microelectronic devices and a trend for the solder bumps to decrease in size [3, 4]. Additionally, the solder bump pitch and the diameter of under bump metallization (UBM) have been decreasing [5]. Therefore, a higher current density and higher chip temperature result in serious reliability issues in flip chip solder bumps over time, such as electromigration (EM), thermomigration (TM), Joule heating, and current crowding. [1, 6, 7]. Over the last 30 years, EM phenomena have been investigated extensively in chip interconnects such as Al and Cu, where EM is the physical phenomenon of metal atoms migrating in the direction of electron flow due to momentum transfer between conducting electrons and diffusing metal atoms [8-10].

Recently, many researchers have reported EM behaviors in various flip chip Pb-free solder bump structures [11–17]. As a result, the current density in solder bumps continuously increases with each generation, making EM an important reliability issue in electronic packaging technology [3, 18–23].

During EM, the solder may react with the UBM to form intermetallic compounds (IMCs), whereby the passivation opening is depleted [3]. As the size of the solder bump decreases, the effect of the IMC layer on EM becomes more important [3]. Dennis et al. investigated the effect of passivation opening diameter and UBM diameter on the EM resistance of SnPb eutectic solder bumps. They reported that the EM lifetime is strongly dependent on the UBM area but weakly on the passivation open area [24]. Nah et al. reported using a thick Cu column as the UBM material and only a tiny amount of solder is necessary, where the bump height is as low as 20 µm [3, 25]. During EM, comprehensive Cu–Sn IMCs formed in the joints [3]. In addition, some of the IMC layers may bridge the joints, or the entire solder joints may be transformed into IMC joints [3]. Therefore, the IMC layer may play an important role in EM in solder joints with a low bump height [3]. C. C. Wei et al. investigated that the shrinking in bump size continues the effect of IMCs on EM becomes more pronounced [3]. In addition, no voids were seen in the 5 µm long stripes, even when the stripes were stressed for up to 900 h. More depletions were observed in longer stripes [3]. R. Huang et al. [26] reported the influence of solder composition, bump size and reflow cycle on the interface reaction between solder alloys and Cu substrates. In this experiment, the diameter of IMC grains increases with decreasing solder ball diameter (200 µm,

500 μ m, and 800 μ m) after one reflow cycle, and a notable size effect occurs in the Sn/Cu solder bump. As the number of reflow cycles increases, the size effect on the interfacial reaction is more pronounced. This phenomenon is the most direct kinetic factor in that the average Cu concentration in the small-sized solder ball rises faster than the other balls [26]. Park et al. [27] studied the solder volume effects on the EM failure mechanism of Cu/Ni/Sn-2.5Ag microbump structures. They found that the electrical resistance of Cu/ Ni/Sn-Ag microbumps with large solder volumes increased quickly, and those with small solder volumes increased slowly, thus demonstrating the dependence of IMC formation mechanisms on solder volume. In the case of a structure with a large solder volume, the Ni barrier was fully consumed because the volume of solder was sufficient for the reaction with Ni barriers. In the case of a structure with a small solder volume, the Ni barrier was partially consumed due to the limited solder volume [27]. However, although the trend of a smaller package is a critical issue, the effect of the solder bump size on EM behavior has rarely been reported.

This study considers the effect of the pad opening size and solder bump height on the EM lifetime of flip chip Cu/ Sn-3.5Ag/Cu solder bumps. Additionally, to focus on EM behavior by excluding extrinsic factors such as Joule heating, EM tests were performed using a multi Sn96.5Ag3.0Cu0.5 (SAC305) solder line sample. The size effect on EM resistance was evaluated to determine the association between the EM lifetime in the solder bump structure and EM behavior in a multiedge drift line structure.

2 Experimental Procedures

A flip chip Cu/Sn-3.5Ag/Cu solder bump sample consisting of a Si/Si structure was used to evaluate the EM lifetimes with changes in the pad opening size and bump height in the solder bump. The Cu line of the chip and substrate side was electroplated with a 4 µm thick Cu layer, and UBM consisted of the sputter-deposition of a 0.5 µm thick Ti/Cu layer. The Sn-3.5Ag solder was electroplated on the UBM. The pad opening side of the chip was patterned at 60, 80, and 100 μ m, and the substrate side was fixed at 80 µm. Three types of chips and one type of substrate were reflowed at 250 °C for 1 min, and samples of different pad opening sizes at constant bump heights and those of different bump heights at constant pad opening sizes were made by controlling the loading on the chip side during flip chip bonding, as shown in Fig. 1. The EM lifetime parameters for each sample condition are presented in Table 1. Figure 1e shows a schematic diagram of electron flow in the EM test sample. The single solder bump (bump (a), as shown in Fig. 1e) on the left side will fail earlier than the three parallel bumps on the right side due





(b) 100 um 80 um 20KU 10Mm 20KU 10Mm 20KU 10Mm 20KU 10Mm

(c)



Chip side



Fig. 1 SEM cross-section images of solder bump of various pad opening sizes and bump heights; **a** 60 μ m, **b** 80 μ m, **c** 100 μ m, **d** 65 μ m, and **e** Schematic diagram of electron flow in EM test sample

 Table 1
 EM lifetime test conditions for various bump heights and pad opening sizes

Bump height (um)	Pad open size (um)	Temp. (°C)	Current den- sity (A/cm ²)	Applied current (A)
80	60	160	4.6×10^4	1.3
80	80	160	4.6×10^4	2.3
80	100	160	4.6×10^4	3.6
65	80	160	4.6×10^4	2.3

to the current density being 3 times higher than the others. Therefore, EM failure will occur at this single bump. The EM lifetime was conducted at current densities of 4.6×10^4 A/cm² and temperatures of 160° C with several samples for each structure tested in a conventional annealing oven. The EM phenomenon in solder bump structures is very complex. It is related to several elements (such as current crowding, Joule heating, IMC decomposition, Kirkendall voiding, and TM) that arise because of the unique geometry, interfacial UBM structure, and complex material structures.

To exclude these various factors related to the solder bump structures, the EM phenomenon was only observed using thin edge drift samples patterned with 100 µm, 200 µm, and 500 µm long lines on a 0.3 µm-thick Ni thin film line structure. To separate between lines, SiO₂ "walls" coated on the Ni line were intentionally left. A small amount of SAC305 solder paste was dropped on the revealed Ni area and reflowed at 220 °C for approximately 5 s. The solder was polished until the SnAgCu line reached a thickness of about 3-5 µm. The schematics of the multi-SnAgCu solder line used in this study are shown in Fig. 2. All samples were annealed for 4 h before conducting the EM test at 150 °C to stabilize their microstructure and the IMC formation between Cu/Ni and the solder. EM tests were performed at 140 °C and $6-7.5 \times 10^4$ A/cm² and realtime microstructure changes were observed in a scanning electron microscopy (SEM) chamber. The edge displacement at the cathode side defined the edge drift area as a function of the stress time divided by the 100 µm line width.



Fig. 2 Schematic diagram of the thin film multiedge drift sample for the EM test

3 Results and Discussion

Figure 3 shows the EM lifetime test results with the pad opening size at a constant bump height. Figure 3a shows the changes in resistance and temperature as a function of current stressing time at 160 °C with current density of 4.6×10^4 A/cm². The initial resistance gradually increases shortly after the electric current is applied. Finally, an abrupt increase in resistance occurs approximately after a 20% increase in resistance, indicating an open electrical failure of the solder bump. Figure 3b shows the association between the cumulative distribution function (CDF) and the time to failure (TTF). As a result of the EM test with the pad opening size at 160 °C and 4.6×10^4 A/cm², the EM lifetimes increase with decreasing pad opening size, as shown in Fig. 3b. This observation indicated that the EM lifetime of the solder bump was affected by the pad opening size under constant stress conditions. The current density of the stress condition was calculated based on the pad opening size. Therefore, although the current density is constant at 4.6×10^4 A/cm², the applied current with each pad opening size is different. Solder bumps with 60, 80, and 100 µm pad opening sizes were applied at 1.3, 2.3, and 3.6 A, respectively. This applied current in the solder bump is a very important factor because the current flow-induced Joule heating is proportional to the square current [16]. The Joule heating power can be depicted as [6]:

$$P = IV = I^2 R \tag{1}$$

where *P* is the Joule heating power, and *I*, *V*, and *R* are the current, the voltage, and the resistance, respectively. The Joule heating power increases with increasing applied current. Joule heating mostly occurs at the chip side in the solder bump, accelerates the EM phenomenon and induces a temperature gradient between the chip and substrate side in the solder bump [1, 15, 16, 28]. Joule heating-induced high temperature at the chip side of the solder bump is enough to accelerate the EM phenomenon because EM is a function of temperature and current density. The temperature gradient in the solder bump is the driving force for TM such that metal atoms migrate from high to low temperature [17, 29–32].

In our cases, since the applied current is different from the pad opening size, the effect of Joule heating is also different. That is, the current-induced effect of Joule heating increases with increasing pad opening size. As the Joule heating increases, the EM lifetime is shorter due to EM and TM acceleration.

Figure 3c shows the association between the mean time to failure (MTTF) and applied current. The MTTF is inversely proportional to the square current due to the increasing Joule heating. It seems that MTTF increases as the pad opening size decreases.



Fig. 3 a Resistance change versus time curve of a flip chip Sn-3.5Ag solder bump at 160 °C and 4.6×10^4 A/cm², **b** EM lifetime test results with pad opening size at constant current density, and **c** MTTF(t₅₀) variations w.r.t. electronic current

Figure 4 shows the EM lifetime test results with bump height variance at constant pad opening size. EM lifetime tests were performed at 160 °C and 4.6×10^4 A/cm² with samples with bump heights of 65 µm and 80 µm because constant loading control is a very difficult process during flip chip bonding. Although two experimental data points are not adequate to evaluate quantitative analysis for EM, we assumed that two experimental data points clearly show EM behavior. Likewise, these experiments were carried out at a constant current density, but the applied current was equal to 2.3 A because the pad opening size was similar. As a result of the EM lifetime test, the TTF increases as the bump height decreases from 80 to 65 µm, as shown in Fig. 4a. It appears that the MTTF increases proportionally to the reciprocal bump height, as shown in Fig. 4b. The extrinsic stress conditions in the solder bump, such as the temperature, current density, actual applied current, and Joule heating effect,



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are equal in both the 80 μ m bump height and 65 μ m bump height samples; only the bump height is different. The temperature gradient in the solder bump decreases with decreasing bump height when the Joule heating effect is constant in magnitude at both 80 μ m bump height and 65 μ m bump height. The TM phenomenon in the solder bump is accelerated as the temperature gradient increases because the temperature gradient in the solder bump is the driving force for TM. Therefore, since the temperature gradient in the solder bump decreases as the bump height decreases, the effect of TM decreases with decreasing bump height. It seems that MTTF increases with decreasing bump height because the effect of TM decreases with decreasing bump height.

Figure 5 illustrates the cross-sectional microstructure of the EM-induced failure of the solder bump. Failure and local melting occur on the chip side of the solder bump due to harsh Joule heating, EM, and TM, as shown in







Fig. 4 a EM lifetime test results with bump height at constant current density, **b** MTTF(t_{50}) variations w.r.t. bump height

Fig. 5 EM induced failure morphology of a flip chip Sn-3.5Ag solder bump with a bump height and opening size of 80 μ m at 160 °C and 4.6×10⁴ A/cm²; **a** bump (a) and **b** bump (b) in Fig. 1e, respectively

Fig. 5a (bump (a) in Fig. 1e). Although the current density of bump (b), as shown in Fig. 1e, is approximately 3 times lower than that of bump (a), EM-induced failure occurs at the chip side in the solder bump irrelative to the electron flow direction. It seems that bump (b) fails at the chip side in the solder bump because Joule heatinginduced TM is more dominant than EM. These experimental results show that Joule heating is a very critical factor in the EM lifetime of the flip chip Sn-3.5Ag solder bump, and the MTTF increases with decreasing pad opening size and bump height; that is, the EM lifetimes increase with decreasing solder bump size. It seems that solder bump size change affects EM reliability, which decreases with smaller and high-performance trends of the package industry. However, these results involve very complex phenomena, including Joule heating and TM, due to the unique structure of the solder bump.

To focus the Pb-free solder EM behavior, EM tests were performed at 140 °C and $6-7.5 \times 10^4$ A/cm² using multi-SAC305 solder line samples with 100 µm, 200 µm, and 500 µm long lines.

Figure 6 shows the SEM image after the 10 h EM test at 140 °C and 6×10^4 A/cm². Sn atoms moved from the cathode side to the anode side along the direction of electron flow, and a Sn atom-depleted area at the cathode side was formed and increased as a function of stress time. The edge displacement was deduced from the depleted area at each long line, which was calculated using an image analyzer, divided by the line width.

Figure 7a shows the edge displacement as a function of stress time at each line length. The drift velocity was calculated using the relationship between the edge displacement and current stress time. From the drift velocity, the threshold current density and critical length was deduced through the EM flux equation. The EM flux equation can be expressed as [21, 32]:

$$J_{EM} = Cv = C \frac{D}{kT} Z^* e \rho j$$
⁽²⁾

where J_{EM} is the EM flux, and *C*, *v*, *D*, *Z**, *e*, *k*, ρ , and *T* are the concentration of atoms per unit volume, the drift velocity, the diffusivity, the effective charge number, the electron charge, Boltzmann's constant, the resistivity, and the absolute temperature, respectively. Equation (2) can be written as follows [34]:

$$v = \frac{D}{kT} Z^* e \rho j \tag{3}$$

The passage of a high current density drives the depletion of metal atoms at the cathode end of the line and extrusion of metal atoms at the anode end due to EM. The







Fig. 6 SEM image of the cathode side of the multi-edge drift sample after 10 h of current stressing at 140 °C and 6×10^4 A/cm²; **a** 100 µm, **b** 200 µm, and **c** 500 µm line length

EM drives atoms to the anode, and compressive stress is built up there. The vacancy concentration in the cathode becomes larger than the equilibrium vacancy concentration, and tensile stress builds up at the cathode end. The resulting stress gradient leads to back stress opposing the electron-wind force. This back stress prevents further transport of atoms to the anode end. Namely, the



Fig.7 a Edge displacements with current stress time of each line length at 6×10^4 A/cm² and 7.5×10^4 A/cm², **b** Drift velocity with applied current density where threshold current density (J_{th}) is obtained by extrapolating the fitted lines to zero drift velocity and, **c** J_{th} of each line length where J_{th} increases proportionally to the reciprocal of the line length

electron-wind force is balanced by a stress gradient that creates an equal but opposite driving force. Therefore, when the EM-induced stress is larger than the back stress, hillocks will create at the anode end, and voids will create at the cathode end. Considering both the EM-induced flux and the flux due to the stress gradient, Eq. (3) can be rewritten as [34]:

$$v = \frac{D}{kT} \left[Z^* e \rho j - \Omega \frac{\Delta \sigma}{L} \right] \tag{4}$$

where Ω , *L*, and $\Delta\sigma$ are the atomic volume, stripe length, and normal stress difference between stripe ends, respectively. Critical stress is attained when the two opposing forces are balanced. The threshold current density is therefore offered by [35]:

$$(jL)_{cr} = \frac{\Delta\sigma\Omega}{Z^*e\rho} \tag{5}$$

Equation (5) shows that the product of current density and length (jL) is the critical value associated with the critical stress of failure. The threshold current density and/or the critical length are the basic parameters of EM. Blech and Herring confirmed the presence of a "threshold current density" or "critical length" in Al interconnects. From the drift velocities at the two current densities in the multi-SnAgCu solder lines, the threshold current density was computed by extrapolation to the zero drift velocity at 140 °C, as shown in Fig. 7b. It is a widely used to calculate the threshold current density [36–38]. The threshold current density means the maximum current density that the solder line can carry without EM damage at 140 °C. Figure 7c shows that the data were a function of the inverse line length (1/L). The threshold current densities were linearly fitted to the inverse line length, as shown in Fig. 7c. This indicates that EM resistance increases with decreasing line length. This result is similar to that of EM in Pb-free solder bumps. Therefore, although the EM failure mechanism of each structure is different, the EM reliability generally increases as the size of the solder bump decreases. It seems that decreasing the flip chip solder bump size will affect EM reliability.

4 Conclusions

The size effect on EM lifetimes in flip chip Pb-free solder bumps was investigated under various structures and stress conditions. The EM lifetime increases with decreasing pad opening size and bump height. As the pad opening size changes, Joule heating is a significant factor because current-induced Joule heating decreases with decreasing pad opening size. As the bump height changes, the temperature gradient-induced TM effect is an important factor because the temperature gradient decreases with decreasing bump height. In the multi-SnAgCu edge drift sample, the current density and line length product show that the EM resistance increases with decreasing solder bump size.

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Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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