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Achieving High Carrier Mobility Exceeding 70 cm^2/Vs in Amorphous Zinc Tin Oxide Thin-Film Transistors

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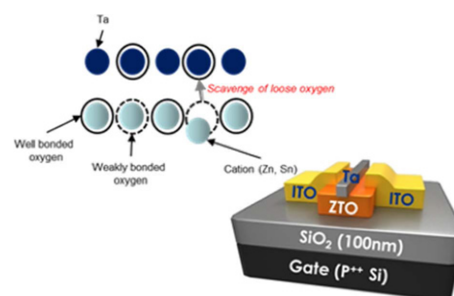
This paper proposes a new defect engineering concept for low-cost In- and Ga-free zinc tin oxide (ZTO) thin-film transistors (TFTs). This concept is comprised of capping ZTO films with tantalum (Ta) and a subsequent modest thermal annealing treatment at 200 °C. The Ta-capped ZTO TFTs exhibited a remarkably high carrier mobility of 70.8 cm^2/Vs, low subthreshold gate swing of 0.18 V/decade, threshold voltage of −1.3 V, and excellent $I_{ON/OFF}$ ratio of 2×10^8. The improvement (> two-fold) in the carrier mobility compared to the uncapped ZTO TFT can be attributed to the effective reduction of the number of adverse tailing trap states, such as hydroxyl groups or oxygen interstitial defects, which stems from the scavenging effect of the Ta capping layer on the ZTO channel layer. Furthermore, the Ta-capped ZTO TFTs showed excellent positive and negative gate bias stress stabilities.

Keywords: zinc tin oxide (ZTO), metal capping, mobility, oxygen-related defect, thin-film transistors (TFTs)



1. INTRODUCTION

Since the discovery of amorphous indium gallium zinc oxide (a-IGZO) in 2004, semiconducting metal oxide-based thin-film transistors (TFTs) have attracted tremendous attention for advanced screens such as liquid crystal (LC) displays, organic light-emitting diode (OLED) displays, and flexible displays.[1,2] The unique electronic configuration of heavy transition ions with the $(n-1)d^{10}ns^0$ orbital allows for the formation of effective percolation conducting pathways in the conduction band, even in a disordered structure, which generates a variety of intriguing properties including high mobility, low-voltage driving, low-temperature processing, and transparency to visible light. Intensive developments in the materials and processing techniques of a-IGZO TFTs have accelerated their implementation into high-end LC and OLED displays.[3-6] The carrier mobility of production-grade IGZO TFTs, however, is limited to < 20 cm^2/Vs. The carrier mobility, which is the most important metric that dictates the signal speed and current driving capability, still needs to be improved to enable a high frame rate (≥ 240 Hz), ultra-high definition (≥ 500 ppi), and integration of a scan/data driver IC onto the glass.[7] A second concern of the a-IGZO system is related to the rarity of In and Ga in the Earth's crust, which causes In- and Ga-based oxide materials to be expensive. The zinc tin oxide (ZTO) system, which is the oxide semiconductor material that is studied in this report, has recently shown a resurgence in the literature due to its abundance and low cost. In addition, the intercalation of the Sn^{4+} cation into the ZTO system can facilitate the percolation carrier conduction due to the similarity of its electron orbital to the In^{3+} cation, which leads to an enhancement in the field-effect mobility.[8] There have been many reports on the effects of thermal annealing, cation composition, and precursors for obtaining high carrier mobilities in ZTO TFTs.[9-11] Hoffman *et al.* reported a high mobility of ~30 cm^2/Vs for TFTs with a cation composition of Zn:Sn =

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50:50 using sputtering method where the thermal annealing temperature was varied from 400 to 600 °C.[9] The effect of the cation composition, which strongly affects the structural and electrical performance, was examined by co-depositing ZnO and SnO_2 targets in a sputtering system.[10] Discernible carrier mobilities with local maxima of 10 to 12 and 8 to 11 cm^2/Vs were observed for cation compositions of Zn:Sn = 25:75 and 80:20, respectively.[11] The TFTs with the ZTO channel layer using atomic layer deposition (ALD), which has the merit of a good controllability over elemental composition and thickness, were reported to exhibit the reasonable mobility of 13 cm^2/Vs.[12] Solution-processed ZTO TFTs with different chemical precursors have also been fabricated; the processing techniques used to fabricate these devices is simple and inexpensive.[13-16] The effect of Zn/Sn ratio[13] and annealing temperature[14] on the structural and chemical properties of ZTO films have been investigated in order to obtain high performance ZTO TFTs. However, the mobilities of ZTO TFTs made via these chemical routes are limited to below 10 cm^2/Vs; this poor performance is attributed to the porous channel structure with residual impurities, such as carbon, stemming from the precursor and/or solvent.

In this paper, we reported an unexpectedly high mobility for ZTO TFTs (70 cm^2/Vs), which was obtained by introducing a capping layer of tantalum (Ta) onto the ZTO channel. In particular, the improvement in the carrier mobility was achieved without compromising the $I_{ON/OFF}$ modulation ratio (> 10^8). The rationale for this superior performance was discussed based on the density-of-states (DOS) and X-ray photoelectron spectra analysis. Furthermore, the electrical stability of the Ta-capped ZTO TFTs was found to be superior to that of the uncapped ZTO TFTs.

2. EXPERIMENTAL PROCEDURE

A 100-nm-thick SiO_2 layer was grown on a heavily-doped p-type Si substrate by thermal oxidation for use as a gate insulator. A 25-nm-thick a-ZTO film was deposited by an RF magnetron sputtering system for use as a channel layer. The working pressure was 3 mtorr and the relative O_2 flow rate of $[O_2]/[Ar + O_2]$ was maintained at 0.1. The RF power was fixed to 100 W. An indium tin oxide (ITO) film was used as the source/drain (S/D) electrode layer, which was deposited by DC sputtering under an Ar atmosphere and patterned through a shadow mask. During ITO preparation, the DC power was fixed to 50 W and the working pressure was 5 mtorr. The channel width (W) and length (L) were 1000 and 300 μm, respectively. The fabricated ZTO TFTs were annealed at 500 °C for 1 h in air ambient (referred to herein as the control device, which has no metal capping layer). The ZTO TFTs had a bottom-gate and top-contact architecture, as shown in Fig. 1. A 40-nm-thick Ta film, used

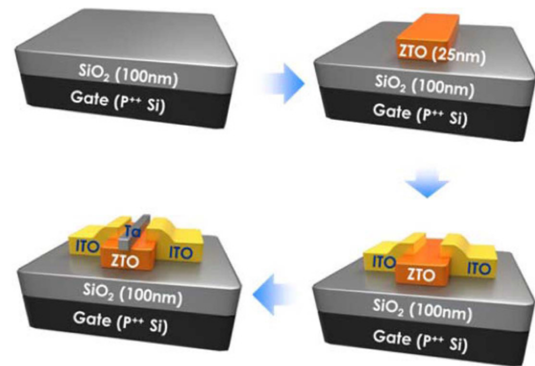

Fig. 1. Fabrication flowchart and schematic structure of Ta-capped ZTO TFTs with a bottom-gate and top-contact configuration.

as a capping layer, was selectively sputtered on the ZTO channel region through a shadow mask with dimensions of W/L = 2300/150 μm. Post-deposition annealing (PDA) was performed at 200 °C for 1 h in air. The transfer characteristics of the ZTO TFTs were measured at room temperature using a Keithley 2636 source meter. The chemical properties of the ZTO thin films were analyzed by X-ray photoelectron spectroscopy (XPS, SIGMA PROBE, ThermoG, UK).

3. RESULTS AND DISCUSSION

Figure 2 shows the transfer characteristics of the control (uncapped) and Ta-capped ZTO TFTs. The field-effect mobility (μ_{FE}) was calculated by the maximum peak value at a V_{DS} of 0.1 V. The threshold voltage (V_{TH}) was determined from the gate voltage (V_{GS}), which induces a drain current of L/W × 10 nA at a V_{DS} of 5.1 V. The subthreshold gate swing ($SS = dV_{GS}/d\log I_{DS}$ [V/decade]) was extracted from the average inverse slope (in the linear portion of the $\log I_{DS}$ vs. V_{GS} plot). The fast bulk trap density ($N_{SS,max}$) and semiconductor-insulator interfacial trap density (D_{it}) were calculated by the following equation:[17]

$$SS = \frac{qk_BT(N_{SS}t_{ch}+D_{it})}{C_i\log(e)} \quad (1)$$

where q is the electron charge, k_B is Boltzmann's constant, T is the absolute temperature, and t_{ch} is the channel layer thickness. N_{SS} and D_{it} in the ZTO TFTs were calculated by setting one of the parameters to zero. Therefore, the N_{SS} and D_{it} values must be considered the maximum trap density formed in a given system. The control ZTO TFTs exhibited promising device characteristics; the μ_{FE}, V_{TH}, SS, and $I_{ON/OFF}$ values were 30.2 cm^2/Vs, 0.30 V, 0.30 V/decade, and 2 × 10^8, respectively (Fig. 2(a) and Table 1). The relatively high mobility of the control ZTO TFTs can be attributed to the synergic effect between the efficient intercalation of the Sn^{4+} cations and the appropriate annealing conditions. A substantial improvement in the carrier mobility was observed for the

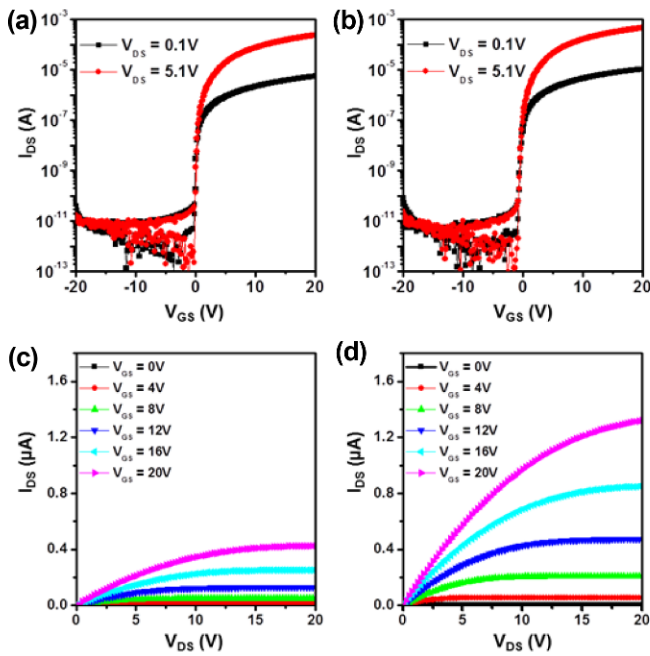

Fig. 2. Representative transfer characteristics of the (a) control and (b) Ta-capped ZTO TFTs. Corresponding output characteristics of the (c) control and (d) Ta-capped ZTO TFTs.

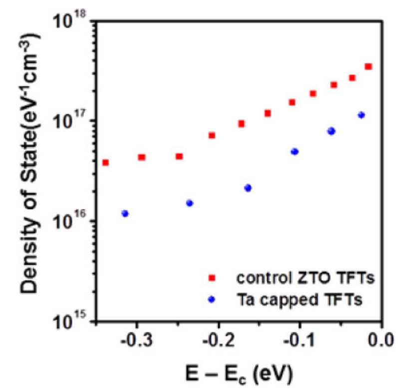

Fig. 3. Calculated DOS distributions as a function of the energy ($E - E_C$) for the control and Ta-capped ZTO TFTs.

Ta-capped ZTO TFTs; the extracted μ_{FE} value was approximately 70.8 cm^2/Vs. It is noted that extraordinarily high mobility (70 cm^2/Vs) values have been frequently reported for ZnO, In_2O_3, and IZO TFTs.[18-20]

Unfortunately, these metal oxide TFTs suffer from unacceptably large I_{OFF} values (10^{-9}-10^{-7} A); this shortcoming has been attributed to the large leakage current of the gate insulator, the high free carrier density (N_e) in the channel layer, and/or the poor definition of the channel region. Conversely, the Ta-capped ZTO TFTs still exhibited a low I_{OFF} (< 10^{-11} A) and a high $I_{ON/OFF}$ ratio (2 × 10^8). The superior transfer characteristics of this Ta-capped ZTO TFT, relative to the control device, were clearly reflected in the excellent output characteristics [Fig. 2(c) and Fig. 2(d)].

To obtain more insight about the superior performance of the Ta-capped ZTO TFTs, the density-of-states (DOS) distributions of the devices in the forbidden band gap of the ZTO semiconductor were extracted using the Meyer-Neldel rule.[21-24] The DOS distributions for both devices were calculated from the temperature-dependent drain current variations below the threshold voltage based on the thermally-activated Arrhenius model. Figure 3 shows the DOS distributions for the control and Ta-capped ZTO TFTs in the tail states regions below the conduction band (*CB*) edge. The DOS values at the *CB* edge for the control and Ta-capped devices were 3.5 × 10^{17} and 1.1 × 10^{17} $eV^{-1}cm^{-3}$, respectively. The lower distribution of the DOS for the Ta-capped ZTO TFTs is consistent with their lower *SS* value (~0.18 V/decade). The N_{SS} values for the control and Ta-capped ZTO TFTs, which were estimated from the *SS* values, were 4.4 × 10^{17} and 2.6 × 10^{17} $eV^{-1}cm^{-3}$, respectively.

The smaller DOS distributions for the Ta-capped ZTO TFTs indicate that the metal capping and subsequent

Table 1. Summary of the TFT device parameters for the control and Ta-capped ZTO TFTs.

Samples	μ_{FE} ($cm^2V^{-1}s^{-1}$)	*SS* ($Vdecade^{-1}$)	V_{TH} (V)	$I_{ON/OFF}$
Control ZTO TFTs	30.8 ± 0.7	0.30 ± 0.02	0.20 ± 0.10	2.0 × 10^8
Ta-capped ZTO TFTs	70.8 ± 0.5	0.19 ± 0.03	−1.30 ± 0.08	2.0 × 10^8

Table 2. Comparisons of device performances of ZTO TFTs reported in the literature.

Process	μ_{FE} ($cm^2V^{-1}s^{-1}$)	*SS* ($Vdecade^{-1}$)	V_{TH} (V)	$I_{ON/OFF}$	Ref.
Sputter	7.3	0.64	0.08	1.1 × 10^8	[25]
ALD	13.2	0.15	0.34	-	[26]
CVD	17.4	0.19	−0.60	-	[27]
Inkjet process	5.1	1.33	2.83	2.2 × 10^8	[15]
Spin coated	4.3	0.40	0.00	4.1 × 10^7	[13]
Sputter	70.8	0.18	−1.30	2.0 × 10^8	This work

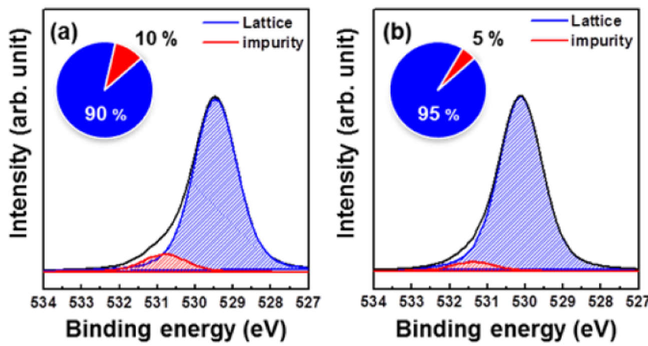

Fig. 4. O *1s* XP spectra of the (a) control ZTO film and (b) Ta-capped ZTO film on the SiO_2/Si substrates.

annealing process at 200 °C drastically reduce the density of localized tail states. According to Drude theory, the carrier mobility in the solid state is inversely proportional to the collision frequency of the charge carriers. Therefore, the effective elimination of localized scattering/trapping centers via the metal capping and annealing process can enhance the carrier mobility. It would be meaningful to compare the device parameters of Ta-capped ZTO TFTs with the other ZTO devices reported in the literature as summarized in Table 2. We note that the μ_{FE} value of 70.8 $cm^2V^{-1}s^{-1}$ in this study corresponds to the highest one.[13,15,25-27]

The chemical states of the control and Ta-capped ZTO stacks were characterized by XPS. Figures 4(a) and (b) show the O *1s* XPS spectra of the control and Ta-capped ZTO stack, respectively, which were extracted from depth profiling XPS analysis. The subpeaks at 529.5 and 530.5 eV were assigned to the oxygen bonded to fully-coordinated metal ions (metal-oxygen lattice) and hydroxyl group-related oxygen bonds, respectively.[28,29] The metal-oxygen lattice portion of the Ta-capped ZTO film increased from 90% (control ZTO film) to 95%. Conversely, the hydroxyl group-related portions were decreased from 10% (control ZTO film) to 5%. Because the hydroxyl groups are known to be acting as the tailing states,[30] this spectroscopic result suggests that the smaller DOS distribution for the Ta-capped ZTO device is partly related to the reduction of hydroxyl impurities in the ZTO film. It would be interesting to discuss how the Ta capping and subsequent annealing affect the structural and electrical properties of the semiconducting ZTO film. The thermal oxidation of Ta films on the ZTO channel layer during the PDA process distinctly affects the chemical states of the underlying ZTO film. The Gibbs free energies of formation (ΔG_f) for ZnO, SnO_2, and Ta_2O_5 are −348.1, −520.5, and −1911.2 kJ/mol, respectively, at ~200 °C.[31,32] The lowest ΔG_f for Ta_2O_5 imply that Ta atoms have stronger oxidation power compared to ZnO, SnO_2, and ZTO. Therefore, it is reasonable that the PDA of the Ta/ZTO stack at an elevated temperature (> 500 °C) will cause the oxidation of the Ta film and the simultaneous reduction of

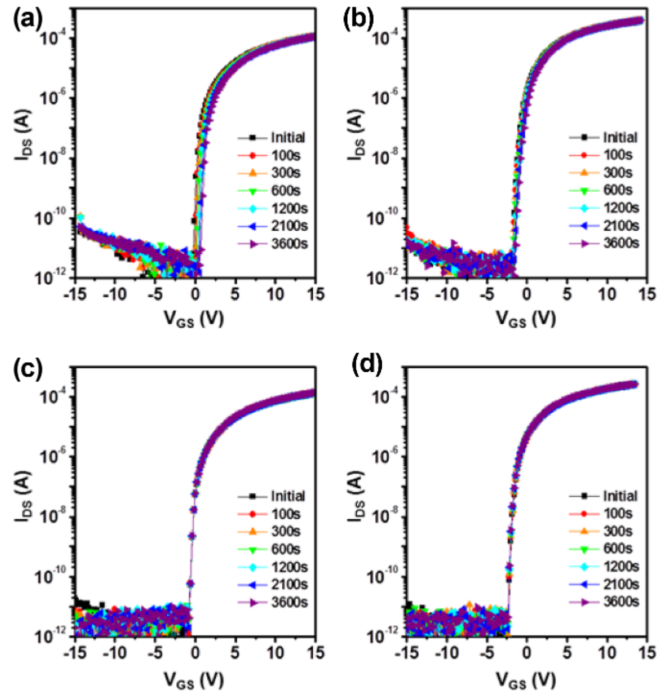

Fig. 5. Evolution of the PBS time-dependent transfer characteristics of the (a) control and (b) Ta-capped ZTO devices. Evolution of the NBS time-dependent transfer characteristics of the (c) control and (d) Ta-capped ZTO devices.

the ZTO film near the Ta/ZTO interface region, which involves the elimination of the lattice oxygens bonded to Zn and Sn cations. However, the lower PDA temperature (~200 °C) in this study will kinetically hinder the reduction reaction because breaking cation-to-oxygen bonds (Zn-to-O or Sn-to-O) requires a high activation energy. In this case, the weakly bonded oxygen species, such as interstitial oxygen and the hydroxyl groups in the ZTO film, will preferentially be eliminated and consumed during the formation of TaO_x.[33] Indeed, some loosely-bonded oxygen species were calculated to exist in the form of OH impurities in the metal oxide semiconductor.[30] This interpretation is consistent with the reduction in the impurity-related oxygen peak in the O *1s* XPS spectrum of the Ta-capped ZTO film.

Finally, the instabilities induced by the positive gate bias stress (PBS) and negative gate bias stress (NBS) in the control and Ta-capped ZTO TFTs were compared. To exclude adverse ambient effects, such as oxygen gas or moisture adsorption/desorption, on the PBS and NBS instabilities of the ZTO TFTs, a 13-nm-thick Al_2O_3 film was deposited as a passivation layer on the control and Ta-capped ZTO TFTs. This was done via an atomic layer deposition (ALD) method.[34] The ALD-derived Al_2O_3 film was selected because it possesses good conformity and excellent diffusion barrier properties against oxygen gas and moisture. Figures 5(a) and (b) show the variations in the transfer curves for the

control and Ta-capped ZTO TFTs as a function of the PBS time, respectively. The devices were stressed under the following conditions: a V_{GS} value of +20 V was applied and the V_{DS} *was* fixed to 5.1 V for 3,600 s at room temperature. The control device suffered from a positive V_{TH} shift of ~0.89 V during the application of a PBS. In contrast, the TC ZTO TFTs exhibited a smaller V_{TH} shift of ~0.40 V under identical PBS conditions. The better PBS stability of the Ta-capped ZTO TFT can be explained by the lower trap distributions below the *CB* edge. When a PBS is applied to the gate electrode, the quasi-Fermi energy level is elevated toward the *CB* edge as a result of downward band banding. The trapping event of the accumulated electron carriers in the channel region under PBS conditions will be proportional to the available DOS below the *CB* edge.[35] Therefore, the improvement in the PBS stability of the Ta-capped ZTO device is attributed to the effective reduction in the tailing trap states distributions, which is caused by the capping-related defect elimination. The NBS-induced instabilities for the control and Ta-capped ZTO devices are also shown in Figs. 5(c) and (d), respectively. In the case of a NBS, the V_{GS} stress value was changed to −20 V, whereas the V_{DS} and duration times were identical to the PBS conditions. Both devices exhibited very stable behavior in terms of the V_{TH} shift, as shown in Figs. 5(c) and 5(d), respectively.

4. CONCLUSIONS

In summary, a new defect engineering process consisting of a capping Ta film and subsequent annealing treatment was proposed in an In- and Ga-free ZTO system. Compared to the uncapped ZTO TFTs, the Ta-capped ZTO TFTs exhibited a remarkable carrier mobility of 70.8 cm^2/Vs and a low *SS* value of 0.18 V/decade (at 200 °C). Additionally, comparable V_{TH} and $I_{ON/OFF}$ ratio were maintained. The two-fold increase in the carrier mobility for the Ta-capped ZTO TFTs can be attributed to the effective reduction of the unwanted tailing trap states, such as hydroxyl groups or oxygen interstitial defects, which comes from the scavenging effect of the capping Ta layer on the ZTO channel layer. Moreover, the fabricated Ta-capped ZTO TFTs showed better PBS stability than the control ZTO TFTs as well as excellent NBS stability. Therefore, this method may be useful for metal oxide TFTs in next-generation active-matrix displays where extremely high mobility is required.

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