Fabrication and Shear Strength Analysis of Sn-3.5Ag/Cu-Filled TSV for 3D Microelectronic Packaging

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In this study, lead free Sn-3.5Ag solder bumps have been deposited on Cu-filled through-silicon via (TSV) by electroplating method. The solder bumps are plated using an acidic solution composed of SnSO₄, H₂SO₄, Ag₂SO₄, thiourea and an additive. The current density is varied from -30 to -60 mA/cm² to obtain the eutectic Sn-3.5Ag solder. The copper is electroplated in TSV using an acidic solution of CuSO₄·5H₂O, H₂SO₄, HCl, and an inhibitor. The bottom-up Cufilling in TSV is achieved by a 3-step pulse periodic reverse (PPR) electroplating. It has been observed that the eutectic Sn-3.5Ag solder is achieved at a current density of -55 mA/cm^2 . The solder bumps are further reflowed onto TSV at 260 °C for 20 seconds, and shear strength of the formed Sn-3.5Ag/Cu-filled TSV joint is investigated. The results indicate the formation of Cu₆Sn₅ and Ag₃Sn intermetallic compounds (IMCs) at the joint interface. It is found that with an increase of shear speed from 0.5-10 mm/s, the shear stress initially increases to a maximum, and then decreases beyond shear speed of 10 mm/s through 500 mm/s. It is shown that the ductile fracture mode gradually decreases beyond shear speed of 10 mm/s and disappears completely at 500 mm/s.

Keywords: through-Si-via (TSV), electroplating, electrolyte, microstructure, solder, reflow



1. INTRODUCTION

Nowadays, high speed, superior performance, light weight, portable, and low power requirements of electronic goods are being extensively investigated in microelectronic packaging devices. The microelectronic industries are continuously looking into and satisfying these demands for the luxurious life of a common man through miniaturization and compact multi-dimensional packaging.^[1,2] The advanced 3D packaging technology where chips are stacked over one another in a minute space has attractive benefits, such as reduction in volume by manifolds compared to the two dimensional (2D)

packaging technology.^[3,4] As a consequence, a drastic reduction in energy consumption is achieved due to a shorter interconnecting path, such as for TSV 3D packaging technology.^[1,5]

In TSV technology, interconnections among stacked Si chips are directly established through conducting vertical columns of copper metal. This technology has various other excellent features like noise free signal processing, high speed, light weight, portable and low power consumption. Silicon chips are stacked together by creating a minute hole through Si called via which is further filled in with copper conductor.^[5] Copper plating has been employed frequently as via filling material in TSVs before solder bumping and final device interconnection.^[6,7] However, the process of traditional electroplating is rather time consuming for obtaining

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a void free copper TSV filing. Studies are being performed to reduce the copper filling times, and to minimize the voids in the Cu-filled TSVs.^[10,11] Several researchers have adopted variations in the electroplating process by modifying the current waveforms, electrolyte components, bath parameters and conditions.^[8,9] The variations of current waveforms in copper electrodeposition processes such as those in pulse reverse current (PR) and periodical pulse-reverse (PPR) current plating methods are most promising compared to direct current electrodeposition.^[10,12-14]

There are enormous amount of research efforts devoted to either defectless filling of the TSV or the extrusion properties of the TSVs using filling materials like Cu-Ni, Cu-W, Cu-CNT etc..^[15-18] However, there exists a limited number of investigations on solder bumping and joint strength analysis of Sn-3.5Ag solder on TSVs. Recently, Jung et al. have examined the joint performance of the low alpha solder (Sn-1 wt%Ag-0.5 wt%Cu bumped on Cu-filled TSV by reflow process.^[19,20] However, the Sn-Ag-Cu alloy may form additional Cu₆Sn₅ intermetallics at the solder/Cu joint leading to more cracks and voids.^[21-23] Therefore, in this study, it is an object to develop a cost effective Sn-3.5Ag solder by electrodeposition process, followed by bumping of the Sn-3.5Ag solder over the Cu-filled TSV. The Cufilling of TSV has been achieved by electroplating process with PPR waveform. The reliability of Sn-3.5Ag solder/Cu filled TSV joint has been investigated using shear strength test and the failure mechanisms of the Sn-3.5Ag solder/Cufilled TSV joint have been discussed.

2. EXPERIMENTAL PROCEDURE

2.1 Via formation

A silicon wafer (*p*-type Si; 4 inch in diameter and 525 μ m in thickness) is selected as the substrate. A photo resist (model: AZ4620) is spin coated onto the Si wafer surface to generate multiple hole patterns. The via formation is accomplished by Deep Reactive Ion Etching (DRIE) process as shown in Fig. 1(a). The deep reactive etching of silicon involves reaction of Si with SF₆ plasma followed by passivation using C₄F₈, for a fixed number of cycles as shown in the Fig. 1(a). The etching reactions in each step are given below:^[24,25]

Etching term (1):

SF₆: SF₆ +
$$e^-$$
 (from plasma) \rightarrow SF₅⁺ + F + 2 e^-

 \Rightarrow Si (solid) + 4F (gas) \rightarrow SiF₄ (gas)

O₂: Residual polymer (passivation) etching, Si surface cleaning

Passivation term (2):

 $C_4F_8: C4F_8 + e^-$ (from plasma) $\rightarrow C_3F_6 + CF_2 + e^-$

 \Rightarrow nCF₂ \rightarrow (CF₂)_n (Teflon like polymer on Si surface)

In this way several vias are created with 60 µm diameter



Fig. 1. (a) DRIE Process and (b) typical via dimensions formed.

and 120 μ m depth in Si wafers. After the vias are formed, the remaining photoresist is removed by using a solution of concentrated sulfuric acid (H₂SO₄) and hydrogen peroxide (H₂O₂) in 3:1 ratio. Further metallization such as SiO₂ as the dielectric layer deposited by high-density plasma chemical vapor deposition (HDPCVD), and Ti as an adhesion layer are coated on the inside walls of the vias. The conducting seed layer Au is deposited by magnetron sputtering over the SiO₂ dielectric layer, respectively demonstrated in Fig. 1(b).

2.2 Chip formation and plating electrodes

After metallization, the Si wafer is sliced into various chips (dimension: $5 \times 5 \text{ mm}^2$) by a diamond saw. The sliced Si chips are used as the cathode substrates for Cu deposition. A Pt sheet ($10 \times 10 \times 0.3 \text{ mm}^3$) is chosen as anode. The electroplating is performed using a commercial pulse-plating unit (EPP-4000, Princeton Applied Research). The electrochemical cell is made of three electrodes, the third electrode being the saturated calomel electrode (SCE) as a standard reference electrode.

2.3 Electrolytic baths and plating experiment

Electrolyte of copper plating bath consists of the CuSO₄· 5H₂O, H₂SO₄, HCl, and an inhibitor. The inhibitor has been chosen from the Ref.^[15] The pH of the electrolyte is \approx 1.0 and the temperature of electrolyte is kept around \approx 24-26 °C. The electrochemical assembly is shown in Fig. 2(a) and the pulse waveform used for the Cu filling is PPR with repeating 3 steps, as shown in Fig. 2(b). In PPR plating, the deposition takes place during negative current cycle, while the dissolution



Fig. 2. (a) Electroplating assembly and (b) PPR waveform.

or the protrusions and dendritic feature is prominent in positive current cycle.^[15] The current pulse in 3-step PPR is given below:

 1^{st} step: -4 mA * 20 s + 4 mA * 1 s + 0 mA * 8 s 2^{nd} step: -6 mA * 20 s + 4 mA * 1 s + 0 mA * 15 s 3^{rd} step: -16 mA * 20 s + 4 mA * 1 s + 0 mA * 15 s

The negative sign indicates the reverse plating current while the positive sign indicates the forward plating current. Total plating time for one complete cycle is around 80 minutes. The Cu-filling efficiency is calculated by the Image-Pro Plus 6.0 program, and given by the equation:

 $\left(\frac{\text{Height of the Cu filled in via}}{\text{Area of the Cu filled in via}}\right) \times 100\%$

The plating bath used for the Sn-3.5Ag solder deposition consist of SnSO₄, Ag₂SO₄, Thiourea and an additive. Thiourea acts as a complexing agent for Sn and Ag alloy deposition.^[26] The pH of the Sn-Ag electrolyte is 2.3 and the temperature of electrolyte is kept around \approx 24-26 °C. The eutectic composition of Sn-Ag plating is determined by varying the

Table 1. Bath compositions and parameters for Sn-Ag plating.

Component	Values
$SnSO_4$	42.8 g/L
Ag_2SO_4	0.08 g/L
H_2SO_4	26.8 mL/L
Thiourea	15.2 g/L
Additive	3 g/L
Current density	$-40-60 \text{ mA/cm}^2$
Inter-electrode distance	30 mm
Plating time	15-60 min
Bath stirring	200 rpm (magnetic)
Temperature	24-26 °C
pH	2.3

Table 2. Bath compositions and parameters for Cu electro-filling.

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Component	Values
$CuSO_4 \cdot 5H_2O$	200-210 g/L
H_2SO_4	200-210 g/L
HCl	10-20 mL/L
Inhibitor	1 mL/L
Inter-electrode distance	30 mm
Plating time	80 min
Bath stirring	200 rpm (magnetic)
Temperature	24-26 °C
Anodic current density	4 mA/cm^2
Cathodic current density	-16 mA/cm^2
pH	1.0

current density from -30 to -60 mA/cm². The polarization measurements are done at a scan rate of 1 mV/s. To obtain uniform bumps, the solder bump height and width are measured as a function of plating time. Table 1 and 2 show the corresponding plating bath compositions and parameters for both Sn-Ag and Cu plating.

2.4 Solder bumping

After the Cu filling of the TSV, the solder bumps are plated to a sufficient size and thickness followed by reflowing them onto the Cu-filled TSVs. Prior to reflow, the bumps are coated with a thin layer of Rosin mildly activated (RMA) flux. Next, the solder bumps are preheated from 150 to 180 °C for 160 s and held at a peak temperature of 260 °C for 20 s. The schematic diagram for the experimental set up and the reflow profile used are illustrated in Fig. 3(a-b).

2.5 Shear strength test

Shear strength test on the Sn-3.5Ag/Cu-filled TSV interface is conducted with a Dage 4000-HS tester. The schematic diagram for the shear test is shown in Fig. 4. The effect of shearing speed is studied from 0.50 mm/s to 500 mm/s at a tip height of 3.0 μ m according to JESD 22-B117 standard. The each shear test is repeated 20 times for better accuracy and average shear stress is calculated, and the effect of shear stress on the joint microstructures is studied.





Fig. 3. (a) Reflow process and (b) corresponding reflow profile.



Fig. 4. (a) shear strength tester, (b) solder ball arrangement for the shear test.

3. RESULTS AND DISCUSSION

3.1 Cu-plating process

3.1.1 Effect of plating time on microstructure of Cu deposits

The effect of plating time on the as deposited microstructures of Cu filled TSVs is shown in Fig. 5. It is noticed that the plating rate is around ~7.4 μ m at 30 minutes, and increases to 12.5 μ m after 60 minutes. The thickness of the plating again increases rapidly beyond 60 minutes approaching 28.24 μ m which is nearly close to the diameter of the via (~30 μ m). The thickness of the plating continues to increase up to 72.29 μ m after 120 minutes of plating. The thickness increase with plating time is linear in nature and may be ascribed due to the increase in deposition rate with plating time.^[27-30] This observation suggests that the copper filling time needed for the TSV filling may lie in the range of the 90 to 120 minutes.

3.1.2 Effect of plating time on filling tendency of TSVs

The effect of plating time is investigated at a constant peak current density -16 mA/cm^2 and anodic current density of 4 mA/cm^2 . Figure 6 shows the cross-sectional SEM image of the Cu-filled TSVs at various filling times of 30, 60, 90 and 120 minutes respectively. It can be observed that initially the rate of deposition is slower at the 30 minutes. Further increase in filling time improves the filling volume in the TSV. A bottom-up filling tendency is achieved around the filling times of 90 and 120 minutes, respectively (Fig. 6(a) and (b)). Generally, a bottom-up filling is required for a void free and defect less filling of TSVs. For a bottom-up filling, the deposition rate and current density should be adjusted in such a way that the suppression of metal ions at the via



Fig. 5. The thickness of copper plantings at different plating times (a) 30 minutes, (b) 60 minutes, (c) 90 minutes, and (d) 120 minutes.



Fig. 6. Cu-filling tendency at different plating times (a) 30 minutes, (b) 60 minutes, (c) 90 minutes, and (d) 120 minutes.

corners dominates the continuous deposition at the bottom.^[8,31,32] The V-shape filling depicts a bottom up tendency and indicates a void free filling as shown in Fig. 6(c). In this work, the competition between suppressor and accelerator is achieved using hydrochloric acid and an inhibitor. A further increase in time to 120 minutes caused a rapid growth rate around the via opening as well as on the outer walls of the via and an overflow of copper plating is noticed (Fig. 6(d)). Therefore, a filling time of 90 minutes is confirmed for the high speed bottom-up filling of Cu inside TSVs.

3.2 Sn-3.5Ag plating process

3.2.1 Polarization studies

Figure 7(a) shows the change in Ag content in the deposits as a function of current density. The Ag content is confirmed from the EDS compositional analysis of the developed coatings at the various current densities. To achieve a eutectic composition of Sn-Ag alloy, the current density is varied from -30 mA/cm^2 to -60 mA/cm^2 . It is observed that the silver content is very high in the deposit at low current density, i.e., 15.72 wt% at -30 mA/cm². An increase in current density further decreases the silver content continuously. The eutectic composition is achieved at a current density of -55 mA/cm^2 . The composition of silver falls beyond -55 mA/cm^2 due to an increase in Sn nuclei with increasing current.^[33] The breakdown potential of Sn-Ag deposition lies in the range of -0.46 to -0.34 V as shown in Fig. 7(b). It is observed that the anodic current flows at -0.34 V to 0, which causes the dissolution at the cathode. The anodic dissolution of Sn-Ag follows in the cathodic region from -0.34 to -0.46. Further, the region from -0.46 to -0.8 consists of only Sn



Fig. 7. (a) Weight percent of Ag as a function of current density, and (b) Polarization curve obtained in Sn-Ag electrolyte.



Fig. 8. The bump surface morphology at the top of Cu-filled TSVs as a function of plating duration.



Fig. 9. Effect of plating time on bump width and height.

deposition. Similar behavior has been reported by Sharma et. al. working on Sn-Ag plating.^[26]

3.2.2 Bump surface morphologies

In order to have a uniform size and shape of the solder bumps, various solder bumps are plated over Cu-filled TSVs with different plating times (Fig. 8). It is observed that the spherical size of the bumps increases in proportion with increasing time (from 20 to 60 minutes). The bump width increases continuously and is slightly non-uniform beyond 40 minutes. It is already discussed that the effect of plating time is always to increase the deposition rate.^[27] A sufficient bump width ~46 µm is obtained after 40 minutes of plating duration. To examine the effect of plating time on bump morphology quantitatively, the bump width and heights are measured with Image J software module and are plotted as a function of different plating times (Fig. 9). It is observed that the bump width increases from 25 to 46 µm continuously with an increase in time from 20 to 40 minutes. Similarly, the bump height also increases from 18 to 35 µm with an increase in plating time from 20 minutes to 40 minutes. This may be due to the increase in growth rate of the depositing metal ions with increased plating times. However, the rate of increase in height and width becomes slower after a duration of 40 minutes. The morphology turns slightly irregular and pointed at 60 minutes of plating (Fig. 8). This type of slight deviation in regular morphology of plated coatings has been ascribed to the concentration polarization of the cathode at higher plating durations.^[27] Therefore, a plating time of 40 minutes is suggested for the plating of uniform and regular sized bumps over the Cu-filled TSVs.

3.3 Plated Sn-Ag solder bumping on TSVs

The plated Sn-3.5Ag Ag bumps over the different TSVs are shown in Fig. 10(a). A typical Sn-Ag bump formed on the single via is shown in Fig. 10(b). The change in shape and size to perfect sphere is noticed after the reflowing of the solders bumps onto TSVs as shown in Fig. 10(c). The change in shapes can be related to the inward surface tension of the molten solder bump. It is shown that the plated and reflowed solder ball is a typical spherical shape in nature with a dimension of ~35 × 46 μ m (Fig. 10(d)). The cross-sectional SEM micrograph of the via top with reflowed



Fig. 10. Electroplated bumps (a) top surface morphology of Sn-Ag bumps on a Si wafer, (b) a single plated Sn-Ag bump over a TSV, (c) top surface morphology of Sn-Ag bumps reflowed on a Si wafer, (d) a single reflowed bump overs a TSV with dimensions, (e) a cross section of the Sn-Ag plated and reflowed bump on a TSV, (f-h) the Ag, Cu, and Sn elemental maps of (e) (IMC thickness $2.8 \mu m$).

Sn-3.5Ag solder bump is shown in Fig. 10(e). The interface examination as shown in Fig. 10(f-h) shows the formation of Ag₃Sn and Cu₆Sn₅ at the joint as detected by the EPMA analysis. This confirms that an excellent metallurgical bonding is established at the Sn-3.5Ag solder/Cu interface.

3.4 Shear strength test

The shear strength test results of the Sn-3.5Ag solder/Cufilled TSV joint is shown in Fig. 11. The shear speed is varied from 0.5 mm/s to 500 mm/s. The fractured surfaces after shear tests at 10 mm/s, 200 mm/s and 500 mm/s are also shown in the insets for comparison. It is observed that with an increase in shear speed from 0.5 to 10 mm/s, the shear stress increases initially from 75 to 110 MPa. As shown in Fig. 11, up to a shear speed of 10 mm/s, the fracture morphology is almost ductile showing big dimples at the joint. Further increase in shear speeds from 10 to 500 mm/s results in a decrease of the shear stress gradually from 110 to 50 MPa. The corresponding fracture morphology at a shear speed of 200 mm/s shows a mixed ductile and brittle type of failure. The number of dimples are lesser in this case as compared to that of 10 mm/s speed. The mixed failure is confirmed by the EPMA elemental maps showing the brittle and ductile regions shown by a big arrow (Fig. 11). The presence of Sn in the EPMA shows the ductile dimples whereas the presence of Cu shows the broken brittle fractured Cu₆Sn₅ IMC. Further, at a sufficiently higher speed of 500 mm/s, the fracture surface morphology changes to completely brittle, i.e. the fractured surface appears smooth without any shear dimples. At low shear speeds, the strengthening of the Sn-3.5Ag solder/Cu interface is due to an increase in dislocation density. The dislocations in the solder ball are tangled more frequently due to the inherent



Fig. 11. The shear stress at the Cu/Sn-3.5Ag solder interface as a function of shear speed.

shear stresses developed.^[34] The shear strength is closely related to the strain rate equation: $^{[35]}$

$$\tau = C(\dot{\varepsilon})^n$$

where, τ is the shear stress, and $\dot{\varepsilon} = d\varepsilon/dt$ is the strain rate, and *n* is the strain rate sensitivity, *C* is a constant. Here, *n* < 0.1 at room temperature. The value of *n* increases beyond a homologous temperature of 0.5. When the shear speed is lower (< 10 mm/s), the shear stress increases continuously with increased shearing. This is due to the increase in work hardening rate caused by an increased dislocation density.^[34,35] However, beyond the shear strength of 10 mm/s, a gradual decrease in shear stress is noticed. The localized deformation in bulk solder caused by the uneven surface of the IMCs is minimized and brittle fracture increases. This decrease in shear stress can be ascribed to the fact that the shear deformation occurs very fast at the joint and fractures eventually due to increase in tendency of brittle fracture.^[20,35-38]

4. CONCLUSIONS

In this study, the formation of Sn-3.5 Ag solder bumps on Cu filled TSV by copper electroplating has been investigated using a periodic pulse reverse (PPR) current waveform. The eutectic composition of Sn-Ag solder is obtained at -55 mA/ cm^2 . It was also found that the thickness of copper layer increases linearly with plating time. The optimum conditions for the 100% filling efficiency was obtained at a cathodic current density of -16 mA/cm^2 , and a plating duration of 90 minutes. The bumped Sn-3.5Ag/Cu solder joint microstructures further confirm a good metallurgical bonding free of any voids and cracks after reflow process. The shear strength test results show that shear strength rises up to shear speeds of ~10 mm/s and falls gradually thereafter with increasing shear speeds. It is also observed that the tendency of brittle fracture increases with the increasing shear speed from 10 to 500 mm/s.

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REFERENCES

- K. Takahashi, M. Umemoto, N. Tanaka, K. Tanida, Y. Nemoto, Y. Tomita, M. Tage, and M. Bonkohara, *Microelectron. Reliab.* 43, 1267 (2003).
- 2. T. C. Tsai, W. C. Tsao, W. Lin, C. L. Hsu, C. L. Lin, C. M. Hsu, J. F. Lin, C. C. Huang, and J. Y. Wu, *Microelectron*. *Eng.* 92, 29 (2012).
- 3. J. V. Olmen, C. Huyghebaert, J. Coenen, J. V. Aelst, E.

Sleeckx, A. V. Ammel, S. Armini, G. Katti, J. Vaes, W. Dehaene, E. Beyne, and Y. Travaly, *Microelectron. Eng.* **88**, 745 (2011).

- 4. M. H. Roh, S. Y. Park, W. J. Kim, and J. P. Jung, *JWJ* 29, 295 (2011).
- R. Hon, S. W. R. Lee, S. Zhang, and C. K. Wong, *Proc. IEEE 2005 Electronics Packaging Technology Conference*, p. 384, IEEE, Singapore (2005).
- M.-H. Roh, H.-Y. Lee, W. J. Kim, and J. P. Jung, *Korean J. Met. Mater.* 49, 411 (2011).
- M. Tomisaka, M. Hoshino, H. Yonemura, and K. Takahashi, *DENSO Technol. Rev.* 6, 78 (2001).
- 8. T. H. Tsai and J. H. Huang, *Microelectron. Eng.* **88**, 195 (2011).
- Z. Patterson, C. Weber, R. Balachandran, R. Gouk, S. Verhaverbeke, and M. Keswani, *ECS Electrochem. Lett.* 3, D41 (2014).
- S. C. Hong, W. G. Lee, J. K. Park, W. J. Kim, and J. P. Jung, JWJ 29, 9 (2011).
- 11. S. J. Hong, S. C. Hong, W. J. Kim, and J. P. Jung, *J. Micro-electron. Packag. Soc.* **17**, 79 (2010).
- 12. J. Y. Lin, C. C. Wan, Y. Y. Wang, and H. P. Feng, *J. Electrochem. Soc.* **154**, D139 (2007).
- J. S. Bae, G. H. Chang, and J. H. Lee, J. Microelectron. Packag. Soc. 12, 129 (2005).
- L. Hofmann, R. Ecke, S. E. Schulz, and T. Gessner, *Micro-electron. Eng.* 88, 705 (2011).
- M. H. Roh, A. Sharma, J. H. Lee, and J. P. Jung, *Metall. Mater. Trans. A* 46A, 2051 (2015).
- S. C. Hong, S. Kumar, D. H. Jung, W. J. Kim, and J. P. Jung, *Met. Mater. Int.* 19, 123 (2013).
- L. P. Zhou, M. P. Wang, K. Peng, J. J. Zhu, Z. Fu, and Z. Li, *T. Nonferr. Metal. Soc.* 22, 2700 (2012).
- T. Wang, K. Jeppson, L. Ye, and J. Liu, *Small* 7, 2313 (2011).
- D. H. Jung, S. Kumar, and J. P. Jung, J. Microelectron. Packag. Soc. 22, 7 (2015).
- D. H. Jung, S. Agarwal, S. Kumar, and J. P. Jung, *JMEP* 12, 161 (2015).

- 21. L. M. Lee and A. A. Mohamad, *Adv. Mater. Sci. Eng.* **2013**, 1 (2013).
- 22. A. D. E. Xu, J. Chow, M. Mayer, H.-R. Sohn, and J. P. Jung, *Electron. Mater. Lett.* **11**, 1072 (2015).
- 23. H. Y. Lee, A. Sharma, S.-H. Kee, Y. W. Lee, J. T. Moon, and J. P. Jung, *Electron. Mater. Lett.* **10**, 997 (2014).
- 24. I. U. Abhulimen, A. Kamto, Y. Liu, S. L. Burkett, and L. Schaper, J. Vac. Sci. Technol. B 26, 1834 (2008).
- 25. K.-S. Kim, Y.-C. Lee, J.-H. Ahn, J. Y. Song, C. D. Yoo, and S.-B. Jung, *Korean J. Met. Mater.* 48, 1028 (2010).
- A. Sharma, S. Bhattacharya, S. Das, and K. Das, *Metall. Mater. Trans. A*, 44A, 5587 (2013).
- A. Sharma, S. Bhattacharya, S. Das, and K. Das, *Metall. Mater. Trans. A*, **45A**, 4610 (2014).
- 28. A. Sharma, Y. J. Jang, and J. P. Jung, *Surf. Eng.* **31**, 458 (2015).
- A. Sharma, S. Bhattacharya, R. Sen, B. S. B. Reddy, H.-J. Fecht, K. Das, and S. Das, *Mater. Charact.* 68, 22 (2012).
- A. Sharma, S. Bhattacharya, S. Das, and K. Das, *Appl. Surf. Sci.* 290, 373 (2014).
- 31. S. C. Hong, W. G. Lee, W. J. Kim, J. H. Kim, and J. P. Jung, *Microelectron. Reliab.* **51**, 2228 (2011).
- C. Okoro, R. Labie, K. Vanstreels, A. Franquet, M. Gonzalez, B. Vandevelde, E. Beyne, D. Vandepitte, and B. Verlinden, *J. Mater. Sci.* 46, 3868 (2011).
- 33. H.-Y. Chen, C. Chen, P.-W. Wu, J.-M. Shieh, S.-S. Cheng, and K. Hansen, J. Electron. Mater. 37, 224 (2008).
- 34. C. R. Siviour, D. M. Williamson, S. J. P. Palmer, S. M. Walley, W. G. Proud, and J. E. Field, *J. Phys. IV* **110**, 477 (2003).
- 35. S. Kumar, D. H. Jung, and J. P. Jung, *IEEE Trans. Comp. Packag. Manuf. Tech. Part A* **3**, 441 (2013).
- 36. A. Tong and Q. Fei, Microelectron. Reliab. 54, 932 (2014).
- D.-S. Liu, C.-Y. Kuo, C.-L. Hsu, G.-S. Shen, Y.-R. Chen, and K.-C. Lo, *Mater. Sci. Eng. A* 494, 196 (2008).
- 38. S.-J. Jeon, S. Hyun, H.-J. Lee, J.-W. Kim, S.-S. Ha, J.-W. Yoon, S.-B. Jung, and H.-J. Lee, *Microelectron. Eng.* 85, 1967 (2008).