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Sn-Ag-Cu to Cu Joint Current Aging Test and Evolution of Resistance and Microstructure

Di Erick Xu,[1] Jasper Chow,[1] Michael Mayer,[1] Jae Pil Jung,[2,*] and Jong Hyun Yoon[3]

[1]Microjoining Laboratory, Centre for Advanced Materials Joining, Department of Mechanical and Mechatronics Engineering, University of Waterloo, Waterloo ON N2L3G1, Canada
[2]Microjoining and Semiconductor Packaging Lab, Department of Materials Science and Engineering, University of Seoul, 90 JunNong-dong, DongDaeMun-gu, Seoul 130-743, Korea
[3]KDone Co. Ltd., 19-5, Baeksukpo-Ri, Asan, Chungcheongnam-Do, 336-821, Korea

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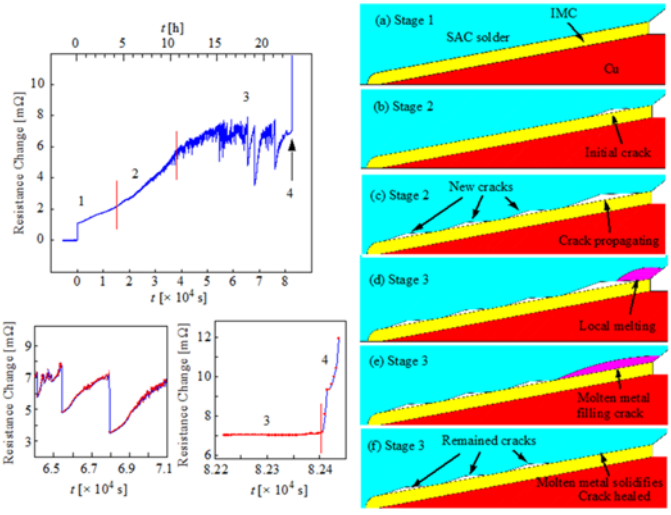
SAC 305 solder bump with 800 μm diameter were produced and soldered to a custom substrate with Cu lines as leads that allow for resistance measurement during current aging. The measured joint resistance values (leads plus solder bump) before aging are 7.7 ± 1.8 mΩ and 11.8 ± 2.8 mΩ at room temperature and 160°C, respectively. In general, the resistance of the solder joint increases instantly by about 1 mΩ, when subjected to a 2.2 A aging current at 160°C. The increase is gradual in the following hours of aging and more drastic as it approaches the final failure. Four stages are identified in the resistance signal curve and compared with observations from cross sections. The stages are IMC growth, crack formation and propagation, intermittent crack healing-forming, and final failure resulting in an open connection at the cathode. Recently a periodical drop and rise behavior was reported for the resistance signal. This behavior is reproduced and attributed to the intermittent crack healing-forming stage. The healing events observed are faster than the sampling time. Possibly, as current is concentrated when bypassing interfacial cracks, local melting occurs partially filling cracks before resolidifying.

Keywords: Sn-Ag-Cu solder, electromigration, four wire method, electrical current aging, in situ monitoring



1. INTRODUCTION

Sn-Ag-Cu (SAC)[1] is widely used in the field of micro electronics as a substitute of Pb based solder, due to the environmental concern associated with Pb. Whether in chip-scale joining such as flip-chip[2] or in package scale joining such as surface mount technology,[3] the solder joint is required to be reliable, especially in harsh applications such as in aerospace.

Avoiding electromigration is more challenging with advancing miniaturization of microelectronics connections. The same current results in higher current density in a thinner connection, thus increases the electromigration rate. For example, the peak current density in a flip-chip joint was found to be twelve times higher than the average current density.[4] Moreover, miniaturization can also cause poor heat dissipation, and an increment in temperature also

*Corresponding author: jpjung@uos.ac.kr

accelerates electromigration.

Research has been reported on electromigration of solder joints. Particles or nanoindentations were used as markers to study electromigration rate of solder joints, and eutectic SnPb is found to have faster electromigration rate than SAC.[5,6] Electromigration can also result in protruding of grains due to the stress caused by massive migration of atoms, and this phenomenon was also used to study solder joint electromigration.[6,7] In some soldering alloy systems such as Sn-Pb, where different elements have obviously different electromigration rate, element distinguishable method such as scanning electronic microscopy (SEM) with back scattered electron signals can be used to study the joint electromigration.[8,9] However this phenomenon is not seen in SAC solder alloy and therefore this method is not adopted in this study. Other microstructural observations including cracks, voids, and intermetallic compounds (IMCs) have been discussed in [10].

Non-destructive signals from solder connections during electromigration testing are used to obtain more data and understand the aging mechanism better. For example, joint resistance is measured non-destructively during current aging test.[11,12] Joint resistance is essential for the performances of microelectronics devices. Chang *et al.*[11] have demonstrated that four wire method is very sensitive to void formation and propagation at solder joint interface, and can be adopted in studies of current aging test systematically. Lin *et al.*[12] explained the behavior of the resistance aging curve being either concave down or up, depending on whether the IMC growth or crack formation is dominant, respectively, and on the direction of IMC growth.

In this study, we apply a combination of destructive and non-destructive measurements and finite element simulation to improve the knowledge of mechanisms causing solder joint aging. For this, the resistance of SAC solder bumps joined to Cu lines is measured using a four wire method during high current aging in elevated temperature, cross-sections are made of samples aged for various time periods, and finite element (FE) models are developed to simulate various degrees of joint degradation.

2. EXPERIMENTAL PROCEDURE

The SAC solder has a composition of 3 ± 0.2 wt. % Ag and 0.5 ± 0.2 wt. % Cu (SAC 305). Several 0.79 mm long sections are cut from the solder wire, placed on custom designed test substrates, and heated inside an oven with a heating rate of 20°C/min. After 2 min reflow at 240 - 250°C, the oven is turned off and the door opened until the samples cool down to room temperature. The top views and cross-sections of a typical solder joint before and after reflow are shown in Fig. 1(a)-(d), respectively. Figure 1(d) shows

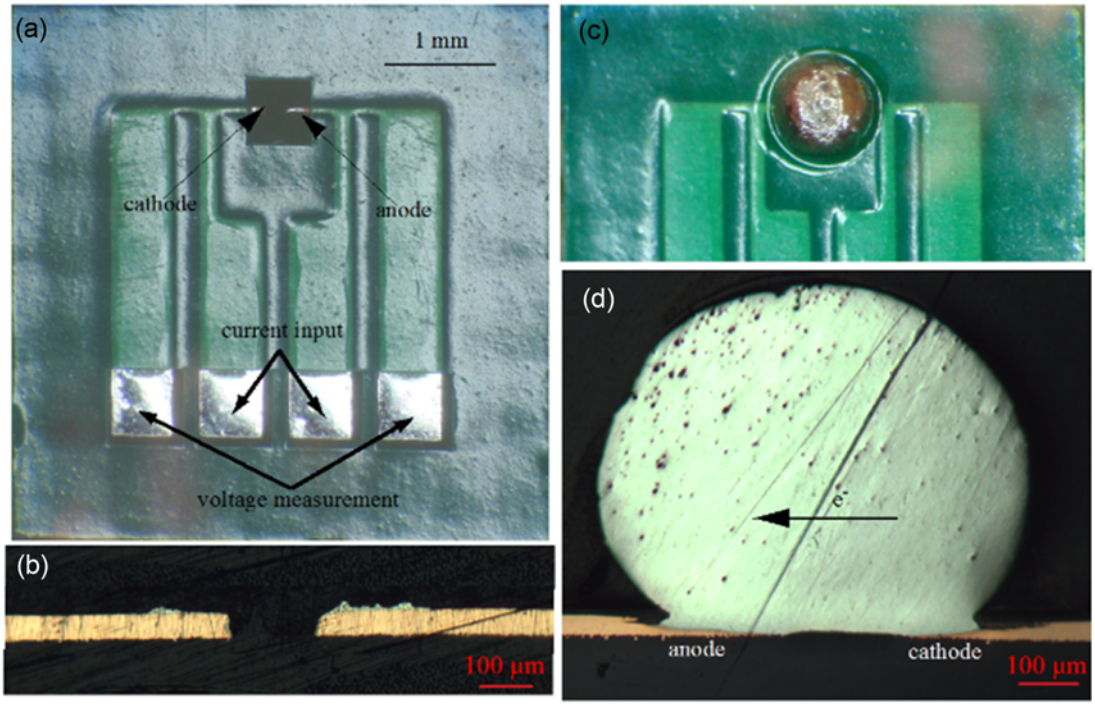


Fig. 1. The top views (a, c) and cross-sections (b, d) of a test substrate before (a, b) and after (c, d) reflowing of a SAC solder bump. The thicknesses of the copper lines and solder resist are 35.4 ± 1.7 μm and 14.3 ± 0.6 μm, respectively. The average horizontal diameter and height of the solder bumps are 869 ± 33 μm and 710 ± 10 μm, respectively. Errors are standard deviations and samples sizes are 5 for all the measurements.

substantial dissolution of the copper lines into the solder ball which is typical for SAC solder.[13] The reflowed solder bumps are subsequently used for high current aging tests in which current would appear to flow laterally from one side of the ball to the other, a situation different from the usual configuration where current flows vertically through the solder joint. However, the numerical results for our solder bumps show current mainly flows vertically following the path of least resistance into the solder as described in section 3.

A high current aging test is used to evaluate the reliability of the solder bump in terms of electromigration. The four wire method is used to measure the joint resistance, as shown in Fig. 1c. To accelerate the aging test, the ambient temperature of the sample is elevated to 160°C. This temperature level was chosen as high as possible without melting the solder bump together with the thermal input from Joule heat from the aging current. To avoid sample damage from thermal shock,[14,15] the sample is heated and cooled slowly enough inside the oven. Compared with current aging, the effect of 160°C thermal aging alone is assumed to be negligible.

The aging current is chosen as 2.2 A after several trial and error experiments to find that higher currents result in too much Joule heat and melt the solder bump while lower currents result in no obvious change in observation during 200 h. The current source is a programmable DC power supply with a current resolution of 1 mA and a current range of 5 A. No discernible drifting is seen from recorded output over 16 h. The temperature, voltage and current are all recorded throughout the aging test in 4 s intervals.

As a result of the substrate geometry and four wire method, the resistance measured also includes part of the copper lines. To better understand the contribution of the copper lines to the resistance signal and the contribution of various failure modes to the resistance increase during aging, a FE model is built and explained in the next section.

3. DISTRIBUTION OF CURRENT IN SOLDER BUMP (FE MODEL)

The software used for the FE study is COMSOL 4.3b. Only DC current is simulated. The geometry is modelled in 3D with components shown in a cross-section in Fig. 2 with dimensions. For simplicity, only two parts of the copper lines and the solder ball are modelled and any IMCs are neglected. The width of the copper lines is 68 μm, and the diameter of the solder ball is 792 μm. The geometry was meshed with 451224 tetrahedral elements. The calculation lasted about 27 s on a standard PC. The electrical conductivity values and the resistance values at room temperature and 160°C are shown in Table 1. The solder bump resistance is calculated from the average simulated voltage drop between

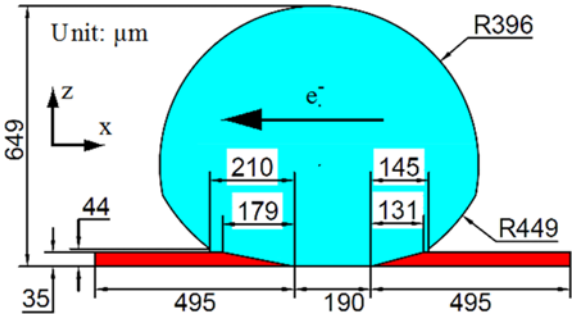


Fig. 2. Illustrative cross-section of the 3D FE model of solder bump. Cu line width is 68 μm.

Table 1. The electrical conductivities and the calculated resistances in the FE model.

	20°C	160°C
Copper conductivity [S/μm]	59.6	38.7
SAC conductivity [S/μm]	7.99	4.90
Total resistance [mΩ]	5.94	9.24
Solder bump resistance [mΩ]	0.84	1.36

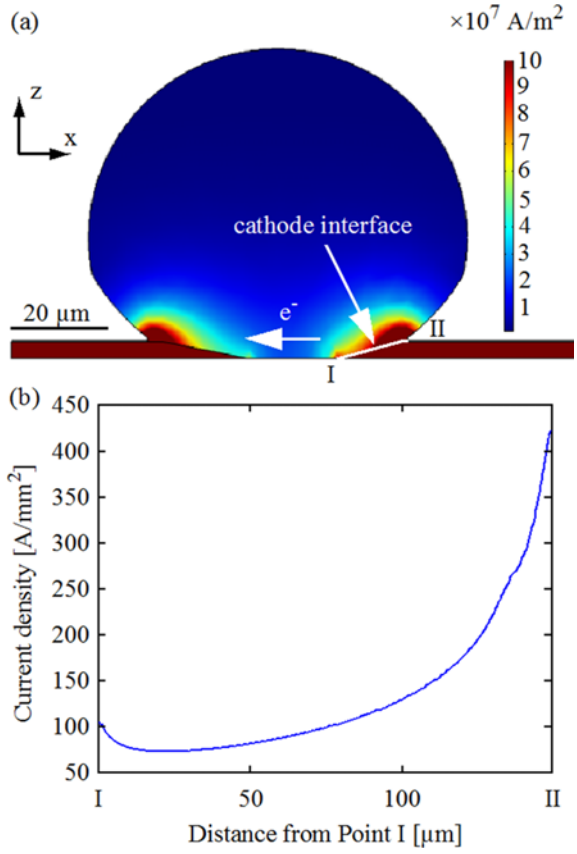


Fig. 3. (a) Simulated current density distribution in the cross-sectional plane of the unaged SAC solder bump during current aging test at 160°C. The current applied to the sample was 2.2 A. (b) the current density distribution along the cathode interface in the cross-sectional plane from points I to II as defined in (a).

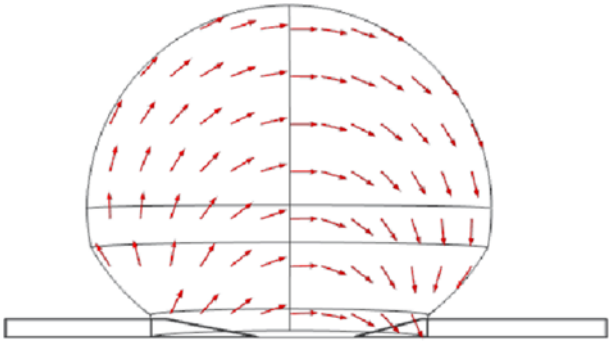


Fig. 4. Simulated current direction distribution in the cross-sectional plane of the SAC solder bump during current aging test. Most of the current flows vertically into the bump. The arrow size is normalized.

the two solder/copper interfaces. The copper conductivity is from[16] and the SAC conductivity is measured from the as received flux-free solder wire. The total resistance is calculated from the voltage drop between outer ends of the copper lines for an applied current of 2.2 A, resulting in a current density of 924 A/mm^2 in the Cu lines.

The current density distribution on the cross-sectional plane of the FE model is shown in Fig. 3a. The current density distribution along the cathode interface in this cross-sectional plane is shown in Fig. 3b. The current density varies along the interface. The highest current density along the cathode interface is at point II in Fig. 3b. The highest current densities along the cross-sectioned interfaces are 423 A/mm^2 on cathode side and 394 A/mm^2 on anode side, respectively. The difference is due to the difference in interface length (Fig. 2).

The highest current density along the interface is at point II and is directed mainly in vertical direction as shown by the numerical result in Fig. 4. The current flows mainly vertically at the SAC-Cu interface since the path of least resistance is through the bulk of the bump, rather than through the more direct but thinner path at the bottom of the bump.

4. RESULTS

4.1 Four Stages of Joint Resistance

A typical resistance signal curve is shown in Figs. 5a-c. In this example, the resistance changed from 6.6 mΩ at room temperature to 10.2 mΩ at the elevated temperature. Corresponding average results from five samples are 7.7 ± 1.8 mΩ and 11.8 ± 2.8 mΩ, respectively. Errors are standard deviations. These value ranges are ~15% larger than the simulated values for the total resistance in Table 1 which possibly is due to variations in Cu line thickness or length. Time 0 is defined as when the current was switched from 0.1 A to 2.2 A after the oven temperature was stabilized. Figure 5d shows the *dR/dt* versus time curve, where *dR/dt* is smoothened

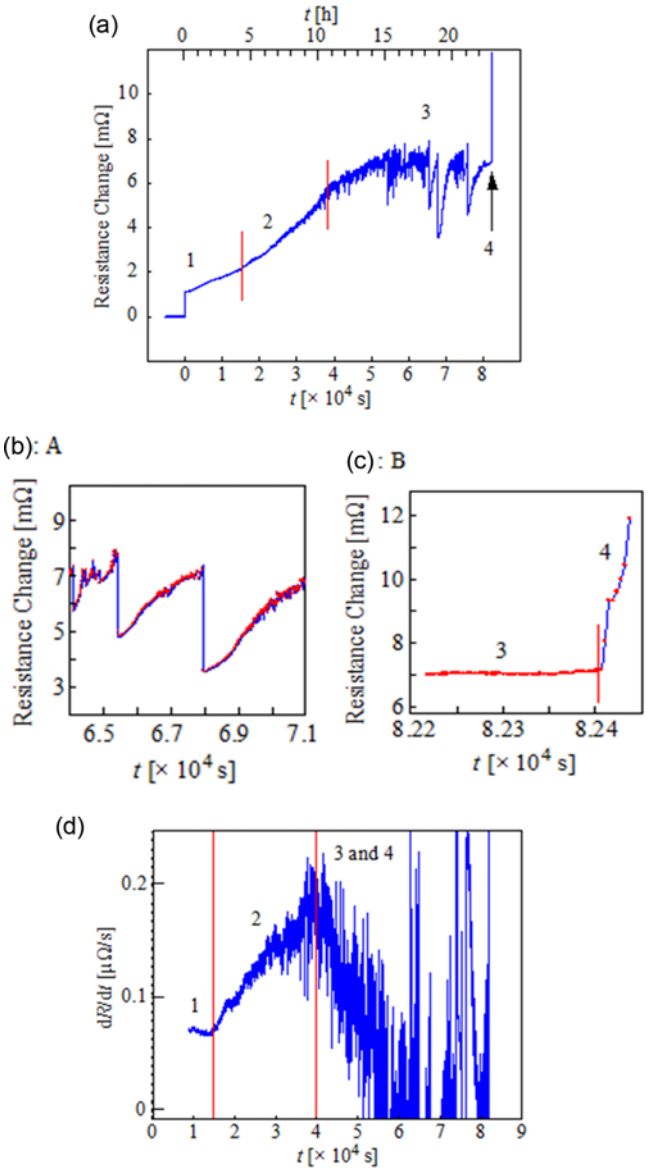


Fig. 5. The (a) over view, (b) example of abrupt resistance drops, and (c) the final failure of a typical resistance change vs. time curve at 160°C. Red dots are recorded data. (d) The *dR/dt* curve of the same example (moving average 4000 s).

using the average over a moving interval of 8000 s.

Four stages are seen in this example. Stage 1 has a constant slope ranging between 0.09 mΩ/h and 0.25 mΩ/h and lasts until about 15 ks. Afterwards the slope increases to 0.53 - 1.04 mΩ/h at about 40 ks (Stage 2). After that, abrupt drops of resistance signals start to become dominant (Fig. 5b) each followed by a slow rise of approximately equal magnitude (Stage 3). Such drop-rise cycles occur every few minutes and generally get larger as the aging continues, the biggest resistance drop being 4 mΩ in the example of Fig. 5b. Similar resistance behavior is also seen

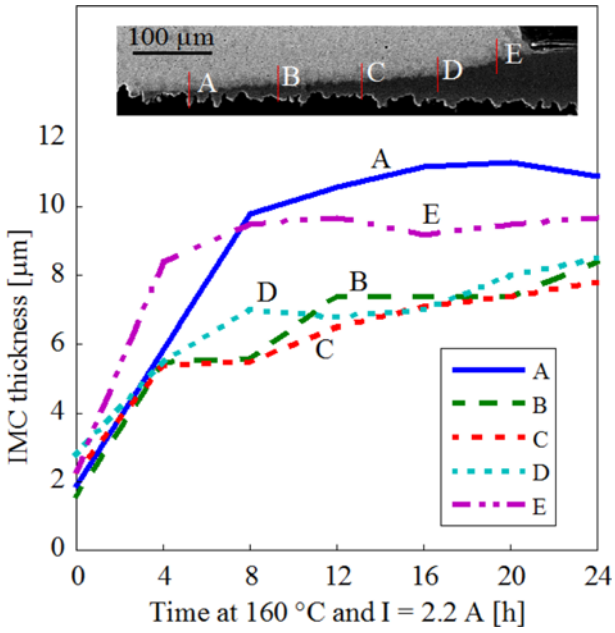


Fig. 6. IMC thickness at locations A, B, C, D, and E.

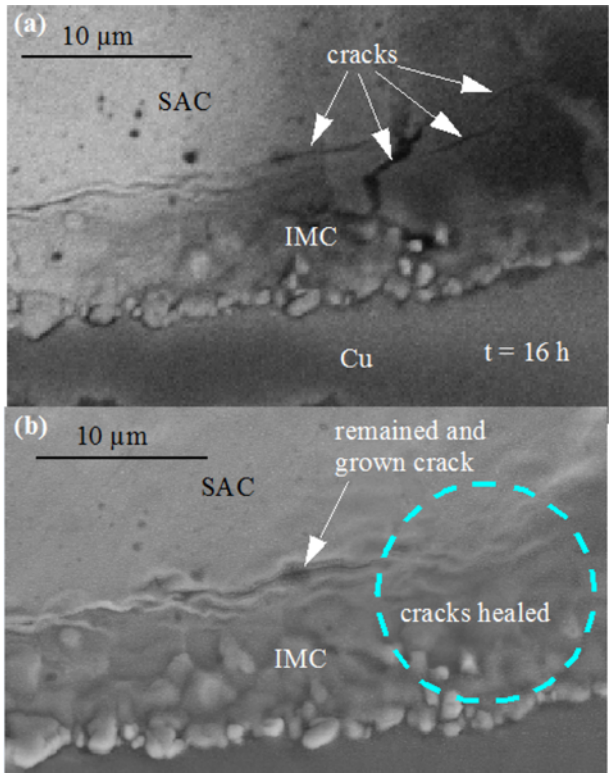


Fig. 7. The cross-sectional SEM images of a typical cathode joint interface after aging at 160°C 2.2 A for (a) 16 h, and (b) 20 h, respectively.

in [11]. Stage 4 is characterized by the abrupt rise of the signal leading to complete failure (open circuit) within typically 10 - 50 s.

4.2 Aging a Cross-Sectioned Sample

A single sample was cross-sectioned and then aged at 4 h intervals and analyzed at 4 h, 8 h, 12 h, 16 h, 20 h, and 24 h, respectively. In each step, the sample is cooled slow enough inside the oven to avoid thermal shock induced stress. A similar method is also used in [5,6]. No IMCs other than Cu_6Sn_5 is seen throughout the whole aging test of this sample, as identified with EDX. The thickness of the IMC is measured at five locations at different times of aging, as shown in Fig. 6. The IMC growing rate is different at different locations along the interface. In locations A and E, the IMC thickness reaches 9.8 and 8.4 μm in 8 and 4 h, at rates of 1.0 and 1.5 μm/h, respectively, and keeps increasing at rates of 0.7 and 0.4 μm/h until 24 h. In the central locations B to D, IMC grows to 5.4 - 5.5 μm in the first 4 h, and slows down to average rates of 0.13 - 0.14 μm/h during 4 to 24 h. The average rates are calculated from linear fits.

Thicker IMC layers are observed at the periphery of the interfaces (locations A and E) compared to the central interfacial area (locations B, C, and D). This possibly is due to the current density being higher at the periphery compared to the central area as shown in Fig. 3b. Higher current density causes higher rate of Joule heat input and thus higher local temperature, leading to a faster IMC growth rate. Moreover, a higher current density also results in a faster electromigration rate, further accelerating IMC growth.

However, not only Joule heat and electromigration can affect IMC thickness but also Cu atomic concentration in the bump near the interface due to reflow, and/or the temperature distribution due to the effect of geometry. On one hand, the localized reflow history possibly resulted in more Cu dissolved into the SAC near location A where more Cu was dissolved than at other locations along the interface. A thicker IMC layer after aging possibly results from more Cu dissolved into the adjacent bump region during reflow. On the other hand, heat build-up possibly is highest close to the center (location A) because it is farthest from the surface of the bump, which can result in higher temperature than caused by Joule heating alone. These two factors possibly explain why the IMC thickness is highest at location A where the current density is relatively low according to Fig. 3b.

IMC can also be a barrier for diffusion between SAC and Cu. When the IMC becomes thick enough, the growing rate slows down due to slower diffusion between SAC and Cu. This results in the IMC growing rate at locations A and E to be slower than B to D after 8 h of aging.

The cross-sectional images of the cathode interface after 16 h and 20 h at 160°C and 2.2 A are shown in Figs. 7a-b, respectively. Cracks are observed in after 16 h aging, some of which disappeared after 20 h aging, indicating a self-

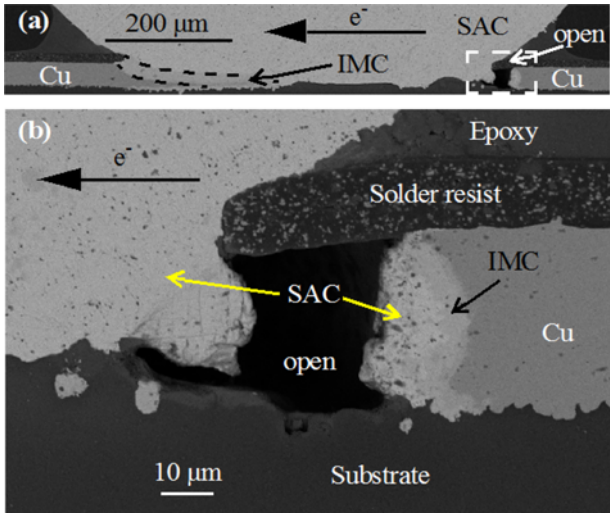


Fig. 8. (a) The cross-sectional SEM image of a typical solder joint after complete failure at 40.19 h. (b) Magnified image of the rectangular zone in (a).

healing process taking place. The resistance signal of this cross-sectioned sample indicates that it is in Stage 1 before 24 h.

4.3 Cross-sections after complete failure

Cross-sectional images of a typical failed sample are shown in Figs. 8a-b. This sample was cross-sectioned after the end of the test. The open is shown in more detail in Fig. 8b. In all samples complete failure is characterized by open cathode joints.

The original cathode interface disappears after complete failure, and the open locates below the solder resist. On the left side of the open is the SAC. On the right side of the open is the Cu line. From the cross-sectional images, the horizontal distance between the right end of the open and the left end of the solder resist ranges from 20 μm to 48 μm. Both IMC layer and SAC layer are observed on the end of the Cu line. The thickness of both IMC and SAC layers together ranges from 10 μm to 36 μm, and the thickness of all the observed IMC layer is 6 μm.

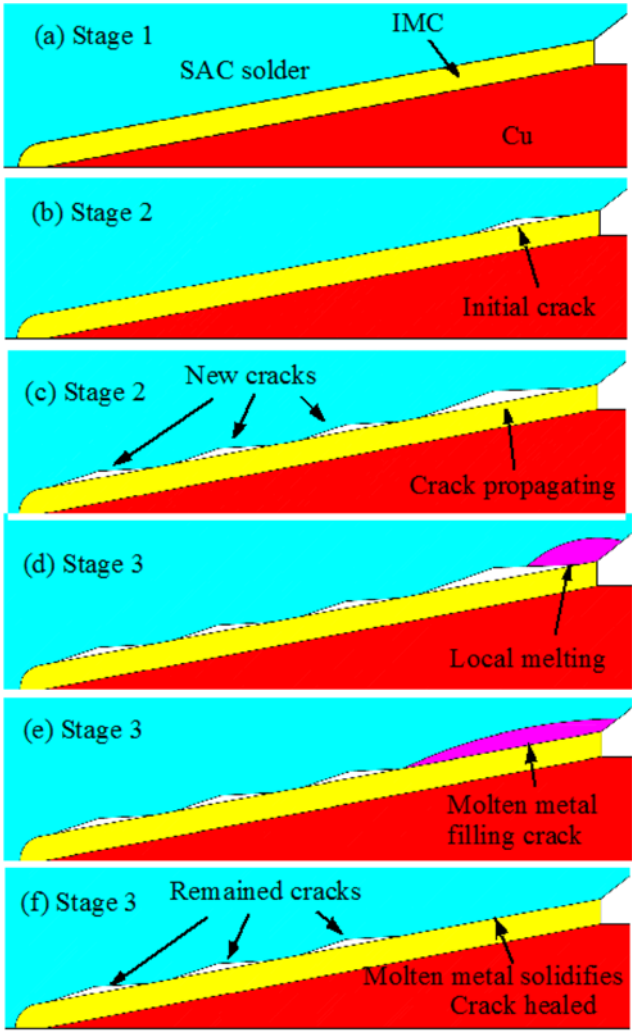


Fig. 9. The different stages of suggested joint interface evolution during current aging test. Stage 1: (a) IMC forming at the interface. Stage 2: (b) the initial crack forming, and (c) the crack propagating along the joint interface while new cracks form. Stage 3: (d) local melting at one contacting asperity due to Joule heat, (e) molten metal filler the crack nearby, and (f) molten metal solidifies and new joint interface forms after one crack is healed. Only cathode is shown.

5. DISCUSSION

The observed interface evolution during the aging test include IMC growth (Fig. 6), crack formation, crack propagation, crack healing (Figs. 7a-b), and opening (Figs. 8a-b). These events all affect the resistance signal, and different stages of the resistance signal are dominated by different events.

A possible explanation for the resistance signal showing different stages in Fig. 5 is given using the illustrations in Figs. 9a-f. In Stage 1, the resistance change is dominated by IMC growth.[17] In Stage 2, in addition to IMC growth, the formation and propagation of cracks at the joint interface becomes dominant on the resistance signal change. As a result, the resistance signal rises faster than in Stage 1. In Stage 3, crack formation and propagation continues, interrupted by sporadic crack healing events, resulting in periodical drop and rise of resistance signals. Though crack formation and healing can be possible in Stage 1, it seems to be too small for affecting the resistance signal in this stage.

The crack in Fig. 7 is caused by electromigration.[18,19] Due to the directional nature of electromigration, cracks preferably form at the cathode[4,18-22] as observed in this study. Though the cross-sectioned sample underwent thermal

cycles resulting from taken out of and put into the oven, the number of such thermal cycles is not large enough to cause cracking at the interface.[14,15]

The apparent instantaneous drop in resistance is either caused by rapid atomic diffusion filling a crack or by local melting and crack filling by the molten material, caused by increased Joule heating of interfacial asperities next to the crack. When the joint resistance increases to a critical value due to crack propagation, the Joule heat increases locally due to the current being concentrated. When the Joule heat is so high that the local temperature can reach the melting point of SAC. The SAC melts locally at the interface and fills the cracks nearby. Less current goes through the molten part because of the higher resistivity of liquid metal than solid metal. As a result, the local temperature drops abruptly and the molten metal solidifies.

The process from the start of local melting to the end of solidification can take less than the sampling period of the experimental setup 4 s, and possibly is much shorter, which is consistent with the resistance signal shown in Fig. 5, where all drops are shorter than one single sampling period.

6. CONCLUSIONS

By monitoring resistance during current aging of SAC to Cu joints and comparing with results from cross-sections, it was possible to clearly identify four stages of aging were identified. Possible explanations were given for mechanisms underlying each stage. Specifically in Stage 3, the resistance signals drop and rise periodically, where the drops are abrupt while the rises are relatively gradual. The abrupt resistance signal drops are explained with crack self-healing event found with cross-section studies.

The method presented in this study is well suited for efficient characterization of solder bump reliability, e.g. for quick comparison of different solder types. The method relies on a custom low-cost substrate and involves simply steps of specimen preparation and subsequent testing. The continuous resistance recording provides ample data for efficient reliability characterizations under current and temperature loads.

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