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Review Paper

Physical Principles and Current Status of Emerging Non-Volatile Solid State Memories

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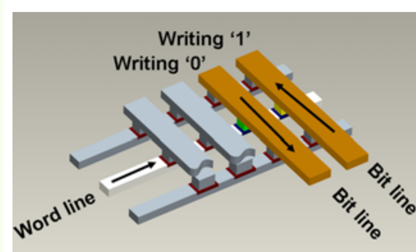

Today the influence of non-volatile solid-state memories on persons' lives has become more prominent because of their non-volatility, low data latency, and high robustness. As a pioneering technology that is representative of non-volatile solid-state memories, flash memory has recently seen widespread application in many areas ranging from electronic appliances, such as cell phones and digital cameras, to external storage devices such as universal serial bus (USB) memory. Moreover, owing to its large storage capacity, it is expected that in the near future, flash memory will replace hard-disk drives as a dominant technology in the mass storage market, especially because of recently emerging solid-state drives. However, the rapid growth of the global digital data has led to the need for flash memories to have larger storage capacity, thus requiring a further downscaling of the cell size. Such a miniaturization is expected to be extremely difficult because of the well-known scaling limit of flash memories. It is therefore necessary to either explore innovative technologies that can extend the areal density of flash memories beyond the scaling limits, or to vigorously develop alternative non-volatile solid-state memories including ferroelectric random-access memory, magnetoresistive random-access memory, phase-change random-access memory, and resistive random-access memory. In this paper, we review the physical principles of flash memories and their technical challenges that affect our ability to enhance the storage capacity. We then present a detailed discussion of novel technologies that can extend the storage density of flash memories beyond the commonly accepted limits. In each case, we subsequently discuss the physical principles of these new types of non-volatile solid-state memories as well as their respective merits and weakness when utilized for data storage applications. Finally, we predict the future prospects for the aforementioned solid-state memories for the next generation of data-storage devices based on a comparison of their performance.

Keywords: solid-state memory, non-volatility, flash, FeRAM, MRAM, PCRAM, RRAM

1. INTRODUCTION

Solid-state memory is a data-storage device that stores data using integrated circuit assemblies without mechanical components, and this distinguishes it from magnetic or optical memory, which contain spinning discs and movable wire/read heads. Solid-state memory can be classified into as volatile memory (VM), which requires power to retain data, and non-volatile memory (NVM), where data can be stored even during a power- off state. Static random-access memory (SRAM) and dynamic random-access memory (DRAM) are two typical examples of volatile solid-state memories. A typical SRAM cell consists of six transistors, of which four are used to store the binary bit and the other two are responsible for controlling the access to the cell during write and read operations. Although this 6T architecture increases the cell size, thus reducing the operation margin for the areal density improvement, the unique flip-flop mechanism of the transistor has enabled SRAM to have faster speed and lower power consumption than any other solid-state memories.[1] Note that in the field of semiconductor memory, the cell size is usually denoted in terms of the number of F^2 units required, where F is known as the feature size or technology node, which is the average half-pitch of the memory cell, i.e., half of the distance between identical features. For these reasons, SRAMs are generally embedded in central processor units (CPU) and function as general high-performance Level 1 (L1) and Level 2 (L2) cache memory.[2] Compared to SRAM memory, DRAM memory exhibits a relatively simple cell structure that comprises a capacitor and a transistor, giving rise to a higher areal density than SRAM. Nevertheless,

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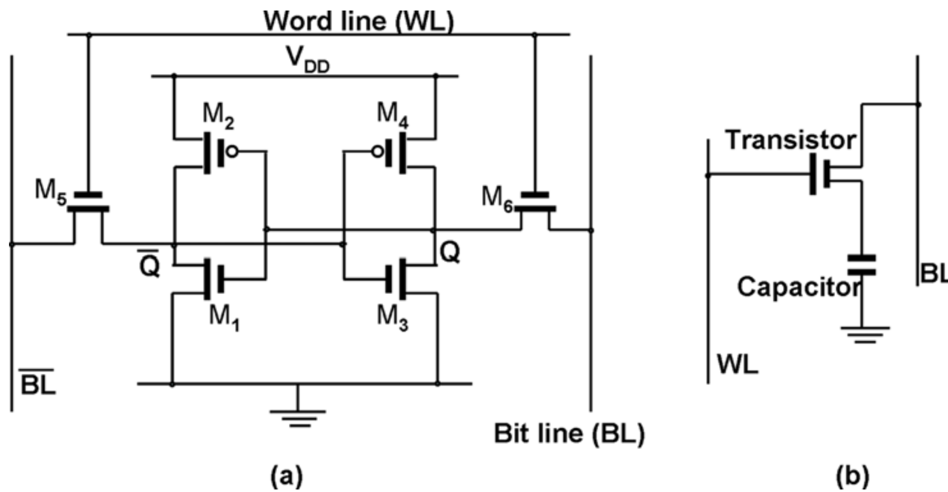

Fig. 1. The cell structure of (a) SRAM and (b) DRAM.

cell capacitors need to be recharged every few milliseconds in order to restore the data, resulting in additional power consumption. Considering its characteristics, DRAM memory has been adopted mainly as the main memory of personal computers (PCs) for the temporary storage of data and instructions that are read and executed by CPUs. The cell structures of SRAM and DRAM memories are schematically shown in Fig. 1.

Volatile solid-state memories usually display a faster write/read speed than mass storage devices such as hard drives, and can be used to store sensitive data that need to be unavailable during power off. However, VM is incapable of retaining data that requires long retention times, triggering the advent of non-volatile solid-state memories. Erasable programmable read-only memory (EPROM) has been widely regarded as the earliest member of the non-volatile solid-state family. EPROMs make use of a special programmer circuit to record data that can be subsequently erased using ultraviolet light. It should be noted that EPROMs usually need to be removed from the device for erasing and programming, and this inconvenience led to the development of electrically erasable programmable read-only memory (EEPROM), which can be programmed and erased in circuits using special electrical signals. In spite of the inherent non-volatility, these erasable ROMs require a long time to erase data and to write new data as well as a higher operating voltage compared to the one normally used in digital circuits. These drawbacks have led researchers worldwide to focus on the development of new types of non-volatile solid-state memories, which has resulted in the introduction of flash memory. The development of flash memory is considered as a milestone in the history of solid-state memory, and it was actually an updated version of EEPROM, that enabled a significantly higher capacity than that of the traditional EEPROM. While flash products can only erase predetermined sections of the chip (also known as 'blocks' or 'pages'), this property enables us to use flash to write large amounts of data into the "block" at a time, leading to a much faster writing speed than its predecessor. Based on the difference in the cell structure, flash memory can be categorized into NAND flash and NOR flash. NAND architecture offers extremely high cell densities and high capacity as well as fast write and erase rates, and it has therefore been widely implemented in data storage applications such as memory cards, universal serial bus (USB) drives, and solid-state drives. On the other hand, NOR flash is a type of RAM that enables easy access to each of its bytes. For this reason, NOR flash is typically used for code storage and execution applications such as simple consumer appliances, low-end cell phones, and embedded applications. At present, flash memory is considered as a suitable replacement for magnetic hard disks because of its extraordinary potential for high areal density, fast access times, and stable operation. Further, flash memories with 1 TB capacity have already been released by Kingston Corporation.

Despite the rapid growth in the capacity of flash memory, we also need to consider that there is an unprecedented rate of growth of the amount of digital data that is generated globally. It was reported that the amount of data generated worldwide has crossed the 4 ZB barrier in 2013,[3] and is expected to reach 40 ZB in 2020.[4] Therefore, in order for flash memory to dominate the current data-storage market, its storage capacity needs to be enhanced so that its rate of growth exceeds the rate of growth of digital data. This requires a continuous downscaling of the cell size. Nevertheless, further scaling down the cell size would induce several scaling-imposed limitations, such as a conventional lithography limit, tunnel-oxide thickness limit, a low gate-coupling ratio, high programming voltage, reduced charge states, and electrostatic interaction between adjacent cells.

Because of the above scaling limits, state-of-the-art NAND and NOR devices are restricted to 20 nm[5] and 45,[6] respectively. To realize a breakthrough in these scaling limits, it is essential to explore some advanced technologies such as 3D stacking of transistors and improvements to the manufacturing process in order to realize continuous increases in the flash capacity. Moreover, even with these innovations, it may still not be possible to economically scale flash to smaller dimensions. In this scenario, concepts involving several new technologies including ferroelectric RAM (FeRAM), magnetoresistive RAM (MRAM), phase-change RAM (PCRAM), and resistive RAM (RRAM), have been proposed, and they remain under investigation as promising candidates for NVM.

In order to improve our understanding of the physical mechanisms behind these prospective memories, and thus trigger more research enthusiasm into the improvement and optimization of the device performances, there is a need for a detailed review concerning the status of these emerging technologies.

2. FLASH MEMORY

As the preferred replacement for conventional mass-storage technologies, flash memory has recently received considerable attention because of its potential high capacity, fast access time, and stable operation. In flash memory, data is stored as a form of an array of floating gate transistors called "cells". Each cell traditionally stores one bit of information, while some newer flash memories, known as multi-level cell (MLC) devices, can store more than one bit per cell. The cell structure depicted in Fig. 2 is similar to that of a standard MOSFET, except that the transistor has two gates rather than one control gate (CG). The additional gate is known as a polysilicon floating gate (FG), and that is insulated all around by a dielectric oxide layer. Therefore, any electrons that are placed in the FG can remain there under normal conditions (e.g., no applied erasing pulse), which leads to flash devices becoming a NVM in which data can be stored even if the power is off. The FG is sandwiched by a tunnel-oxide layer and an inter-poly dielectric (IPD) layer that usually consists of triple oxide-nitride-oxide (ONO) layers. The tunnel layer isolates FG from the channel region inside the substrate, while the IPD layer can effectively prevent possible electron leakage between the CG and FG.

In flash memory, the programming/erasing operations are accomplished by injecting electrons into the FG ("0" state) or by removing electrons from the FG ("1" state) based on either Fowler-Nordheim tunneling[7-9] or channel hot-electron injection.[10-12] A schematic of the typical bias condition for Fowler-Nordheim tunneling is shown in Fig. 3. Fowler-Nordheim tunneling is a quantum-mechanical process where a particle can tunnel through a barrier that classically it

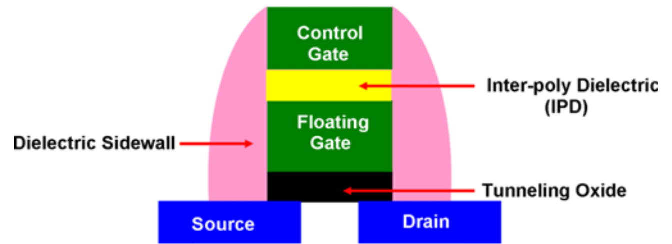

Fig. 2. The structure of the floating gate cell.

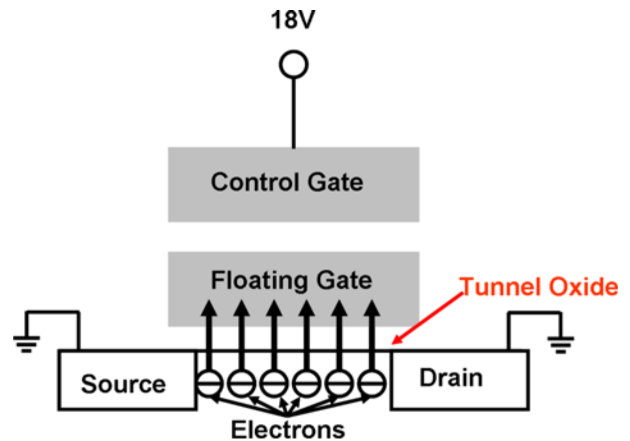

Fig. 3. Programming of Flash memory based on Fowler-Nordheim mechanism.

cannot surmount. To induce Fowler-Nordheim tunneling, a high voltage is applied between the CG and the drain, producing a strong electric field across the tunnel oxide. According to the quantum mechanical theory,[13] such a high field can lower the potential barrier of the tunnel oxide and make it sufficiently penetrable. In this case, the electrons that overcome the oxide tunnel barrier can cross the oxide layer, and they either are then swept into the FG (programming), or are removed from the FG into the channel region in the substrate (erasing). The programming operation can be realized by applying a positive voltage between the CG and the drain, whereas then application of a negative voltage would give rise to the erasing process. However, the physical mechanism of channel hot-electron injection is different from that of Fowler-Nordheim tunneling, which can be recognized from Fig. 4, showing its cell-bias conditions during the programming operation. As illustrated in Fig. 4, a high source-to-drain voltage is applied in conjunction with a high gate voltage. This high source-to-drain voltage would generate a strong lateral field across the channel, where the electrons will thereby gain sufficient kinetic energy and accelerate toward the drain. Prior to entering the drain and being swept away, the electrons collide with the silicon lattice and are redirected toward the tunnel oxide with the aid of the vertical gate field. This would render electrons captured

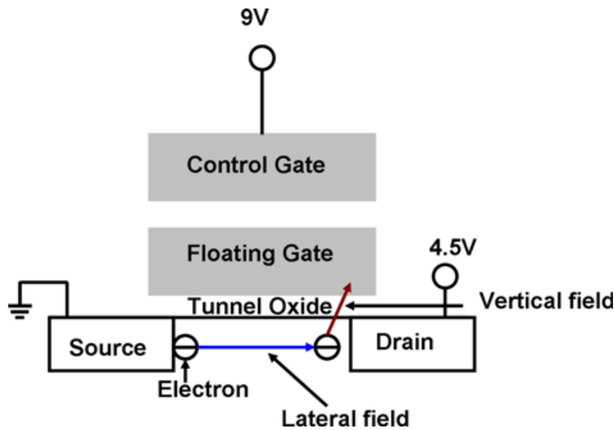

Fig. 4. Programming of Flash memory based on channel hot electron injection mechanism.

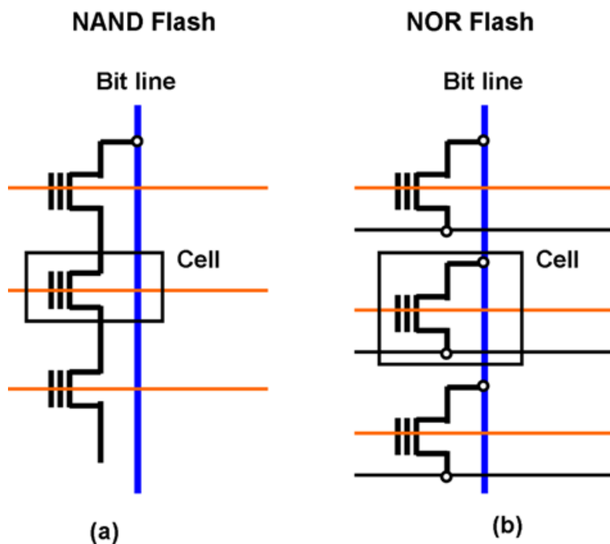

Fig. 5. Cell architecture of (a) NAND Flash and (b) NOR Flash.

on the FG and retained as stored charges. The readout operation is performed by applying a voltage around the threshold voltage of the MOSFET channel between the source and drain to form a current, which is sensed and interpreted as a binary bit.

As mentioned above, flash memory can be classified as either NAND flash or NOR flash in terms of the cell structure, as illustrated in Fig. 5. In NOR flash, cells are arranged in parallel such that one end of the cell is connected to ground and the other is connected directly to a common drain that is called a bit line, which resembles a NOR logic gate. When one of the word lines (connected to the CG of the cell) is made high, the corresponding storage transistor acts to pull the output bit line low. Owing to its architecture, NOR flash can allow for a fast read performance while yielding a high die cost and large power consumption. This is primarily because of the increase in the cell size.[6,14] In contrast to NOR, NAND flash builds cells in series with adjacent cells that share the source and drain. This specific structure waives the requirement for an extra metal line and thus significantly reduces the cell size, enabling the NAND memory to have a much smaller cell size and lower die cost than the NOR memory.[5,15] However, NAND gives a slow read performance, as the readout current is lower when using a serial transistor.[16] As a result, NOR flash is often used for fast code executions such as in the basic input/output system in PCs and it has applications in almost all handheld devices technology, including that of cellphones and PDAs. On the other hand, NAND flash is employed mainly for data-rich applications such as digital still cameras (DSCs), USBs, MP3s and iPhones, for which slow read speeds are not an issue.[17]

Flash memory has become a ubiquitous device for consumers worldwide, and the growth rate of its storage capacity is even faster than the prediction by Moore's Law that the capacity of storage device will double every two years.[18] In addition, if the number of electrons in the FG can be controlled precisely, the readout current can be therefore sensed at a larger number of levels (instead of either “presence” or “absence”) resulting in the storage of two or more bits of information per memory cell without any shrinkage in feature size; this is called multi-level technology. Although disadvantages such as low capacity and large power consumption have limited the application of NOR flash as mass storage, it has been widely implemented in embedded systems because of its fast random-access function. In addition, as the driving force for the growth of NOR flash technology, significant price reductions have been observed over the past 15 years, decreasing from approximately US $80,000/GByte in 1987 for the first ETOX™ NOR Mbit flash product to about US $32/GByte in 2011 for Gbit devices.[6] NOR flash with a capacity of 8 Gb at 45 nm was released in 2012, and has been in production since 2013.[19] However, it should be noted that in spite of the recent developments in NOR technology, the influence of NOR flash in the solid-state drives (SSD) market has been significantly eroded. This has resulted from the advantages of NAND technology, namely higher density, lower cost, lower power consumption, and faster programming performance. NAND flash is designed at a much lower cost than NOR (about US $1/GByte in 2011[6]), and the latest technology has enabled the bulk production of 64 Gb NAND flash.[20] To date, NAND flash has been considered as a replacement for hard-disk drives (HDDs), and NAND flash-based solid-state drives (SSDs) have already been adopted in PCs and servers to substitute HDDs.[21] Although significant achievements have been realized in NAND and NOR memories in terms of size reduction and cost lowering, flash memory inevitably faces some stern challenges when further scaling down cell size for higher density. Such challenges are

usually classified as physical scaling challenges, electrical scaling challenges, and reliability challenges,[16] as detailed below.

2.1 Physical scaling challenging

The fabrication of flash memory requires a variety of physical and chemical processes performed on a semiconductor substrate (e.g., silicon), for which the fundamental is called photolithography.[22-25] Photolithography, which is also known as optical lithography, is a process used in microfabrication to pattern parts of a thin film or the bulk of a substrate. The first step of photolithography is the substrate preparation, where the substrate is cleaned to remove any undesired substances, such as water, from the substrate surface. Then, silicon dioxide (SiO_2), which acts as a barrier layer, is deposited on the surface of the wafer. Subsequently, a layer such as SiO_2 is coated with a photoresist film whose solubility can be changed when exposed to light. This would enable the selective removal of either the exposed or non-exposed regions of the photoresist by immersing it in a solvent (called "developer"), which is known as "development". Photoresists can be classified as a positive photoresist and a negative photoresist. The difference between these two photoresists is the solubility of the photoresist portion that is exposed to light. The region of the positive photoresist that is exposed to light becomes soluble to the photoresist developer, whereas for the negative photoresist, the exposed region remains insoluble. After deposition of the photoresist, mask alignment is the next step. A mask or "photomask" is an opaque plate with holes or transparencies that allow light to shine through in a defined pattern. The photomask should be aligned with the substrate so that the pattern can be transferred onto the substrate surface. Once the photomask is accurately aligned with the pattern on the substrate surface, it is exposed to a very intense light through the pattern on the photomask, and this causes a chemical change that allows some of the photoresists to be removed by the corresponding developer. The patterns that are lithographically printed in photoresists must be mapped into the substrate, and this can be achieved using the etching process. Etching that uses either liquid ("wet") or plasma chemical agent ("dry") is carried out to remove the region that is not covered by photoresist, thereby transferring the pattern to the oxide layer. Finally, the remaining photoresist is removed using a simple solvent, which is called a resist stripper, giving rise to a substrate with a patterned oxide layer. A schematic of the entire photolithography process is shown in Fig. 6.

It is accepted that photolithography plays an important role in determining the physical scaling size of a flash cell. However, the minimum feature size that can be printed by a photolithography system is roughly proportional to the ratio of the laser beam wavelength (λ) to the numerical aperture (NA) of objective lens.[26,27] In this case, by either reducing the beam wavelength or increasing the numerical aperture, we can effectively reduce the feature size, and this would reduce the depth of the laser focus that is inversely proportional to the ratio of λ to NA.[28,29] Consequently, the feature size obtained from conventional lithography is confined to an approximately 40 nm technology node.[30] In this case, new techniques such as self aligned double patterning, where the conventional lithography process is enhanced to produce double the expected number of features, has been proposed to extend scaling beyond conventional lithography limits.[16,31,32] This technique allows the space between lithographic lines to be further subdivided, thus enabling NAND scaling to 20 nm.[16] For the NOR case, double patterning cannot scale lithography nodes below 65 nm, for which the layout of the memory cell has a 45°

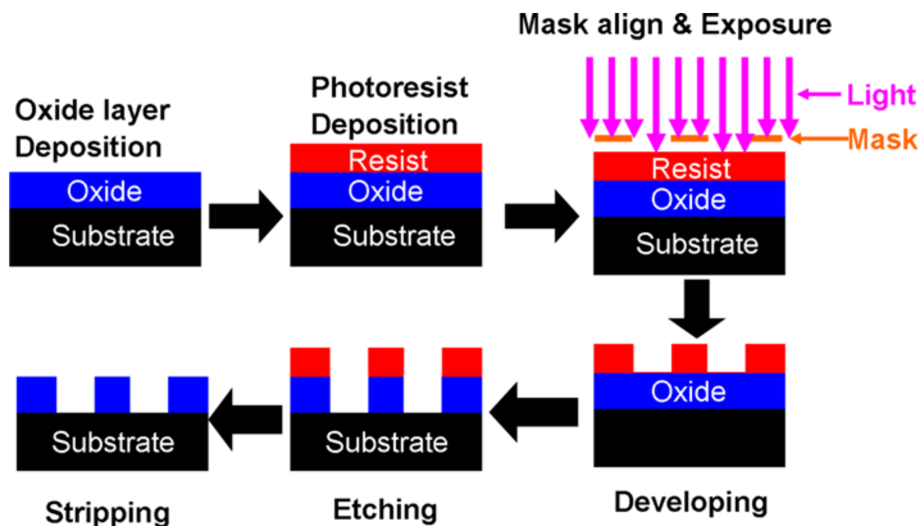

Fig. 6. The steps of the photolithography process.

angle structure around a source contact that is not conductive optically.[33-35] Accordingly, a self-aligned contact (SAC) technology has been introduced to enable a NOR cell at approximately 45 nm.[33] The SAC architecture can further scale down the NOR cell by introducing patterning-friendly line/space features rather than 1D holes to form drain plugs, and by allowing the direct proximity of drain plugs over the gate spacer.[33] The potential of using this technology to further scale NOR cells down to around 20 nm has been envisioned.[6] In addition to the above two solutions, the recent development of 3D flash memory technology is another possible approach to alleviate conventional lithographic limitations. 3D devices have more bits at a fixed area in the X/Y plane by introducing another scaling dimension, namely the Z direction. One of the pioneering companies in the fabrication of 3D flash memory is Toshiba, which has developed 3D NAND processes with its bit cost scalable (BiCS) product.[36] This approach enables the fabrication of 3D stacked devices in a few steps and does not require repetitive processing, thus promising a new low-cost scaling path to NAND flash fabrication. As depicted in Fig. 7, such a BiCS architecture turns the NAND string by 90 from a horizontal to vertical position. The word line remains in the horizontal planes. This allows for a more economical fabrication process compared to the stacking of complete devices, and the cost benefit does not decrease for a very high number of layers. Since the advent of BiCS, various novel 3D structures such as pipe-shaped BiCS (P-BiCS),[37] terabit cell-array transistor (TCAT),[38] vertical stacking-array transistor (VSAT),[39] and vertical gate (VG)[40-42] have been proposed to realize higher density and lower cost. Recent stacked-memory-devices-on-logic (SMOL) structures that integrate VSAT and PIPE architectures have shown potential for terabit-level memory densities in a cost-effective manner.[43]

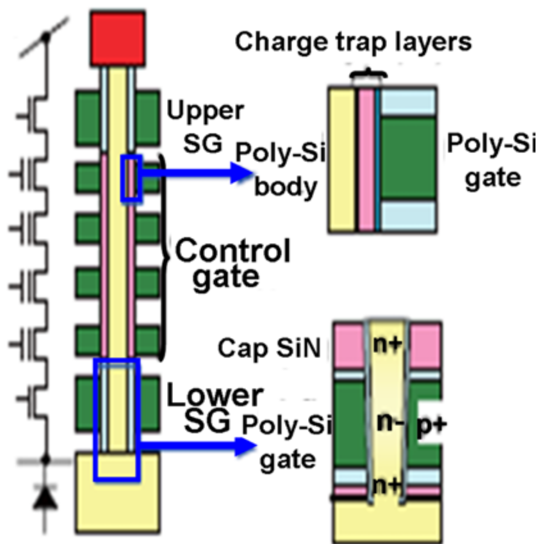

Fig. 7. 3D NAND Flash based on BiCS structure. Reprinted with permission from.[36]

2.2 Electrical scaling challenging

The electrical scaling challenges faced by flash technology can be sub-classified into the following aspects. First, the tunnel-oxide layer needs to be thick enough to prevent electrons tunnelling which is due to defects in the tunnel oxide based on the "percolation" theory,[44] as illustrated in Fig. 8. Therefore, for long data retention, a tunnel-oxide layer with a thickness greater than 8 nm is required,[5] and this corresponds to a node that is greater than 20 nm. A possible solution to this problem is to implement a nanocrystal FG using the structure given in Fig. 9.[45] Nanocrystal FGs store electrons in nanocrystals, and electron loss is therefore caused only by defects that are directly underneath the nanocrystal, while electrons stored in other nanocrystals will remained. It is necessary to ensure that the size of the nanocrystals is less than 2 nm in order to prevent statistical fluctuations when the scaling cell size is below 20 nm.[5] The most commonly used methods employed to form nanocrystals as a trapping center are self-assembly,[46] precipitation,[47] and chemical reaction,[48] of which the last two are widely believed to be better able to form nanocrystals for a mixed material trapping layer because of the ease with which the density and size of the nanocrystals can be controlled.[49] From the perspective of the materials, nanocrystal memory can be classified as semiconductor nanocrystal, metal nanocrystal, and high-k dielectric nanocrystal. Considering

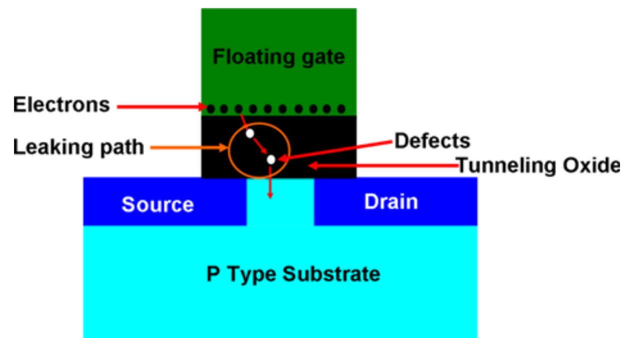

Fig. 8. Electron leakage due to the thin tunnel oxide.

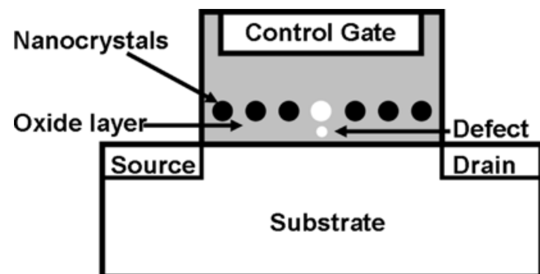

Fig. 9. Nanocrystal Flash cell.

the natural compatibility with the semiconductor industry, semiconductor materials such as Si and Ge are widely used for nanocrystal memory.[50-55] Si nanocrystal memory was introduced as a replacement for the conventional FG structure in the 1990s, and it has received considerable attention since then. Nevertheless, the trade-off between the operation speed and the retention time has severely impeded its prospects for memory application.[49,50] Compared with Si, Ge nanocrystals enable us to realize a longer data retention time owing to its higher dielectric constant and smaller band gap.[49,50,56] In addition, it was found that by using the Si interface around the Ge nanocrystal, we can increase the barrier height between the Ge/Si interface, thus preventing the leakage of the stored electrons. Metallic nanocrystals such as Au, Pt, Ag, Ni, and Co[57-62] are currently regarded as very encouraging candidates to simultaneously satisfy the fast program/erase speed and long retention time under low voltage operation.[50] This is because of the large energy-band offset between the substrate and storage nodes. Moreover, as the electric field between the metal nanocrystal and the sensing channel undergoes a significant enhancement, the metal nanocrystal memory enables a more efficient program/erase operation.[49] However, the potential metal and oxide reactions and/or metal diffusion toward the substrate after nanocrystal fabrication may degrade the device performance.[63] High-k dielectric nanocrystals,[64-66] which are mainly HfO_2 and CeO_2 embedded in SiO_2, are made from phase separation at the high-temperature annealing treatment (>900°C) of mixed oxides,[49] and they show very little lateral or vertical stored charge migration after an endurance test.[50] This may imply that such nanocrystal memory may be suitable for high-density two-bit memory applications. The major advantage of nanocrystal memory is its superior potential in the development of a thin tunnel-oxide layer, while simultaneously maintaining a long data retention time, as well as a more simplified fabrication process than stacked-gate non-volatile memory devices. Nevertheless, as the size of the nanocrystal cell is further downscaled, the number of nanocrystals contained in each memory cell is also reduced, thus making the syntheses of suitable materials with uniform size and shape more challenging.[50] Besides, although the charge loss through the tunnel oxide is primarily due to the nanocrystal memory, a high-density nanocrystal system may result in charge leakage through the surrounding oxide more readily, which requires passivation of the surrounding oxide.[50]

The second electrical scaling limit involves the gate-coupling ratio (GCR). For the flash memory, the GCR, which is calculated as $Capacitance_{CG\text{-}FG}/Capacitance_{FG}$, must be maintained above 0.6 in order to control the channel and prevent gate-electron injection during the erasing process.[17] The increase in the GCR can be realized by wrapping the control gate around the floating gate to geometrically increase the GCR. Nevertheless, during the downscaling process, there is not enough space remaining to accommodate such a wrapping structure because of the demand for a thick IPD layer to reduce the leakage. This significantly limits the scaling of flash below 20 nm. This drawback can be overcome by using either a high-K IPD material[17,67-70] or a charge-trapping device instead of an FG device.[71-76] The high-K IPD materials enable a high GCR without the requirement for a wrap structure. However, most high-K IPD materials with high GCR value generally exhibit a low bandgap, which is not suitable for flash memory because of its susceptibility to the gate injection. In addition, some high-K IPD materials that have a large bandgap are incapable of offering high GCR. Furthermore, even if we can find a high-K IPD material that has both a large bandgap and high GCR, it may trap electrons during the programming/erasing processes. The solution to this issue is to implement multiple layers of the FG material combined with high-K IPD.[77]

As the downscaling of flash memory using high-K IPD remains challenged, a charge-trapping device has been introduced as an alternative solution to extend the recording density of flash beyond the scaling limits. A conventional charge-trapping device replaces the FG with a nitride layer (normally SiN), and is sandwiched by two oxide layers, as shown in Fig. 10. Because of the absence of FGs associated with a deep trapping barrier of SiN, both the GCR issue and the charge loss in the tunnel oxide can be suppressed using the charge-trapping device, allowing for a thin tunnel oxide (2 - 3 nm). However, the conventional $Si/SiO_2/SiN/SiO_2/Si$ (SONOS) device encountered a problem when using a thin tunnel oxide. The substrate hole may directly tunnel into the nitride layer under a low electric field that is induced by the storage charge to neutralize the electrons, thus impairing the data retention. Hence, to mitigate the performance of SONOS, a set of new nitride storage devices with more reliable performance, such as $TaN/Al_2O_3/SiN/SiO_2/Si$ (TANOS),[72] bandgap engineering SONOS (BE-SONOS),[73] BE-metal/$Al_2O_3/SiN/SiO_2/Si$ (BE-MANOS),[74,75] BE-metal/$Al_2O_3/SiO_2/SiN/SiO_2/Si$ (BE-MAONOS),[74,75] and BE-charge

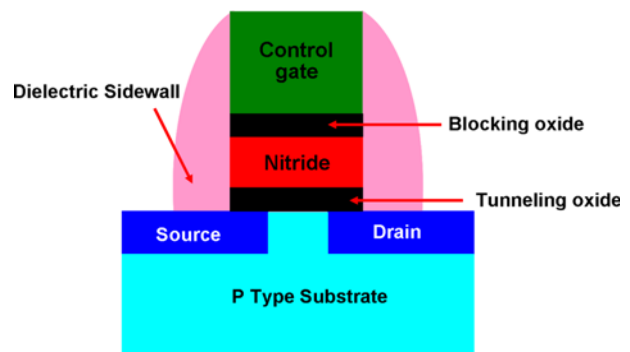

Fig. 10. Cell structure of charge trapping device.

trapping nitride flash (BE-CTNF)[76] have emerged. It is obvious that charge-trapping devices provide better scalability than conventional FG devices and are less prone to cell interference. However, scaling NAND flash memories far below the 20 nm node remains questionable despite the presence of the charge-trapping device.[5,78] This is because reducing the feature size may adversely affect the capability of flash memory to accommodate sufficient electrons, thus deteriorating the retention reliability as well as the programming statistics.[5]

The third electrical scaling limit is the high programming voltage, particularly for NOR. As the programming/erasing mechanism of NOR flash is primarily governed by channel hot-electron injection, a voltage of greater than 4 V is required between the source and drain in order to activate electrons to overcome the barrier height. As a result, to enable it to withstand the high programmed voltage, the gate length cannot be scaled below the channel length. The emergence of the 3D flash cell sacrifices space in the Z direction in return for more space in the X/Y dimension, and it is therefore considered as an effective way of circumventing the gate length limit. In addition, the distance between adjacent cells is reduced by further scaling the cell, which increases the coupling interference between neighboring cells. In this case, the charges stored in adjacent cells would start to affect each other, known as cross talk, eventually resulting in readout errors. Such a problem can be addressed by either decreasing the thickness of the FG,[77] or using charge-trapping devices, where the latter is regarded as the most suitable approach to eliminate FG-FG interference.

2.3 Reliability scaling challenging

As mentioned above, one of the most attractive characteristics of flash memory over other storage devices is its multi-level storage. However, because the multi-level cells (MLCs) give rise to more charge states than single-level cells (SLCs), the variation of the readout current between different charge states is significantly reduced hence increasing readout errors. As a result, the use of error-management techniques such as error-code correction (ECC)[16,79] becomes important for the sake of recovering data or preventing errors, and the need to introduce more efficient ECC engines adopted by the HDD industry into MLC has been investigated.[79-81] In addition to the readout limit, the number of electrons stored in the FG is also reduced when further scaling down the cell because of a decrease in the cell capacitance. It was reported that the number of electrons in NOR flash at 45 nm is around 1000,[16] while for NAND, it is less than 500.[16] Although the number of electrons is smaller at smaller lithographic nodes, the leakage current caused by defects remain the same. In this case, the impact of the defect leakage current on the cell threshold voltage is more pronounced for smaller cell sizes, which may cause fluctuations in the threshold voltage, and even increase the error rate.[6] While such a weakness can be strongly suppressed by using either a charge-trapping device or nanocrystal memory, both the charge-trapping device and nanocrystal memory can store only a smaller number of electrons compared to FG, further exacerbating the decrease in stored electrons for each storage level. Under such circumstances, non-charge-based memory concepts that are presented in the following sections are possible alternative solutions.

The advent of some advanced technologies such as the use of high-K IPD materials and charge-trapping devices can undoubtedly alleviate the scalability of 2D flash memory. However, conventional 2D flash memory will eventually reach its physical limitations along with the continuous shrinkage of the physical feature size. Therefore, a transition from 2D flash to 3D flash is currently required in order to extend the density of flash memory beyond its scaling limits. In 3D flash, multiple layers are stacked in the Z dimension, while a relatively large physical cell size remains in the X-Y dimension. As a result, it is capable of providing a small effective cell size without impairing the cell performance and reliability. Encouraged by BiCS, various low cost 3D architectures have been proposed to date, which can be simply classified into two groups: vertical channel and vertical gate. The vertical channel structure shown in Fig. 11 takes advantages of the transistor channel in the vertical direction,[37] while the vertical gate architecture illustrated in Fig. 12 resembles the placement of blades of 2D NAND arrays vertically side-by-side.[40] Based on one of the aforementioned approaches, Samsung released the first 3D NAND product in 2013,[82] thus inspiring other flash suppliers to explore more advanced 3D NAND products that have different structures. In addition to the aforementioned 3D configurations that utilize charge-trapping devices, a 3D flash architecture that adopts an FG device was recently developed,[83] as depicted in Fig. 13. In spite of the superiorities

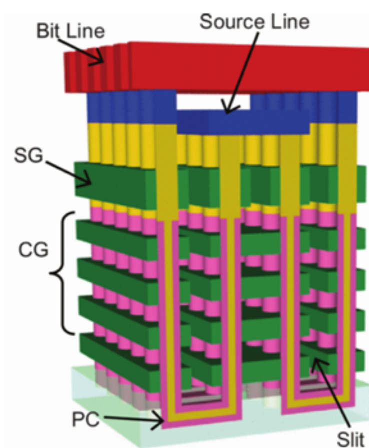

Fig. 11. A typical structure of vertical channel cell. Reprinted with permission from.[37]

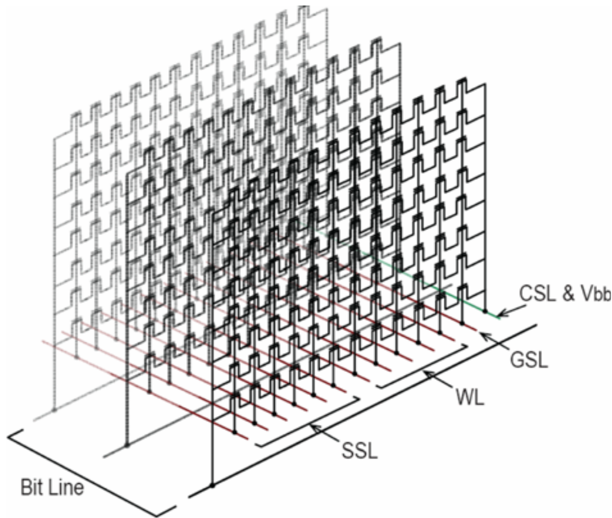

Fig. 12. A typical structure of vertical channel cell. Reprinted with permission from.[40]

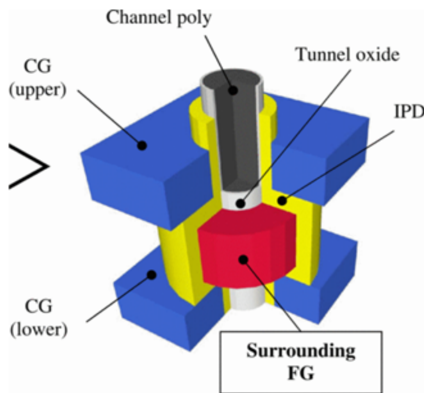

Fig. 13. Cell structure of the FG-based 3D Flash. Reprinted with permission from.[83]

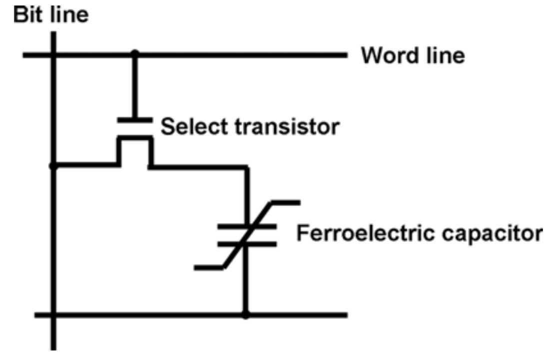

Fig. 14. Cell structure of FeRAM.

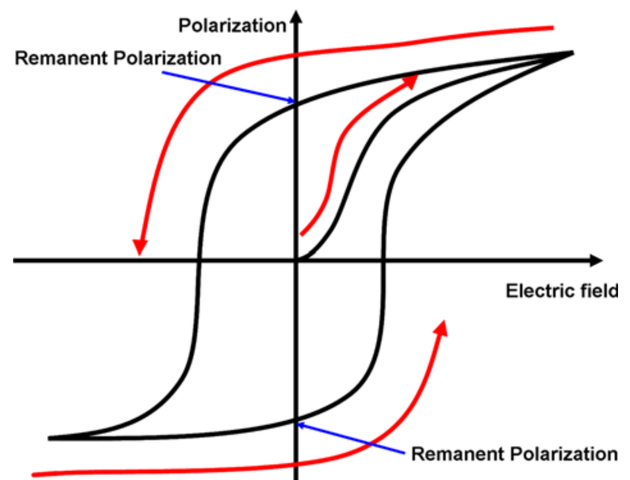

Fig. 15. Hysteretic loop of FeRAM.

of the 3D flash, it also yields considerable overhead cost because of the use of the multiple layers. In addition, the use of a charge-trapping device in 3D flash memory would make the cell susceptible to the geometric limitations to which the 2D floating gate device is subjected. Consequently, more innovative technologies are required in order to lead 3D flash memory into the 10 nm regime.[84]

3. FERROELECTRIC RANDOM ACCESS MEMORY

Ferroelectric memory (FeRAM) is one type of non-volatile memory that has a similar structure to DRAM, but which uses the ferroelectric layer instead of the dielectric layer. The unit cell of FeRAM comprises a capacitor and a transistor, and is referred to 1T1C architecture, as illustrated in Fig. 14. The storage function of FeRAM is realized by the ferroelectric material in the cell capacitor, which exhibits a non-linear relationship between the applied electric field and the stored charges. The dipole formed in the ferroelectric material when subject to an external electric field is aligned with the field direction ascribed to the small shifts in the position of atoms as well as shifts in the distributions of electronic charge in the crystal structure, while the dipole will return to its original polarization state when the electric field is removed. Such a change in the ferroelectric polarization state forms a hysteretic loop, as shown in Fig. 15, whereby the two remnant polarizations can represent binary bits. For instance, binary “0” and “1” are stored in terms of the negative polarization and the positive polarization, respectively. In FeRAM, writing is achieved by applying an external field to charge the capacitor, forcing the dipoles into the up or down orientation (depending on the polarity of the charge), thereby storing a “1” or “0”. In order to perform the reading process, the “0” state is maintained in the cell. In other words, if the cell is originally held in the “0” state, there will be no output signal. If the cell state is set to “1” then polarization re-orientation will occur and this would generate a pulse of current that is considered as the readout

signal. It is obvious that the readout process requires the cell to be overwritten, and therefore, the data must be rewritten into the cell after being read. This is known as a "destructive read".

Although flash memory has been currently dominating the market of NVMs, FeRAM has exhibited a number of advantages compared to flash memory. The most attractive feature of FeRAM is its low power consumption, which cannot be presently countered by any other NVMs. This is because FeRAM requires neither a refresh process, which is indispensable for DRAM, nor the transfer of the electrons across a high-energy barrier, which is required by flash memory. Hence, FeRAM allows for a writing voltage of less than 2 V against NAND flash, which requires a writing/erasing voltage of approximately 20 V.[85] Because of this advantage, there is no need for FeRAM to have a voltage pump-up circuit, which is required for flash memory. In addition, as the charge pump, which takes a considerable time to build up the current, is eliminated in FeRAM, FeRAM has realized a write speed of a few nanoseconds compared to flash memory, with a write speed of the order of a few milliseconds.[85] Furthermore, FeRAM has exhibited an excellent endurance of greater than 10^{14} cycles,[86-89] which is close to SRAM (around 10^{16})[86] and much longer than flash memory(around 10^5).[86] These advantages have made FeRAM suitable for radio- frequency identification (RFID), smart cards, ID cards, and other embedded memory applications such as railway passes, automobile equipment, and domestic electronic appliances.[85] Nevertheless, the difficulty experienced in downscaling FeRAM cells has significantly limited its density improvement, and is due mainly to two reasons. First, scaling down the cell size will give rise to a reduction in the amount of charge inside the FeRAM capacitor. Consequently, the sensor amplifier cannot be triggered if the amount of charge is below a given level. An additional scaling limit is that the ferroelectric material in FeRAM will lose its ferroelectric characteristic at a very thin thickness, and thus creates an obstacle for scaling up the density. As a result, improvements in the FeRAM density are relatively slow compared with that of flash memory, and the maximum capacity that is currently possible with FeRAM are 128 Mb and 4 Mb at the laboratory level[90] and industrial level[91] respectively, which is much lower than that of flash memory.

In order for FeRAM to extend scaling limits, a possible solution is to look for new ferroelectric materials. The conventional ferroelectrics such as $Pb(Zr_x, Ti_{1-x})O_3$ (PZT) and $SrBi_2Ta_2O_9$ (SBT) usually have polarization in the range 20 - 35 $\mu C/cm^2$,[86] and this would further compress the scaling space left for FeRAM. In this case, it is possible to replace PZT or SBT with $BiFeO_3$ (BFO)[92,93] to enhance the FeRAM density, considering that a polarization value of BFO is more than twice that of PZT. Besides BFO, H_fO[94,95]

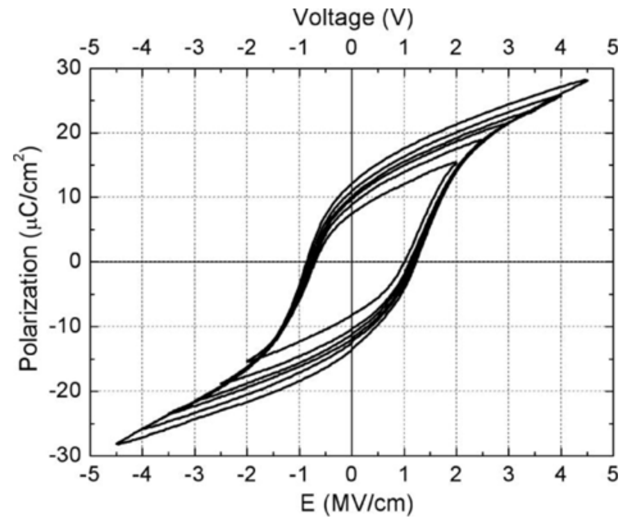

Fig. 16. Ferroelectric hysteresis curves of 10 nm thick HfO_2 doped with silicon. Reprinted with permission from.[94]

has recently exhibited the potential to bring FeRAM into the gigabit era. The ability to provide gigabit density using a 10 nm thick H_fO film has been demonstrated according to its corresponding ferroelectric hysteresis loop, as shown in Fig. 16.[94] In addition to H_fO, $(Bi, La)_4Ti_3O_{12}$ (BLT) is also a prospective candidate for future FeRAM materials.[96,97] In terms of the cell structure, the accepted FeRAM architecture that is currently employed to realize a higher recording density is to utilize the 3D capacitor, which exhibits a large area without the need to increase the lateral cell size to obtain the required polarization to retain the signal strength. In this context, it is reasonable to propose that the density of FeRAM can be further alleviated by introducing higher-quality ferroelectrics into a 3D capacitor. Recently, 3D ferroelectric nanocapacitors have been successfully fabricated,[98,99] but the capability of these 3D capacitors to have a uniform ferroelectric film thickness with a high aspect ratio remains in doubt.[86] Another approach to increase the capacity of FeRAM is to change the traditional capacitor-type FeRAM to the transistor-type FeRAM[100-104] where the gate insulator in a conventional MOSFET is replaced with a ferroelectric insulating layer, which is also called Fe field-effect transistor (FeFET) RAM. As ferroelectricity behaviour has been identified in a variety of doped and polycrystalline HfO_2, considerable research efforts have been recently devoted to the development of the HfO_2-based FeFET[101-103,105,106] using standard high-k metal gate (HKMG) processes. The most prominent advantage of FeFET over the conventional FeRAM is that the physical thickness of the gate stack can be significantly reduced, thus allowing for an improvement in scalability.[104] The ability to exhibit a promising write speed (down to a few ns), long endurance (up to 10^{12} cycles), and MLC using FeFET has already been demonstrated and a 64 KB SBT-based FeFET array has been fabricated.[107] The

FeFET RAM is able to provide a density that is comparable to that of flash, and it was therefore proposed as a replacement for NAND flash in the technology node below 16 nm. However, the short retention time of FeFET RAM has severely handicapped its potential as a total replacement for NAND flash, and can be hardly alleviated when scaling below 16 nm, because of the tradeoff between the thick Fe layer required for data retention and the thin Fe layer required for extreme scaling to and below 16 nm.[104] Recently, organic ferroelectrics such as polyvinylidene fluorides (PVDF),[108] have received more attention because of the advantages of simplicity, large-area fabrication, non-toxicity, and flexibility when they are made on flexible substrates such as polymers,[109,110] graphene,[111,112] and carbon nanotubes (CNTs).[113] However, the drawback can be attributed to the low spontaneous polarization and high gate leakage compared to their inorganic counterparts. The presence of some molecular-based ferroelectrics,[114-116] which gives high values of the spontaneous polarization, may be considered as a potential solution to this problem.

4. MAGNETIC RANDOM ACCESS MEMORY

Magnetic RAM, which is derived from an observation of the tunnel magneto-resistance (TMR) effect, is considered to be a possible contender to compete with other RAM devices. The TMR effect occurs in a magnetic-tunnel junction (MTJ) that consists of a thin insulator sandwiched by two ferromagnets, as illustrated in Fig. 17. The magnetization directions of these two ferromagnets can be switched by an external magnetic field. If the two magnetizations are in a parallel orientation, the electrons are more likely to tunnel through the insulating layer compared to the case with anti-parallel magnetizations. Hence, the MTJ can be switched between a high resistance state and a low resistance state depending on the resulting magnetization orientations. Because of the TMR effect, the memory cell of MRAM consists of a single-pass transistor for the selecting bit during readout, and an MTJ that comprises a thin tunnel barrier such as MgO sandwiched by two ferromagnetic layers, as shown in Fig. 18. One of the ferromagnetic layers whose magnetization is pinned along one orientation is called a fixed layer, and the other in which the magnetization can be readily rotated is called a free layer. The resistive state of MRAM depends extensively on the relative orientation of magnetization between the free layer and the fixed layer, as the parallel magnetization directions between these two layers result in a low cell resistance, while anti-parallel magnetization leads to a high resistance. According to the designed structure, the writing operation in MRAM is performed by applying a current pulse to two perpendicular lines (bit line and digit line) to reverse the magnetization of the free layer at the line intersection at which the MRAM

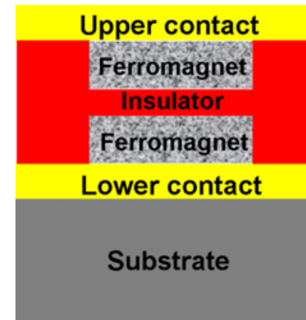

Fig. 17. Diagrammatic structure of a MTJ.

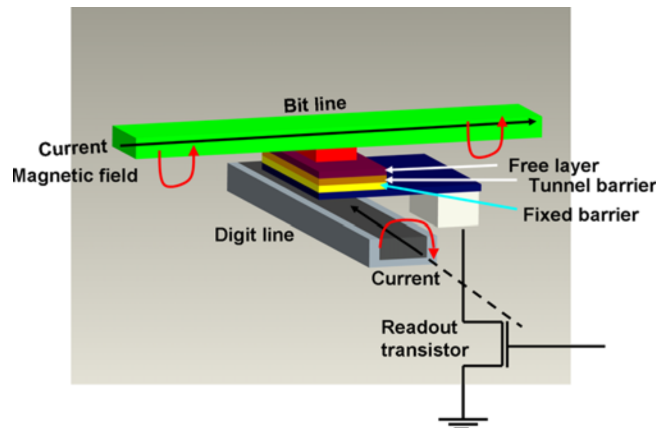

Fig. 18. Cell structure of MRAM.

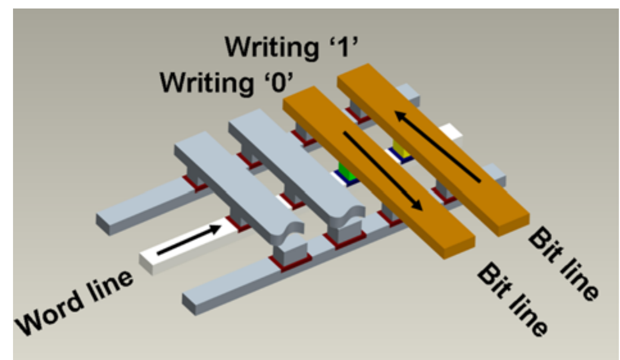

Fig. 19. Writing mechanism of MRAM using MTJ.

cell is located, which is illustrated in Fig. 19. During the read process, the selected transistor is turn on and a bias voltage is applied to the cell to determine its state by measuring the amount of current flowing through the cell.

As the readout process is mainly ruled by the TMR effect, the TMR ratio, i.e., the ratio of the resistance of MTJ in the anti-parallel state to that in the parallel state, becomes a very critical parameter to determine the performance of MRAM. The theoretical possibility to achieve a TMR ratio of 1000% using a fully crystallized Fe/MgO/Fe MTJ was first proposed

in 2001.[117,118] In 2004, a TMR ratio of 88% at room temperature for fully epitaxial Fe/MgO/Fe MTJ and a ratio of 220% at room temperature for a highly oriented (001) CoFe/MgOCoFe MTJ deposited by sputtering were demonstrated experimentally.[119,120] Excited by the above accomplishments, a TMR ratio of 230% at room temperature for sputtered $Co_{60}Fe_{20}B_{20}$/MgO/$Co_{60}Fe_{20}B_{20}$ MTJ and a ratio of 260% for $Co_{40}Fe_{40}B_{20}$/MgO/$Co_{40}Fe_{40}B_{20}$ MTJ were subsequently revealed,[121,122] and they were deposited with a standard spin-valve structure with an antiferromagnetic (AFM) layer on a thermally oxidized Si wafer using a conventional sputtering machine. TMR ratios of more than 600% at room temperature and of 1100% at 5 K using a pseudo-spin-valve MTJ were recently demonstrated.[123,124]

The most attractive characteristic of MRAM is its extremely fast operation speed, which falls into the sub-ns regime.[125] This is well below that of DRAM and flash, and is even comparable to that of SRAM. In addition, MRAM has little degradation even after a large number of write/read cycles, and thus presents a much better endurance ($>3 \times 10^{16}$) feature than flash.[86] Nevertheless, density-scaling limits presently pose a formidable barrier that prevents the large-scale production of MRAM in the semiconductor market. According to Fig. 18, MRAM makes use of an additional metal line (digit line) for writing, and consequently leads to a large cell area factor, which restricts the density of MRAM. Moreover, as the switching field is approximately inversely proportional to the cell size, a larger field is required when further scaling down the MRAM cell,[126] causing additional power consumption in accordance with reliability issues arising from electron-migration phenomenon in metal lines. Besides, along with the decrease of the cell size, the cross-talk effect, where the magnetization of one MRAM cell may be affected by the adjacent cell because of the short distance between these two cells will become more evident, which may increase the programming error rate. For the above reasons, MRAM has currently been limited into embedded memories such as drive recorders where the density is not the primary concern,[85] and it may also be a satisfactory space memory if it fulfils the temperature-range requirements.[126]

To date, thermal-assisted switching (TAS)[127-130] and spin-transfer torque switching (STT)[131-136] are regarded as two prospective ways for MRAM to eliminate programming errors and reduce the switching field. TAS is based on the heat- assisted magnetic recording (HAMR) concept,[137] where the current is injected through the MTJ to generate Joule heating in order to lower the magnetic anisotropy of the free layer during the write process, thus decreasing the switching current as well as the power consumption. A TAS-MRAM with 2 bits per cell beyond the 65 nm technology node has already been demonstrated.[138] However, more attention has recently been given to the STT MRAM (STT-MRAM) because of its ability to offer the fast speed of SRAM, the capacity and cost of DRAM, and the non-volatility of flash in conjunction with the approximately unlimited endurance.[132] The fundamental physics behind STT is that when applying a current through a magnetic layer, the spins of electrons that constitute the current will be aligned to the magnetization orientation, which is known as spin-polarization, and these spins can be repolarized if such a spin-polarized current is directed into another magnet. During the repolarization process, the magnetic layer is subjected to a torque that can stimulate spin-wave excitations or flip the magnetization direction of the magnetic layer at sufficiently high current density.[139] According to this mechanism, the STT-MTJ can be switched between a low resistance state and a high resistance state using the spin-polarized current that is induced between the fixed layer and the free layer. The cell structure shown in Fig. 20(a) shows the switching of STT-MTJ from the anti-parallel orientation to the parallel orientation. In order to induce such a switching, the electrons should flow from the pinned layer to the free layer. The electrons that have the same spin direction as that of the magnetization in the pinned layer would remain to form the spin-polarized current after they cross through the pinned layer. Subsequently, this spin polarized current flows through the free layer that is subjected to the torque that results from the spin- angular momentum of the polarized current. This enables the magnetic state of the free layer to be changed if the torque is sufficiently strong, compared to that of the threshold value. To achieve the switching from the parallel orientation to the anti-parallel orientation shown in Fig. 20(b), the electrons should flow from the free layer to the pinned layer. Once the electrons reach the pinned layer, the electrons with the same spin direction as that of the pinned layer would pass through the pinned layer, while the others will be reflected at the boundary between the insulator and the pinned layer, and bounced back to the free layer. This reflection would produce the spin transfer torque on the free layer and switch the magnetization of the free layer when it exceeds the threshold value.

As the write operation in STT-MRAM is achieved by applying a current through the magnet itself rather than by generating a very strong reversal field, it is advantageous for STT-MRAM to offer lower power consumption than the conventional MTJ counterparts. Besides, STT-MRAM no longer required an additional metal line as the current path, thus resulting in better scalability. Based on the physical origin of the free layer magnetization, STT-MRAM is categorized into an in-plane MTJ, where the magnetization of the ferromagnetic layers lies in the film plane, and a perpendicular MTJ, where the magnetization direction is perpendicular to the film plane. A much more mature technology has been employed for in-plane MTJ compared

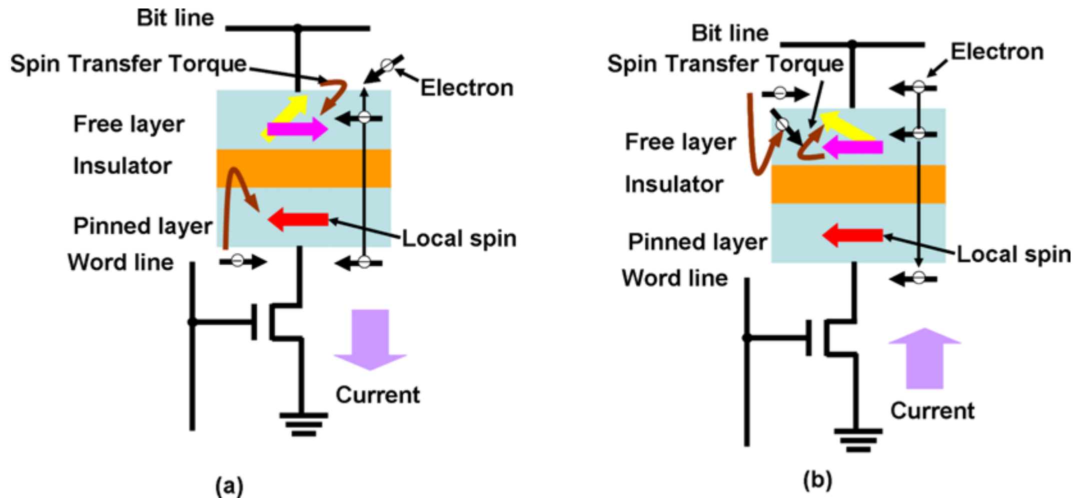

Fig. 20. Spin transfer torque magnetization switching (a) from anti-parallel to parallel and (b) from parallel to anti-parallel.

to its perpendicular counterpart, while the perpendicular MTJ is believed to contribute to lower switching current density.[133] Recently, a 1.5 Mb STT-RAM with a write speed of 10 ns and a current density of the order of a few 10^6 A/cm^2 at the 54 nm node has been demonstrated,[132] and the scaling roadmap has forecasted an outperforming of STT-MRAM over SRAM at 15 nm node.[133] The introduction by Everpin[140] of 64 Mb STT-MRAM, which is integrated with the latest technology to scale 17 nm STT-RAM current down to 40 μA, and which is compatible with the performances of CMOS transistors,[135] also provides motivation to further the development of STT-MRAM technology. A more recent innovation on MRAM technology is the presence of domain-wall racetrack memory (also known as a "virtual hard disk"), which combines the high performance and reliability of solid-state memory with the low cost of a conventional hard disk, as illustrated in Fig. 21. As can be seen from Fig. 21, information in the racetrack memory is stored in the form of a pattern of magnetic domains separated by domain walls. These domains move on the application of a spin-polarized current or an external magnetic field to the nanoscopic wire where domains are located, and the write/read functions are operated once the domains pass the fixed write/read heads. Racetrack memory avoids the need for mechanical components, and therefore provides better anti-wear characteristics and higher robustness than hard disks. One limitation of racetrack memory is the slow motion of the domain wall, which can be improved using nanosecond pulses of electric current. A domain wall moving speed of 138 m/s has already been achieved,[141,142] giving rise to a high data rate. However, there remain problems such as small crystal imperfections, which need to be solved before this technology can be used more widely. Based on the above introduction, the merits that the conventional MRAM absorbs from any other non-volatile compatriots, along with the potential that emerging

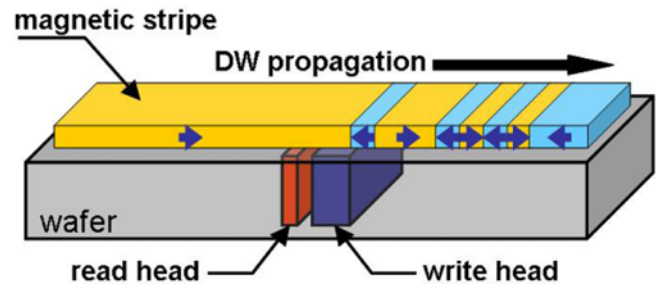

Fig. 21. Domain-wall racetrack memory.

MRAM has displayed to improve the scaling bottleneck, has made MRAM one of the promising alternatives for "universal" memory. The practicality of using MRAM to simultaneously satisfy high storage capacity, low power consumption, room-temperature operation has been recently demonstrated in theory.[143] However, the small resistance ON/OFF ratio remains a major concern for STT-MRAM.[86]

5. PHASE-CHANGE RANDOM ACCESS MEMORY

Phase-change RAM, which is also known as PCRAM or PRAM, is another type of NVMs that stores data by means of switching resistive states of phase-change materials (PCMs) between a low-resistive crystalline phase and a high-resistive amorphous phase. The PCRAM idea was first proposed by S. R. Ovshinsky[144] in 1968, after he observed a threshold switching process in thin layers of chalcogenide glass alloys. A chalcogenide is a chemical compound consisting of at least one chalcogen anion and at least one more electropositive element. However, this reversible switching behaviour was not properly understood until there were developments related to the discovery of some high-

performance PCMs as well as the booming of the semiconductor manufacturing technology over the last 10 - 15 years. Consequently, to date, we have seen a large number of technical papers on PCRAM technology associated with a large number of US patents, which implies the success and the good potential of PCRAM for the data storage industry.

5.1 Phase-change materials

It is well known that any solid substance consisting of metals, semiconductors, or insulators exist in the form of either an amorphous phase, where the atoms are not arranged in regular arrays, or the crystalline phase, where the atoms are arranged in an ordered pattern extending in all three spatial dimensions. However, only a small portion of these solids that satisfy data-storage criterions can be adopted for PCRAM applications, the properties of which require:[145]

- A large difference between the amorphous state and the crystalline state in the electrical property (resistivity) in order to extract a useable readout signal.
- A relatively low phase-transition temperature in order to reduce the power consumption, but which is high enough to provide the sufficient lifetime.
- A quick and stable phase-change transition required for fast programming.
- The ability to withstand billions of phase changes over a period of several years from an endurance point of view.
- A high scalability to maintain a cell size below tenth of nm.

Because of the stringent requirements mentioned previously, for a long time, PCM technology experienced a somewhat slow development. This was however accelerated by the revelation that when exposed to a laser pulse, metal alloys along the GeTe-Sb_2Te_3 pseudo-binary line exhibits a very large optical contrast and a very fast switching speed between an amorphous state with low reflectivity and a crystalline state with high reflectivity.[146-149] This finding has led to the application of PCMs on optical storage disks including DVD-RAM,[150-153] DVD-R/W,[154-157] and recent Blu-Ray disks,[158-161] and it has triggered the emergence of a new memory device using PCMs, so called PCRAM. It should be noted that most of the PCMs used today are chalcogenide-based alloys that contain chalgogenide elements (O, S, Se, Te, Po) in Group VI of the periodic table. Chalcogenide alloys have a large resistivity difference between the amorphous and crystalline states, which can be up to five orders of magnitude for some materials,[162] therefore leading to a detectable readout signal. In addition, the ability to realize data retention for 10 years at 85°C using chalcogenide alloys has been demonstrated, making PCM suitable for embedded memory applications.[163,164] Moreover, the crystallization time of the chalcogenide alloys for ultrascaled devices can be reduced to 1 ns[165-167] and a recent publication has even reported an observation of a 1 fs crystallization behaviour on $Ge_2Sb_2Te_5$;[168] this indicates a very fast programming speed. As a result, such a unique integration of all the aforementioned properties has made chalcogenide-based alloys the most successful PCMs for PCRAM applications.

Chalcogenide alloys are usually classified into three main families: Te-based eutectic alloys, GeTe-Sb_2Te_3 pseudo-binary materials, and Sb eutectic alloys,[155] as shown in Fig. 22. In general, Te-based eutectic alloys, which include $Ge_{15}Te_{85}$, show a highly stable amorphous state at room temperature at the expense of a fast crystallization rate,[155] whereas pseudo-binary line GeTe-Sb_2Te_3 alloys give a fast recrystallization

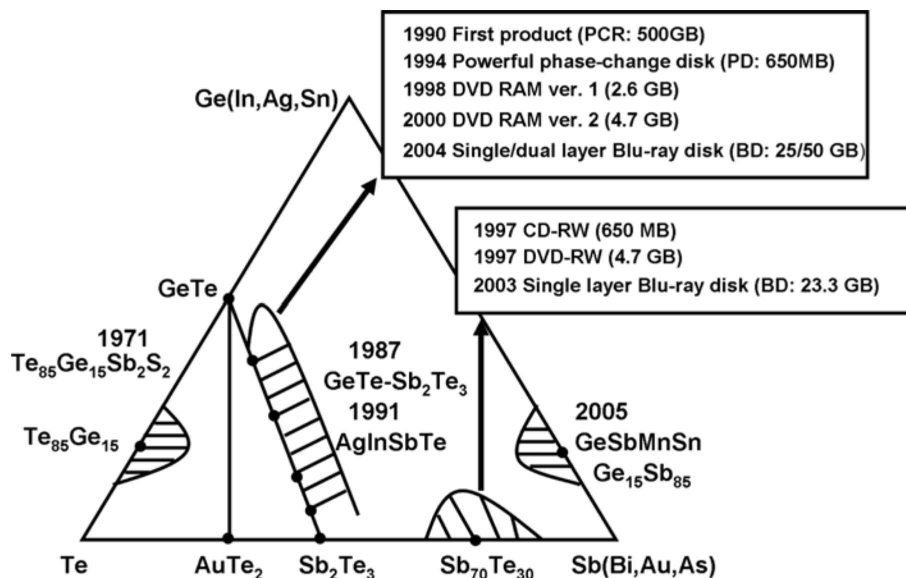

Fig. 22. Schematic phase diagram depicting different PCMs. Reprinted with permission from.[155]

and a remarkable optical contrast. In addition, the difference in the electrical resistivity of $GeTe-Sb_2Te_3$ alloys between the crystalline phase and the amorphous phase may be more than three orders of magnitude.[169] Therefore, $GeTe-Sb_2Te_3$ compounds such as $Ge_2Sb_2Te_5$, GeSbTeN, GeSnSbTe, GeBiSbTe, GeBiTe and GeInSbTe,[146,147,170-174] have been considered as types of PCMs for applications to PCRAM. It should also be noted that $Ge_2Sb_2Te_5$ (GST) is the most widely used material within the $GeTe-Sb_2Te_3$ pseudo-binary line, and is regarded as the "gold standard" of PCMs against which other alloys are often compared. Sb eutectic alloys,[175-178] which mainly comprise the doped SbTe compounds such as $In_x(Sb_{70}Te_{30})_{1-x}$ and $Ag_xIn_y(Sb_{70}Te_{30})_{1-x-y}$, are considered as fast-growth materials whose crystallization occurs from the boundaries between the amorphous mark and the surrounding crystalline matrix because of the low nucleation probability of the doped SbTe material. Therefore, the resulting crystallization is dominated by the subsequent growth of the crystalline-amorphous interface.[179] Differing from the doped SbTe, the chalcogenide alloys located in the $GeTe-Sb_2Te_3$ line exhibit a nucleation-driven crystallization mechanism, where crystallization usually starts with some small, unstable clusters inside the amorphous state, and some clusters eventually grow to a critical size beyond which they are stable and thus become crystallites.[180,181] It is evident that the use of growth-driven crystalline materials would allow for a fast switching speed and a high retention temperature at the cost of a poor cycle endurance and a low resistance ratio[182] compared to the nucleation-driven compatriots. Figure 23 shows the difference between these two crystallization mechanisms.

5.2 Operations of PCRAM devices

Figure 24 illustrates the schematic representation of a conventional ovonic unified memory (OUM) PCRAM cell,[182] also known as a Lance-like structure. As can be seen from Fig. 24, the PCM that is generally considered as a GST is sandwiched between the top metal electrode and a resistive electrode (also called a heater), which is encapsulated by a thermal insulator. Programming is induced by applying a current vertically from the bottom electrode to the top electrode via the heater and the PCM. Such a current brings about Joule heating inside the PCM, whose phase can be switched at the heater/active chalcogenide interface where a "mushroom"-like phase-change volume is formed because of the resulting high current density. The reading in PCRAM is achieved by applying a low voltage and by sensing the current through the cell. Phase transformations in the PCRAM device from either the amorphous state to the crystalline state or vice versa can be accomplished by adjusting the characteristics of the applied current pulse. To produce the amorphous phase, a high-current pulse heats up the programmable volume of the PCM to the melting temperature, followed by a rapid cooling that turns the undercooled molten material into the amorphous phase with a high resistance. This is called the RESET state. In this case the mobility of the atoms is too low to allow for a structural change at a temperature significantly below the glass-transition temperature. Hence, the atomic structure of the GST volume presents a state that lacks a long-range translational order, i.e., the amorphous phase. To recover the crystalline phase, the temperature inside the amorphous GST

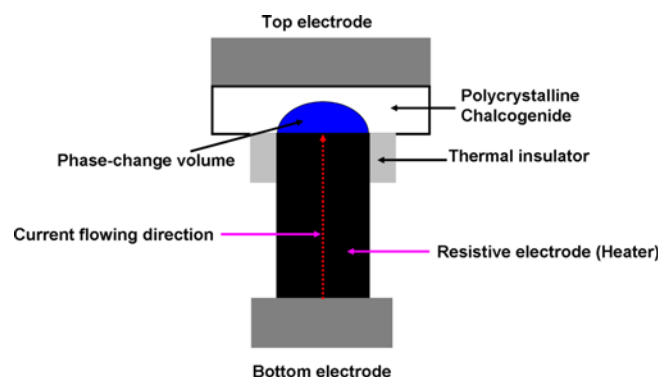

Fig. 24. The cell structure of the OUM PCRAM.

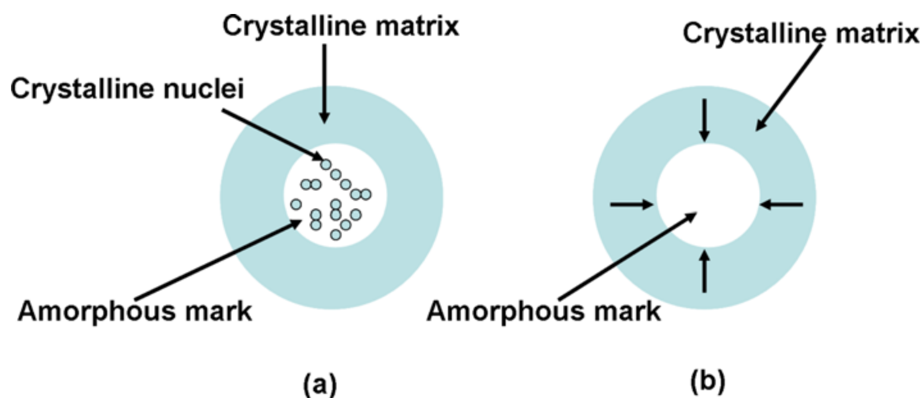

Fig. 23. Crystallization behaviour of PCMs based on (a) nucleation-driven mechanism and (b) growth (interface)-driven mechanism.

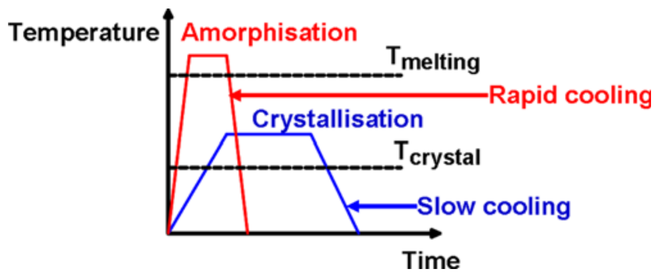

Fig. 25. Principle of electrical probe memory using phase-change materials. T_m is the melting temperature and $T_{crystal}$ is the crystalline transition temperature.

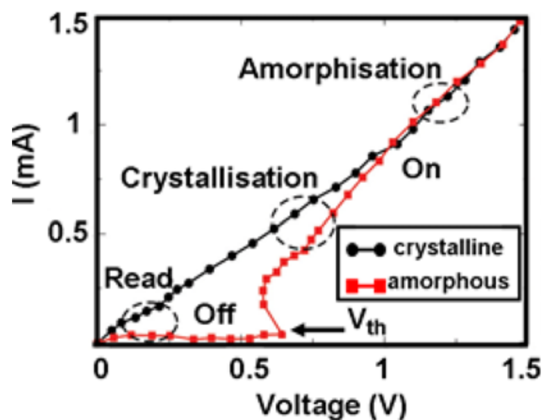

Fig. 26. Threshold switching phenomenon observed in PC-RAM device. V_{th} is the threshold switching voltage, and I represents the resulting current. Reprinted with permission from.[188]

needs to be increased above the glass-transition point, but below the melting one, resulting in a high atomic mobility. This would yield a phase transition back to the energetically more favorable crystalline phase or the SET state. Figure 25 shows the thermal switching characteristics of a PCRAM cell. It should be noted that unlike covalent semiconductors whose amorphization does not change the local ordering, the amorphization of GST material induces a pronounced variation on the local ordering as well as a substantial change on the physical properties.[155,183-185] This local-order variation was proposed as a flip of the Ge atoms from an octahedral position into a tetrahedral position without the rupture of strong covalent bonds.[186,187] Such a transition is assumed to be responsible for not only the significant change of the physical properties such as optical reflectively and electrical resistivity, but also the fast performance and repeatable switching over millions of cycles.[187,188]

In addition to the thermal switching, PCRAM has also exhibited a unique electrical switching characteristic, called "threshold switching", as shown in Fig. 26. Figure 26 clearly reveals that PCRAM memory in the amorphous phase can range from a high resistivity state (of the order of several MΩ) (OFF state) to a low resistivity state (of the order of a few kΩ) (ON state) when increasing the bias voltage. This transition occurs in the form of an appearance of a "snap back", as the bias reaches a characteristic voltage referred to as the threshold voltage, V_{th}. Threshold switching plays a key role in determining crystallization kinetics, as it allows a high current density in the amorphous state without the application of large write voltages. Without such a switching mechanism, which enables large currents to flow in the amorphous material at low voltages (~a few V), a very high voltage (~100 V) would be required to switch the material, effectively making electronic programming non-practical.[187] While threshold switching is one of the most important features of PCM, the fundamental physics behind threshold switching remains controversial, and several models have been proposed to investigate the mechanism of threshold switching. A thermal model was first proposed to attribute threshold switching to thermal breakdown in the amorphous film.[189] However, as more evidence subsequently revealed that threshold switching is a purely electronic effect as opposed to a thermal effect,[190,191] an electrical model that ascribed the threshold switching to the balance between a strong Shockley Reed Hall (SRH) recombination through trap levels and a generation mechanism driven by both electric field and carrier densities has emerged.[192] Meanwhile, the cause of threshold switching in another electrical model was explained using trap-limited transport theory.[193] Differing from the above models, a crystallization model owes the origin of threshold switching to the field-induced nucleation of conductive cylindrical crystallites.[194] As material parameters and experimental environments are different within these models, the physical reality of these models still need to be further verified, thus necessitating the exploration of more plausible models.

5.3 Scaling of PCRAM device

It should be noted that both SET and RESET states of PCRAM are usually achieved by a current pulse generated by a cell-selection device. Hence, each PCRAM cell actually consists of a phase-change element and a cell selector. The MOSFET is probably the most widely used cell selector for memory integration in CMOS technology.[195] However, due to its limited current drivability, a MOSFET with a larger size is required in order to provide a sufficiently high RESET current for amorphization; this will severely impair the scalability of PCRAM cell. Therefore, realizing a reduction in the programming current is a very important technical criterion for PCRAM in order to achieve a high areal density as well as low power consumption. To realize this target, several PCRAM cell architectures have been proposed, and they fall into three main categories: devices where scaling is achieved by reducing the contact area, devices where scaling is achieved by reducing the size of the PCM itself, and other miscellaneous device structures.[162]

5.3.1 PCRAM scaled by reducing the contact area

The aforementioned Lance-like PCRAM cell presented by Intel-Ovonyx using 180 nm COMS technology[182] is not only the simplest PCM structure, but also the predecessor of various types of recently reported PCRAM devices, whose feature size is significantly limited by the lithographic and process capability. As a result, the requirement to minimize the heater/PCM interface under the sub-lithographic regime triggers a variety of many novel cell structures where scaling is secured by decreasing the contact area of the heater with PCM material. One example is the edge-contact cell structure.[196] As shown in Fig. 27, the edge-contact cell adopts a conductive liner as a heater to concentrate the volume of Joule heating, allowing for a very low RESET current of 200 μA at the expense of a large layout area and reduced writing endurance. Subsequently, a cell structure, called a "μTrench" structure, which was presented by STMicroelectronics, demonstrated the ability to reduce the programming current to 600 μA using 180 nm technology[197] and 400 μA using 90 nm technology, respectively.[198] The contact area of the μTrench cell shown in Fig. 28 is defined by the intersection of the thin vertical heater and the trench (μTrench) where the PCM is deposed. Further, owing to its particular structure, the heater/PCM interface is far more stable than that of the edge-type cell, thus leading to a write endurance of up to 10^{12} cycles.[198] However, it should be noted that although the μTrench cell can offer a low programming current and high write endurance, its contact area between the PCM and the heater still suffers from the lithographic limits. Another novel cell structure derived from the μTrench is the "ring" cell.[199] The ring cell in Fig. 29 acquires a ring- shaped contact area between the heater and the PCM by depositing a thin metallic layer cover by oxide in the lance contact, subsequently followed by planarization and PCM deposition. Through this mechanism, the shell thickness plays a more important role in determining the contact area than the contact diameter. Similar to the μTrench cell, the benefit of this ring design is its small contact area, while the main drawback is the difficulty in fabricating such a structure. Accordingly, an improved

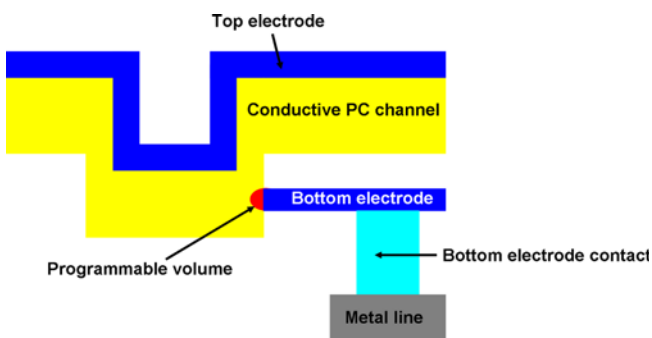

Fig. 27. Edge-contact PCRAM cell.

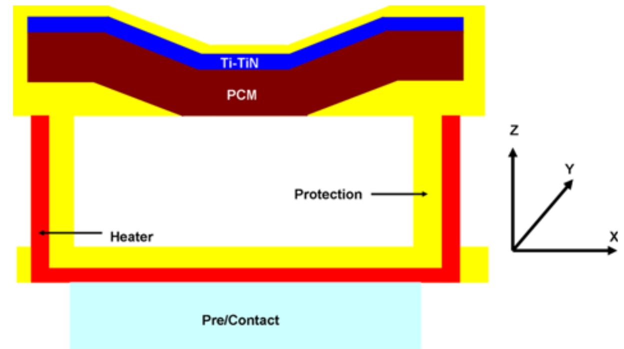

Fig. 28. Cross sectional structure of 'μTrench' PCRAM cell along x direction.

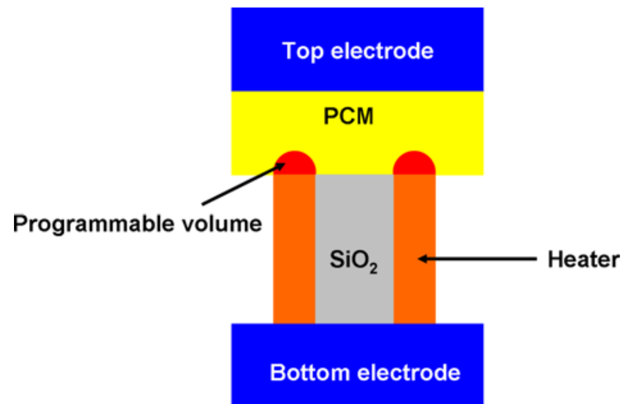

Fig. 29. Ring shaped PCRAM cell.

version of a ring cell has been introduced to avoid recessed core dielectrics inside the contact hollow, giving a reset current of around 450 μA for a patterned 60 nm diameter contact hollow.[200]

5.3.2 PCRAM scaled by reducing the size of PCM itself

An alternative method of reducing the reset current is to reduce the volume of the PCM, which has been demonstrated by the "pillar" structure,[201] as shown in Fig. 30. The key component of the pillar structure is the small cylindrical chalcogenide bar, which is called a pillar, and is built from the resist trimming and the pillar etch, followed by a deposition of the oxide isolation and the formation of the contact electrode. Using the pillar cell enables a low reset current of 900 μA for a 75 nm diameter cell using 180 nm CMOS technology.[201] However, realizing the etching process for the pillar cell is very challenging. The volume of the PCM can be scaled down by another cell structure, called line PCRAM,[202] where the PCM is fabricated in the form of a "line" shape to connect two adjacent electrodes at either side of the active material line. It was claimed that this cell offers a low programming current because of a better thermal insulation performed by the active material instead of the metallic heater, but the horizontal layout is unsuccessful

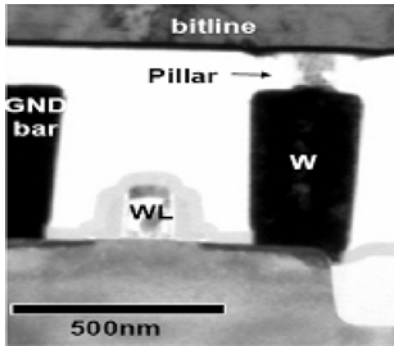

Fig. 30. Pillar PCRAM cell. Reprinted with permission from.[201]

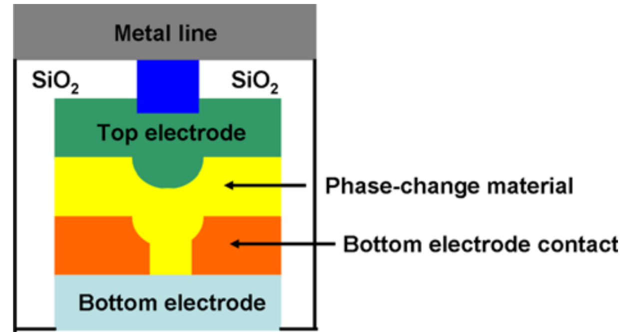

Fig. 32. 'Pore' PCRAM cell architecture.

in terms of the device size.[203] The "bridge" architecture,[204] which is similar to the "line" structure, is another lateral cell with a thin phase-change bridge connecting the two electrodes by crossing a dielectric layer that separates these two electrodes. The ability of the phase-change bridge cell to offer a reset current of 80 μA at a cross section of 60 nm^2 has been verified.[204] Fig. 31 shows the architectures of the line cell and the bridge cell, respectively.

5.3.3 Other miscellaneous PCRAM cells

It should be noted that in addition to the cells introduced above, there are other PCRAM cell structures available today, which mainly include the "pore" type, cross-spacer type, and dash type. "Pore" architecture is a typical representative of these cells, which lowers the reset current by recessing the bottom electrode.[205] The pore device shown in Fig. 32 has a metal layer as the top electrode above the PCM, which is confined into a pore that is etched through an insulator to another metal layer as the bottom electrode. By precisely defining the pore diameter, a reset current of less than 250 μA with a patterned 40 nm diameter has been achieved for a pore cell;[206] however, it involves a more complex fabrication technique. The strategy of the cross-spacer PCRAM structure illustrated in Fig. 33 is to

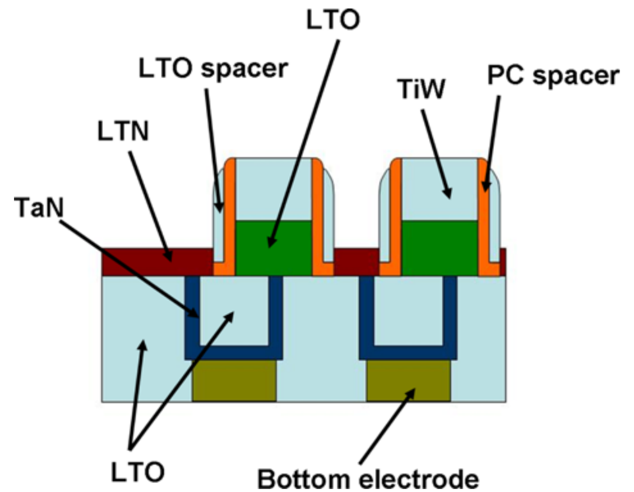

Fig. 33. Cross-spacer PCRAM cell architecture.

generate an ultra-small lithographic-independent contact area by substituting the thickness of both the PCM and the low-temperature oxide-spacer sidewalls for a μTrench width.[163,207] As the cross-spacer cell can scale both the electrode and the PCM to a smaller size, the ability to obtain a low reset current of 80 μA using 180 nm technology has been proven.[207] Furthermore, the dash cell in Fig. 34,[208,209]

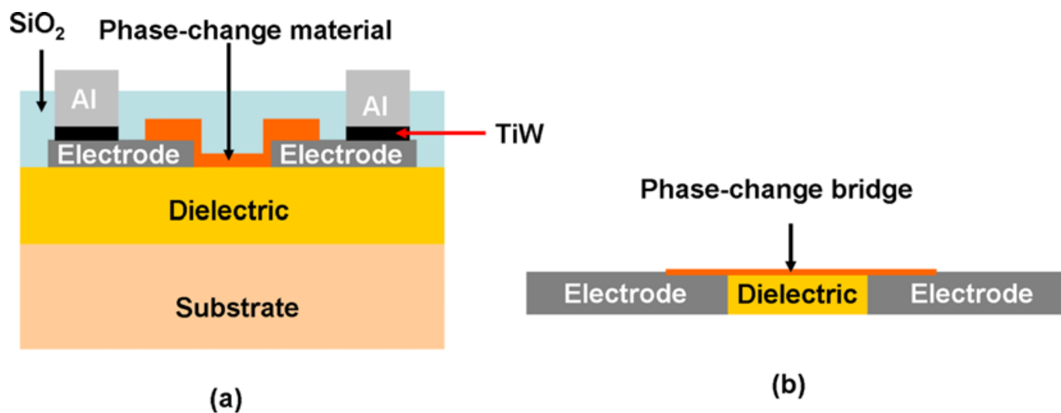

Fig. 31. PCRAM cell using (a) line structure and (b) bridge structure.

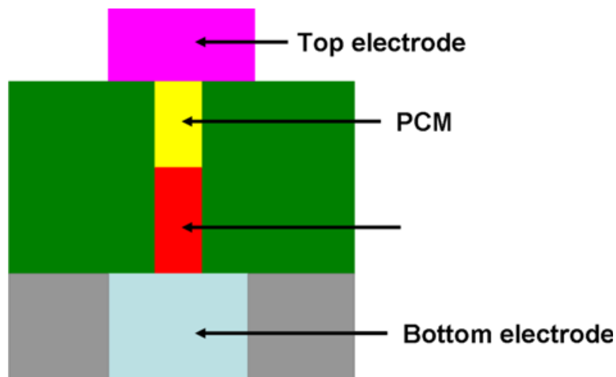

Fig. 34. Dash type PCRAM cell architecture.

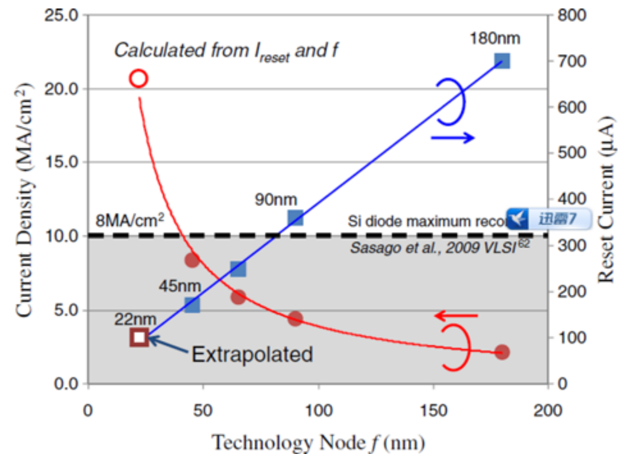

Fig. 36. Scaling of reset current by miniaturization of m-trench PCRAMs. Calculated current densities are also plotted. The grey area corresponds to a current density less than 8 MA/cm^2, which is the maximum tolerable values of a silicon diode.[210] Reprinted with permission from.[211]

which is produced from a combination of the chemical vapor deposition (CVD) of a chalcogenide material with the double-cutting process in a slit with a 7.5 nm width and 30 nm depth, has enabled a reset current of 160 μA using sub-20 nm technology.[208] More recently, a highly integrated 3D cross-point PCRAM device that comprises a phase-change cell and a poly-Si diode has been proposed,[210] as shown in Fig. 35. It was found that the maximum current density that the poly-Si diode can provide is around 8MA/cm^2, which further proves that reducing the reset current is the most important prerequisite for PCRAM to cross the gigabit density barrier. The feature size as a function of both current density and reset current is schematically shown in Fig. 36. According to Fig. 36, the reset current needs to be sustained below 100 mA in order to attain a 20 nm feature size. However, this would result in a current density greater than 20 MA/cm^2, which is beyond the limit that can be withstood by the metal wire. Consequently, if poly-Si diode is chosen as the cell-selection device, the maximum reset current needs to be restricted below 32 mA in order to obtain a 20 nm feature size.[211] Besides the aforementioned PCRAMs, another PCRAM that replaces the bulk chalcogenide with a super-lattice of thin chalcogenide layers having a different composition has previously been investigated.[212] Because of the low thermal conductivity of the super-lattice-like structure, a phase-change switch can be induced without melting, thus allowing for lower programming current and fast working time.

The advantages of PCRAM, which includes good scalability, high speed, high endurance, non-volatility, and cost-effectiveness, has made PCRAM the most competitive rival of flash memory. The ability for PCRAM to replace Nor flash at the 90 nm node has already been verified,[213] and an 8 Gb PCRAM at the 20 nm node has recently been released,[214] which is comparable to the state-of-the-art NOR flash technology (8 Gb at 45 nm). Moreover, the scalability of PCRAM device to <5 nm has recently been demonstrated using carbon nanotubes as electrodes,[215,216] and a cycling endurance of 10^{11} was also reported.[217] Nevertheless, the capacity of PCRAM still lags behind the most advanced NAND flash chip (128 Gb at 20 nm) because of the tradeoff between the high programming current and the limited current drivability of the cell selector. Consequently, various cell structures have been proposed to reduce the programming current. In addition to those cells introduced above, the PCRAM density can be further increased by using either a multi-level cell (MLC) or 3D stackable memory. As PCM exhibits a very high resistance ratio between the amorphous

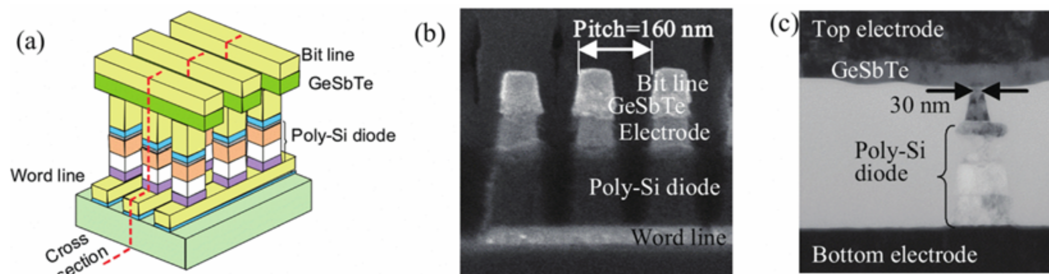

Fig. 35. Cross-sectional views of phase change memory array. Reprinted with permission from.[210]

state and the crystalline state, it is possible to classify the resistance of the cell into different levels in a continuous manner to correlate different numerical values, through which doubling or multiplying bits stored in the same cell can be achieved. A 4-level cell in a 32-kbit array with <8 iterative programming steps has been demonstrated.[218] One important criteria that the MLC needs to fulfill is that all levels should remain separated well from each other even with GB-size chips, after many cycles and for years of operation.[163] However, this cannot be achieved by the PCM because of its long-term resistance drift that is governed approximately by a power law,[219] severely limiting the MLC reliability. Therefore, further development of the MLC is required in order to fully satisfy the stringent criteria. The concept of the 3D stackable memory that implements a multilayered structure, where multiple layers of the memory elements are stacked above each other,[163] stems from the cross-point architecture idea that the memory cell comprises a top electrode connected to the column metal (bit line), the PCM, and a bottom electrode. These are deposited on a selector device connected to a row metal (word line), as shown in Fig. 37. Such a cross-point PCRAM device with a multilayered structure has been demonstrated,[220,221] whereas a realistic 3D stacked PCM memory cell is still lacking. Therefore, the ultimate solution to overcome the scaling limits of the PCRAM, either in the 2D or 3D case, is the minimization of the memory selector while simultaneously sustaining the sufficiently high-current density for programming. Several alternative memory selectors to MOSFET such as bipolar transistors,[220] PN junction diodes,[220] Schottky diodes,[222] metal-insulator-transition,[223] and ovonic threshold switch (OTS),[221] have generated considerable research interest. However, none of the current candidates can completely fulfill the requirements of the so-called "perfect" selector that has high on-state conductivity, infinite off-state resistance, and a small layout area,[163] which has led to the exploration for more innovative memory selectors.

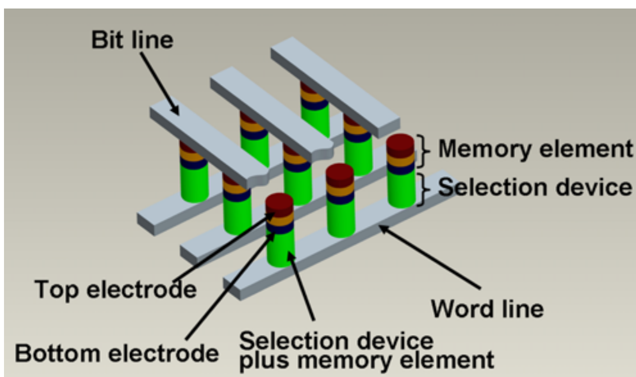

Fig. 37. Structure of the cross-point PCRAM cell.

6. RESISTIVE RANDOM ACCESS MEMORY

Binary numbers are denoted in resistive RAM or RRAM in the form of two or more distinctive resistance states. The memory cell of RRAM is generally composed of a switching layer sandwiched by two electrodes to form a metal-insulator-metal (MIM) architecture. By applying an appropriate voltage or current to the cell, the MIM can be toggled between a high-resistance state (HRS), which represents a logic value "1", and a low-resistance state (LRS), which represents a logic value "0". Such a resistive switching can be categorized as unipolar switching and bipolar switching in light of the voltage polarity. Unipolar switching that is independent of voltage polarity allows for a transition from HRS to LRS (SET process) when achieving a "set" voltage magnitude (V_{SET}), while the reversible switching from LRS to HRS (RESET process) is attained at a "reset" voltage magnitude (V_{RESET}). It should be noted that a compliance current (CC) is generally required during the SET process to protect system from permanent breakdown, whereas this is not the case for the RESET process. In contrast, bipolar switching between LRS and HRS, or vice versa, can be accomplished by applying successive electrical pulses with alternate polarities. It should be noted that some resistive switching materials exhibit a third switching behavior that has the characteristics of both unipolar and bipolar switching, called nonpolar switching.[224] Figure 38 shows various resistive switching behaviors of RRAM in terms of I-V curves.

Although reversible resistive switching was observed in various binary oxides more than four decades ago,[86,225-227] its switching mechanism has not been fully understood in spite of the advent of several hypotheses with their respective theoretical demonstrations. Therefore, further clarification of the reversible switching mechanism for the investigated resistive materials will be the first priority in order to make RRAM viable for industrial application. The remainder of this section presents a brief introduction of various resistive switching materials as well as their respective possible switching mechanism.

6.1 RRAMs using binary oxide

Although the research interest in binary metal oxides such as NiO,[228] TiO_2,[229] Nb_2O_5,[230] and ZrO_2[231] was devoted to their high-dielectric constant gate-oxide application in the early stage, the current research focus concerning binary oxides has changed to their resistive switching characteristic after the initial exploration on resistive switching materials for NVM applications. The introduction of the binary oxides into RRAM applications was initiated from a cross-point cell with a Pt/NiO/Pt structure,[232] after which a large number of binary oxides, such as TiO_2,[233-235] TaO_x,[236, 237] Nb_2O_5,[238,239] ZrO_2,[240,241] WO_x,[242-245] and MnO_x,[246,247] have been

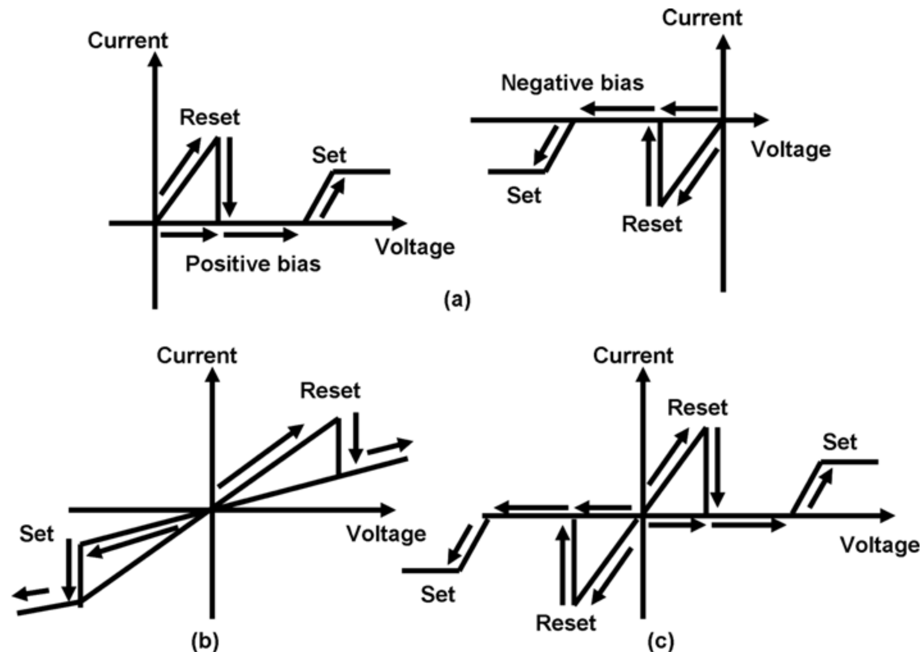

Fig. 38. Resistive-switching behaviors of RRAM devices based on (a) unipolar switching, (b) bipolar switching, and (c) nonpolar switching.

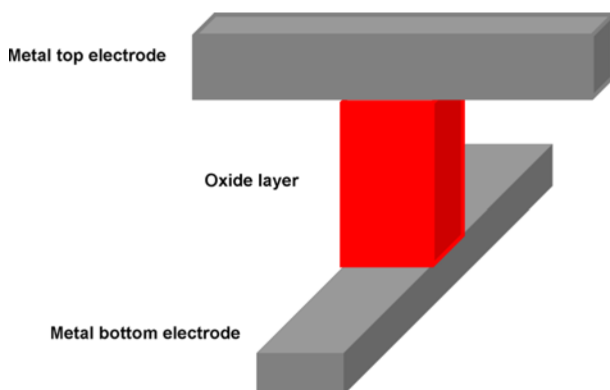

Fig. 39. Cross-point based RRAM cell.

considered as alternatives for RRAM applications. Such a cross-point cell structure is depicted in Fig. 39. The trigger of the resistive switching inside binary oxides remains unclear, but the formation and rupture of the conduction filament (CF) is regarded to be the most likely mechanism responsible for the switching. One plausible explanation for the formation and rupture of the CF is the thermochemical effect.[248] The thermochemical mechanism assumes that there is a large number of O^{2-} ions accumulated around the electrode, thus leading to the formation of oxygen vacancies. With the application of a negative bias to the top electrode, the O^{2-} ions are pushed away from the top electrode, while the oxygen vacancies are attracted towards the top electrode. In this case, the vacancy dopants drift in the electric field through the most-favorable diffusion paths, such as grain boundaries, to form a filament-like path with a high electrical conductivity.[249] Once the conductive filaments are formed, the current flow that would concentrate on the resulting filaments can trigger fast growth of these filaments because of the local heating by the concentrated current flow, which corresponds to a SET process or a switching from HRS to LRS. It is believed that the switching from LRS to HRS, i.e., the RESET process, is caused by the thermal rupture of the filaments according to the heat produced in the presence of a large current flow. In contrast to the thermochemical effect, another interpretation ascribed the occurrence of the RESET process to the disassociation of the oxygen vacancies in the conductive channel when applying a positive bias to the top electrode.[250] Such a positive bias would drive the oxygen vacancies in the conductive channel away from the top electrode to destroy the filament. In this case, the RESET process is not the outcome of the rupture of the conductive filament by Joule heating. This non-thermal RESET process associated with the aforementioned SET process is schematically shown in Fig. 40.

With the exception of a few materials such as Nb_2O_5 and TaO_x, most binary oxide operate in unipolar mode, while a novel bipolar binary oxide, WO_3, has been recently found to exhibit potential as the best-switching material because of its compatibility with the conventional tungsten structure in semiconductor devices.[86,242-244]

6.2 RRAMs using Perovskite oxides

Perovskite oxide materials such as $Pr_{1-x}Ca_xMnO_3$

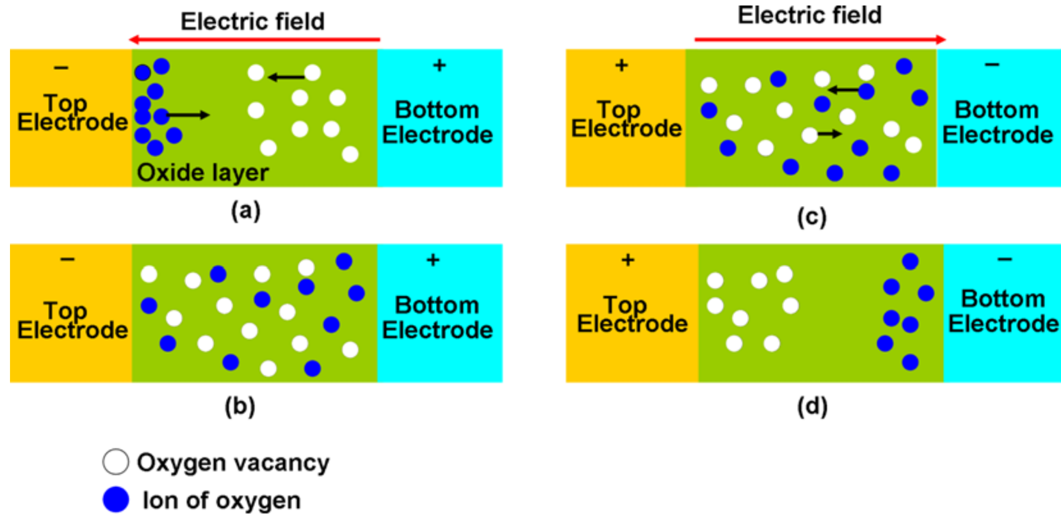

Fig. 40. Illustration of the resistive switching mechanism in bipolar oxide-based memory cell: (a) schematic illustration of the SET process, (b) schematic view of the conducting filament in the low resistance state (on state), (c) schematic illustration of the RESET process, and (d) schematic view of the conducting filament in the high resistance state (off state).

(PCMO),[251,252] $PbTiO_3$ (PTO),[253] PZT/$La_xSr_{1-x}MnO_3$ (LSMO),[254] $La_{1-x}Ca_xMnO_3$ (LCMO),[255,256] $SrTiO_3$ (STO),[257,258] and $SrZrO_3$(SZO)[259,260] have recently attracted significant interest for application to RRAM because of their inherently hysteretic I-V characteristic. SZO is the one of the perovskite oxides that was first found to have a resistive switching characteristic,[259] and this was responsible for the idea to use SZO as a storage material owing to its long retention, large ON-OFF resistance ratio, high switching speed, and low power consumption. The switching observed in SZO appears to be a generic property of the oxides in the presence of intrinsic defects that partly consist of impurities that have different oxidation states and vacancies.[259] These defects can be employed to form a series of states at various levels within the energy gap. Consequently, the charge-transfer processes via donor and acceptor levels (Cr^{3+} and Cr^{4+}) are believed to be responsible for resistive switching.[259] In addition to SZO, several ferroelectric perovskite complexes are also found to have resistive switching characteristics, such as PTO and PZT/LSMO. Resistive switching in PTO is ascribed to the ferroelectric switching that alters the carrier depletion, and consequently the conductivity of delocalized electrons,[86,251] whereas the ferroelectric-resistive switching in PZT is realized by means of the variation of the tunneling probability with ferroelectric switching.[86] As opposed to the previously mentioned members of the material family, PCMO is another perovskite-based resistive switching material that has an important magnetoresistance functionality. The switching mechanism of PCMO is reported to originate from the change of the Schottky-barrier height via the carrier capture and release process at the interface between PCMO and the electrode.[261,262] Another interface-type hypothesis attributed the resistive switching of PCMO to the space-charge-limited conduction (SCLC) that dominates the interface resistance.[263] According to the SCLC theory, the I-V characteristics exhibit an ohmic conduction in the low-voltage region, while turning to fit Child's square law when the voltage exceeds the trap-filled limit voltage.[248] As opposed to the interface-type mechanism, a filamentary conduction mechanism that forms filamentary high conductivity path in the oxide film is also believed to be responsible for the resistive switching of PCMO.[251,264] As a result, the genuine switching mechanism of Perovskite materials requires more in-depth study.

Besides the materials described above, multiferroics such as BFO have recently displayed advantageous properties as perovskite complexes that include high resistance ratio, long data retention, and CMOS compatibility with a real top electrode.[265] Nevertheless, the mechanism of multiferroics has yet to be fully understood.[86]

6.3 RRAMs using solid electrolyte

RRAM cells using solid electrolytes are also called electrochemical metallization (ECM) cells, which are composed of a thin solid electrolyte sandwiched by an electrochemically active metal electrode such as Ag or Cu, and an electrochemically inert metal electrode such as W or Pt. The switching mechanism of the ECM cell is mainly attributed to the formation and dissolution of the CF inside the ECM due to the electrochemical effect,[266,267] as shown in Fig. 41. For the SET process, the applied positive voltage will stimulate the metal ions that are generated by the oxidization (oxidization refers to the loss of an electron) of the anode metal atoms to diffuse through the solid electrolyte layer into the cathode, where they are reduced (reduction refers to the gain of an electron) back to metal atoms. Such a continuous

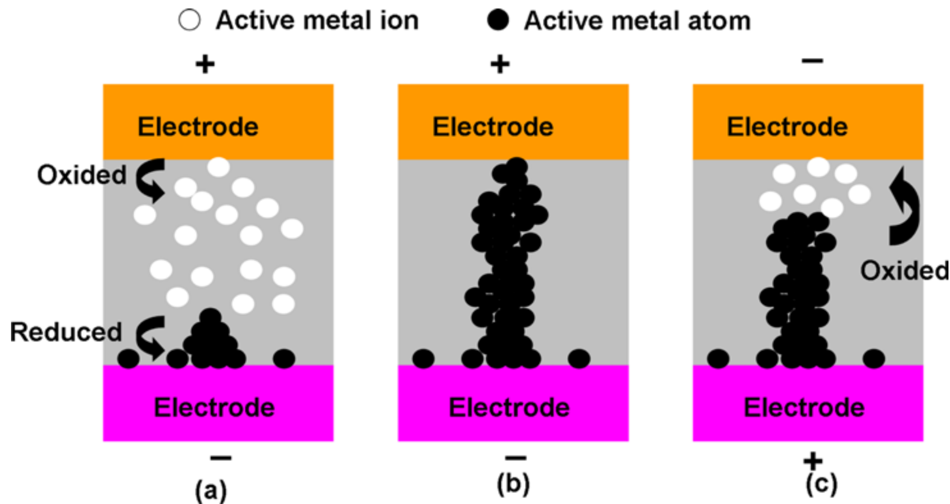

Fig. 41. (a) Electrochemically active metal atoms oxidize to ions at the anode, and then the active metal ions migrate to the cathode and deoxidize therein; (b) Precipitations of active metal atoms at the electrochemically inert electrode and finally form a highly conductive filament in the cell. (c) When the polarity of the applied voltage is reversed, an electrochemical dissolution of the filament takes place, resetting the system into HRS.

precipitation of anode metal atoms at the cathode will lead to a conductive filament to switch HRS to LRS. It is feasible to achieve the reset process by reversing the polarity of the voltage to generate an electrochemical dissolution occurring in the weakest part of the filament to switch the LRS back to HRS.

The materials used for the ECM system include chalcogenides without oxides, such as GeSe[268,269] and Cu_2S,[270] which are associated with a number of oxides e.g., HfO,[261,271] Ta_2O_5,[272] and TiO.[261,271] ECM is superior to RRAM that uses oxide in terms of the switching speed and endurance cycle, while the challenge during device fabrication in controlling the thermal stress that is caused by the large thermal coefficient of metal cations remains an issue to be resolved for ECM.[261]

6.4 RRAMs using organic materials

In addition to RRAMs that use inorganic materials, several organic materials that have small molecules,[273-277] polymers,[273,278-281] and composites containing nanoparticles (NPs)[273,282-285] also present the switching mechanism, and thus have the potential for RRAM applications. As seen in Fig. 42, four device structures have been particularly utilized by organic RRAM,[273] i.e., a single layer with only one type of organic material, a bilayer with two types of materials, a trilayer consisting of nano-traps for charge carriers sandwiched by two organic layers, and spin-cast polymer-NP blends that have a random distribution of nano-traps throughout the entire region of the host matrix. The switching mechanisms of the organic RRAM remain unclear and may vary depending on the specific material. It is believed that the resistive switching of a poly(3-hexylthiophene) (P3HT) layer sandwiched by copper and aluminum electrodes is induced by the formation of a conductive filament that is due to the migration of Cu ions into the organic layer, and this was observed by secondary ion mass spectroscopy analysis.[286] Such a conductive bridge was also found in poly(ethylenedioxythiophens).[287] In addition to filamentary-type conduction, SCLC is also responsible for the switching mechanism of some organic materials such as polystyrene (PS)+Au NPSs and poly [3-(6-methoxyhexyl)thiophene] (P30Me),[288] while the resistive switching inside the Cu-tetracyanoquinodimethane (TCNQ)[289] or a [6,6]-phenyl-

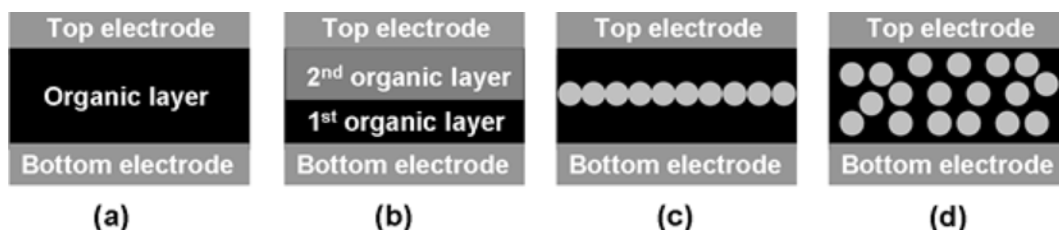

Fig. 42. Typical structures of resistive organic memory cell: (a) a single-layer structure without nanoparticles (NPs), (b) a bilayer structure containing two kinds of polymers, (c) a structure with nano-traps buried in the middle of an organic layer, and (d) a polymer-NP composite with NP raps randomly distributed throughout the entire host polymer. Reprinted with permission from.[273]

C6l-butyric acid methyl ester (PCBM) and tetrathiofulvalene (TTF) dispersed in a polystyrene matrix[290] is attributed to the charge-transfer effect. Moreover, the conducting switching mechanism of organic RRAM that uses molecular materials, e.g., the Rose Bengal molecule in supramolecular matrices of polyelectrolytes, is explained by the conformational changes in molecules or molecular bundles.[274,275] A similar switching behaviour was also observed in poly(2-(9H-carbazol-9-yl)ethyl methacrylate) (PCZ) and poly(9-(2-((4-vinylbenzyl)oxy)ethyl)-9H-carbazole) (PVBCz).[281,291] The organic RRAM has recently attracted significant interest because of its relatively low cost, flexibility, and scalability, while the short retention time and small endurance cycles severely limits its practical use.[273] Therefore, an optimization of the switching characteristics of organic RRAM is required, but it cannot be achieved until the switching mechanism of organic RRAM is fully understood.

Recent findings that include the introduction of the crossbar structure[86,292] and the selection of the proper switching and electrode materials,[86,293] together with the measurement of the RRAM switching speed using TiO_2,[86,294] have demonstrated the capability of RRAM to have ultra-high density, good stability, and fast switching speed. This enables RRAM to be considered as a favorable competitor for next- generation NVMs. To date, HfO_x and WO_x-based RRAMs have exhibited an excellent scalability below the 10 nm cell size.[295,296] In addition, the ability to generate an ultra-fast switching speed of ~100 ps has been realized for TaO_x and Pt dispersed SiO_2-based RRAMs.[297,298] Moreover, an ultra-low energy consumption of <0.1 pJ[296,299] and extremely long endurance of $>10^{12}$ switching cycles[300] have been successfully accomplished using Ni/GeO/HfON/TaN and TiN/Hf/HfO_2/TiN sandwich structures and Pt/Ta_2O_{5-x}/TaO_{2-x}/Pt RRAM cells, respectively. Furthermore, a data-retention time of up to several months and even up to 10 years has also been demonstrated both experimentally and by performing simulations using RRAMs.[301] Therefore, these encouraging findings, together with the launch of the world's smallest, full-functional HfO_2-based RRAM, which has an area of less than 10×10 nm^2 and a reliability endurance of more than 10^9 cycles, in conjunction with fast nanosecond-range ON/OFF switching times at low voltages and a large resistive window (>50), has enabled the development of RRAM technology. It has also promoted the role of RRAM in the NVM family.[296] A more exciting fact is that the recording density of RRAMs can be significantly increased with the help of MLC technology, which is analogous to PCRAM as described above. In this case, by carefully controlling the switching mechanism, the RRAM resistance can be tuned between different levels that correspond to multiple bits. One approach employed to realize such a multilevel recording is to set a variety of compliance currents, whereby four resistance states have been achieved in a Cu/Cu-doped HfO_2/Pt structure,[302] as shown in Fig. 43. Another approach for multilevel recording is to set various stop voltage during the reset process. By doing this, it is possible to obtain five resistance states in a graphene/SiO_2/graphene nanogap structure,[303] as depicted in Fig. 44. A branch of MLC technology, known as conductance quantization, has recently received considerable attention. The quantized conductance that is described as integer multiples of e^2/h (e is the electron charge and h is Planck's constant) usually occurs in a metallic wire where an atomic-scale constriction is formed by separating two electrodes that are in contact with each other.[304] As the atomic-scale conductive filament formed in RRAM cell actually connects the top electrode to the bottom electrode, the multilevel recording can be achieved if the RRAM

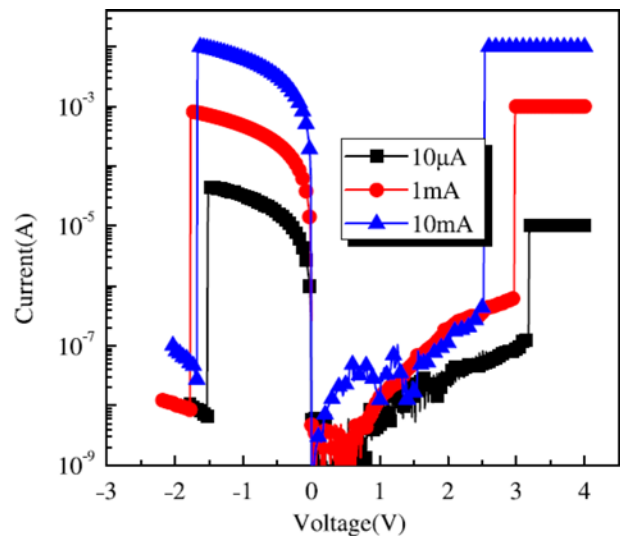

Fig. 43. Multilevel storage behaviour under various compliance currents. Reprinted with permission from.[302]

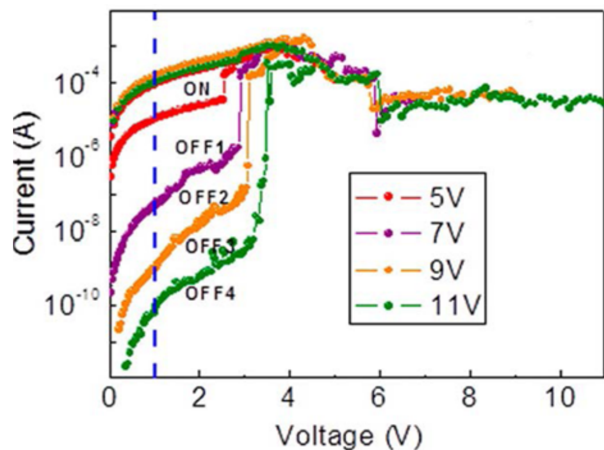

Fig. 44. Multilevel storage behaviour under various stop voltages. Reprinted with permission from.[303]

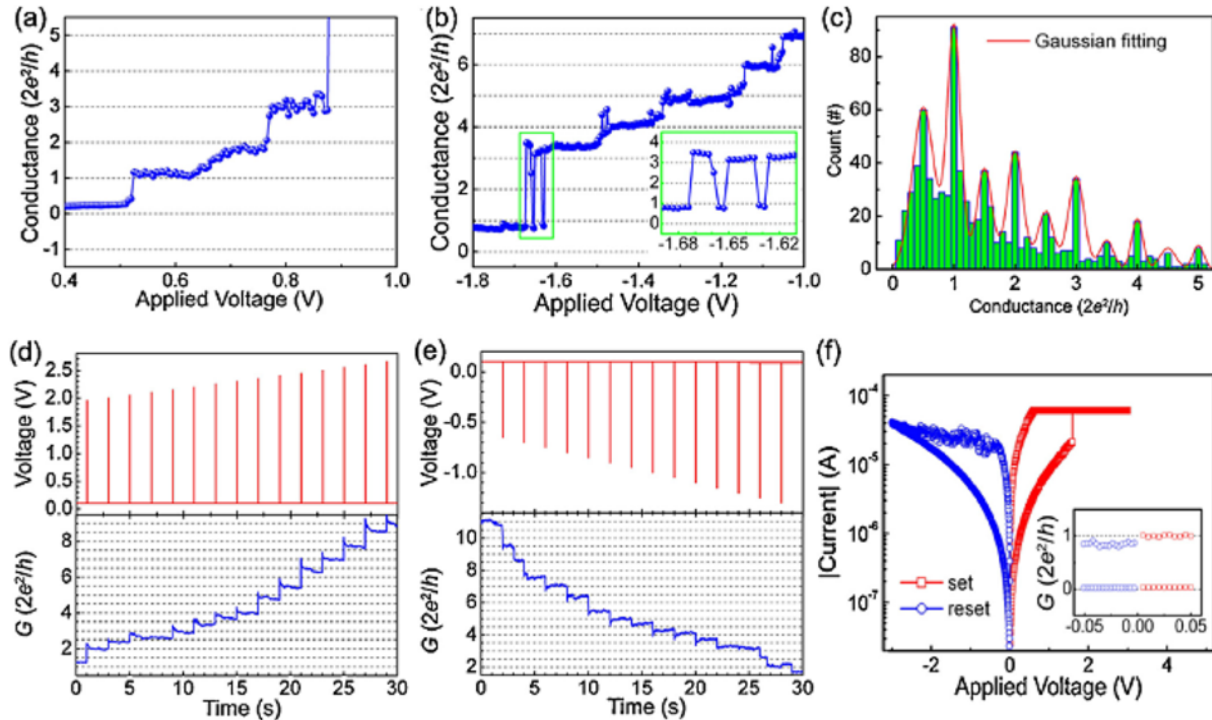

Fig. 45. Conductance quantization of the Ag/P3HT:PCBM/ITO device. (a) Conductance quantization during set process. Sweep speed: 0.25 V/S. (b) Conductance quantization during reset process. Sweep speed: 0.15 V/S. The inset shows the conductance oscillation between 3 and 1 G_0. (c) Histogram of more than 800 quantized conductance values extracted from about 150 set and reset processes. Conductance quantization under (d) positive voltage pulses with a width of 1 ms and (e) negative voltage pulses with a width of 5 ms. (f) Resistive switching between HRS and a desired quantized conductance of 1 G_0. The inset is the conductance values in low voltage regions. Reprinted with permission from.[301]

conductance can be quantized carefully. Most recently, the conductance of the Ag/P3HT: PCBM/ITO device has been successfully quantized based on an Ag filament.[301] It was shown that the sweep speed of the conductance quantization for the set process and reset process are 0.25 V/s and 0.15 V/s, respectively, as depicted in Fig. 45. In spite of these prospective findings, there is still a need for the commercialization of RRAM. Compared to other NVM candidates, RRAM is still an emerging technology that is in its infancy, resulting in various switching mechanisms being proposed for different switching materials, and even different conducting mechanisms for a single switching material. Therefore, to ensure the consistency of the experimental data,[86] it is essential to take care with electroforming as the initialization process of RRAM systems.

7. CONCLUSIONS

NVM consists of several overlapping technologies that share one common trait, i.e., non-volatility. Today, NVMs, which are particularly motivated by the emergence of flash memory, are driving information-processing technology into a broadening spectrum of new applications ranging from RFIDs, which requires only several KB of storage, to high-density storage of hundreds of GB in chips. Many of these applications are possible because of the performance gains and/or increased complexity realized by scaling. As the dimensional scaling of semiconductor devices using conventional CMOS technology will eventually approach the fundamental limits, it is important to revolutionize the current CMOS process technology or to explore new alternative information-processing devices and microarchitectures. This has led to the birth of a series of new type of flash memory structure, as well as several non-charge-storage memories such as FeRAM, MRAM, PCRAM, and RRAM. A performance comparison of these emerging NVMs and conventional solid-state memories such as SRAM and DRAM is presented in Table 1.

The current mainstream NVM is no doubt flash memory that can be classified as a NAND type and NOR type. NAND flash is mainly used for data storage, whereas NOR is used for code storage. Although a drastic increase in the areal density of NAND and NOR flash has been observed recently, they both face some serious scaling issues. For NAND flash, maintaining a GCR > 0.6 and preventing FG-to-FG cross talk are two difficult challenges when scaling below 20 nm. Three innovative technologies, namely high-K IPD, charge-trapping device, and 3D flash memory appear to

Table 1. Comparison of conventional and emerging memories. Reprinted with permission from.[86]

Type	Volatile memory		Non-volatile memory		Emerging non-volatile memory			
	SRAM	DRAM	NOR-FLASH	NAND-FLASH	MRAM	PRAM	FRAM	RRAM
Cell elements	6T	1T1C	1T	1T	1(2)T1R	1T1R or 1D1R	1T1C	1T1R or 1D1R
Cell	Latch	Stack/trench capacitor	Floating gate/ charge trap	Floating gate/ charge trap	Magnetoresistance	Phase-change	Polarization-change	Resistance-change
Minimum cell size	$140F^2$	6 F^2	10 F^2	5 F^2	20 F^2	4.8(4) F^2	22 F	4 F^2
Write/erase time	0.3ns/0.3ns	<10ns/<10ns	1ms/10ms	1ms/0.1ms	10ns/10ns	20ns/50ns	10ns/10ns	5ns/5ns
Endurance (cycles)	$>3\times10^{16}$	$>3\times10^{16}$	$>10^5$	$>10^5$	$>3\times10^{16}$	10^8	10^{14}	$>10^{10}$
Application	Cache	Main memory	Storage	Storage	Storage	Storage	Storage	Storage/Main memory

be potential solutions to alleviate such scaling issues. The successful implementation of the high-K IPD in the 20 nm and 16 nm nodes has already been demonstrated, indicating the prospects of scaling NAND memory into the 10 nm regime. However, the use of high-K IPD leads to a continuous increase in the word line-word line (WL-WL) electric field, and breakdown also becomes a serious scaling limitation. It can therefore be expected that further scaling will continue to be challenging as the electric field increases at each new node. Charge-trapping devices adopt only one gate to control the MOS device, whereby the GCR issue has been eliminated, and the cross talk between thin nitride storage layers is either insignificant or significantly reduced. However, it should be noted that despite the ability to scale below 20 nm, the use of charge-trapping devices cannot mitigate the fundamental limitations such as WL breakdown and too few electrons. At present, charge-trapping devices are rarely utilized in 2D NAND flash because of the existence of high-K IPD, while it can be found in most 3D NAND devices where the WL breakdown and electron number issues can be effectively suppressed because of the larger size compared to the 2D case. To date, 3D NAND flash appears to be the most promising candidates for next-generation flash devices to date, as it has broken through the physical limits imposed by 2D structures according to the successful vertical stacking of memory arrays. Such a 3D structure allows for high density by increasing the layers vertically, and thus circumvents the few electrons and WL breakdown limitations. For the above reasons, the majority of NAND flash manufacturers have focused their attentions on the fabrication of 3D NAND flash, and they have announced plans to introduce 3D NAND products using various 3D architectures. However, 3D structures have unique overhead costs that affect the array efficiency. In addition, each layer may need to be contacted separately, and this may incur additional processing cost. The number of layers must be sufficiently high to ensure high density along with the relaxation of the technology node, leading to an additional overhead cost. This tradeoff affects each 3D architecture, and a rapid replacement of 3D structures for 2D flash therefore cannot be realized in the near future. The main problem that limits the scaling of NOR flash arises from the demand for a >8 nm thick tunnel-oxide layer to avoid electron leakage. Besides, programming in NOR flash is obtained from the generation of hot electrons that is provided by a steep junction profile in the presence of a high lateral electric field. This in turn may cause a short channel effect and leakage current that disturb the program. Besides the technical limits, NOR flash is also facing stiff competition from both NAND flash and other emerging NVMs. The NOR flash market in high-density applications, such as in feature phones, has been steadily eroded by NAND, and several emerging memory technologies, such as PCM, can provide a similar performance (and better) at a somewhat lower cost. To prevent this occurrence, charge-trapping devices have recently been introduced to NOR flash memory to replace the original FG structure. With the aid of charge-trapping devices, the limits from the tunnel-oxide thickness can be significantly improved, while the leakage from the short-channel effect and junction breakdown remain. Consequently, the areal density of NOR flash has been experiencing a somewhat slow increase over the past 5 years, with a current node at 45 nm and slowly evolving to about 32 nm.

The idea of using FeRAM to achieve non-volatility is to toggle and sense the polarization state of a ferroelectric capacitor. The destructive read characteristics of FeRAM memory has actually imposed rigorous requirements on the ferroelectric and electrode materials that need to withstand extended operation cycles while exhibiting a significant difference in two polarization states. The difficulty in finding appropriate ferroelectric materials has severely limited the areal density of FeRAM, which is at least one technology generation behind NOR and NAND flash, and is not capable of MLC. In this case, the desire for FeRAM to replace NOR

or NAND Flash has gradually vanished. However, FeRAM memory has recently attracted considerable interest in embedded applications such as ID cards and smart cards because of its fast speed, low power consumption, and long endurance cycles. In order for FeRAM to come with its rivals for high-density storage, the basic geometry of the cell must be modified while maintaining the desired isolation. Recent developments in electrode materials indicate that there is promise to thin down the ferroelectric capacitor and extend the viability of 2D stacked capacitor in the near-term.[305] Beyond this time, the need for a 3D capacitor still imposes steep challenges.

MRAM that takes advantages of the TMR effect to accomplish programming/readout operations is considered the closest to a real "universal" memory owing to its ultra-fast speed and extremely high endurance. Nevertheless, the ability to provide a sufficiently high electrical field to achieve switching of the MTJ in scaled cells remains questionable, and limits the potential of the field switch MTJ MRAM to extend beyond the 65 nm node. Fortunately, this drawback can be significantly improved by means of the STT-MTJ MRAM, where a spin-polarized current transfers its angular momentum to the free magnetic layer in order to reverse its polarity without resorting to an external magnetic field. Nevertheless, the system endurance may be deteriorated by this substantial current passing through the MTJ tunnel layer. In addition, with the continuous downscaling the stability of the storage element suffers from thermal noise. Therefore, it is projected that perpendicular magnetization materials that have already been commercialized in HDD are needed at 32 nm and below.[306] In this case, it is not expected that STT-MRAM can replace NAND flash in the short term. However, its SRAM-like performance and much smaller footprint relative to that of the conventional 6T-SRAM have gained much interest in that application, especially in mobile devices.

The concept of PCRAM stems from the significant difference in resistivity between the amorphous and crystalline states of the chalcogenide glass (the most commonly used alloy is GST), which can be used to denote logic "1" and logic "0". The advantages of PCRAM over other NVMs arise from its somewhat simple cell structure and the low-voltage operation, making PCRAM attractive for embedded NVM applications. The major challenges for PCRAM are the high current required to reset the phase-change element and the fairly long set time. However, as the programming volume reduces along with the scaling of the cell, it can be reasonably inferred that both of the above issues will become easier with scaling. Another problem that results from the interaction of the phase-change material with electrodes may impose long-term reliability issues and limit the cycling endurance, impairing the feasibility for DRAM-like applications. Since 2011, PCRAM has been used in feature phones as a replacement for NOR flash, and since 2012, it has been mass-produced using the 45 nm. Furthermore, the scalability of PCRAM devices to <5 nm has recently been demonstrated using carbon nanotubes as electrodes.[307] This may imply that the replacement of NOR flash is not the ultimate goal for PCRAM. The current consensus is that the performance merits and scalability of PCRAM render it suitable for storage-class memory (SCM), which requires high-density, fast read/write and high endurance, and a complementary high-density memory to DRAM. Considering its limited endurance and smaller bandwidth, it is not possible for PCRAM to completely replace DRAM. However, the inherent non-volatility of PCRAM can avoid the refreshing power and the dead time for refreshing which has increasingly become a problem for DRAM. Hence, a hybrid memory consolidating the advantages of both PCRAM and DRAM may be a suitable candidate for future high-performance memory.

Compared to its predecessors, RRAM is a relatively new memory device that is still in the developmental stage. Although RRAM can be divided into several categories, all of the resistive memories induce the storage function through a switching process between two distinct resistive states. RRAM changes the MIM resistor conductivity using atomic processes, and they are therefore not limited by the number of storage electrons. In principle, it should also be limited by the number of atoms that provide the electrical characteristics. The main challenge for RRAM is that there is not yet a sufficient understanding of the atomic details, which limits the scaling of RRAM. At the device level, <10 nm RRAM has been reported.[308] In the array level, a 20-nm 1-Gb 2-layer 3D RRAM has been reported.[309] Further, at least one company has announced the introduction of products using RRAM as an embedded memory. However, high-density RRAM must still overcome several difficult challenges to become cost competitive relative to NAND. Recent developments in 2D NAND that enabled scaling below 20 nm and the introduction of 3D NAND have further reduced the required space for RRAM. An extreme scalability below 10 nm and a high ON/OFF ratio, bipolar, compact and high-endurance cell-selection devices are key challenges for high-density RRAM.

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REFERENCES

1. V. P.-H. Hu, M.-L. Fan, P. Su, and C.-T. Chuang, Comprehensive analysis of UTB GeOI logic circuits and 6T SRAM cells considering variability and temperature sensitivity, *IEDM Tech Dig*. pp. 32.4.1-4 (2011).
2. C. Lam, Cell design considerations for phase change memory as a universal memory, *IEEE VLSI Tech*. pp. 132-133 (2008).
3. L. Wang, C. D. Wright, M. M. Aziz, P. Shah, C. H. Yang, and G. W. Yang, Terabit-per-square-inch scanning probe phase-change memory model based on nucleation-growth theory, *Mater. Lett*. **112**, 51-53 (2013).
4. L. Wang, C. D. Wright, M. M. Aziz, J. Ying, and G. W. Yang, Optimisation of scanning probe phase-change memory in terms of the thermal conductivities of capping and under layer, *Europhys. Lett*. **104**, 56007-6 (2013).
5. C.-Y. Lu, Future prospects of NAND Flash memory technology-the evolution from floating gate to charge trapping to 3D stacking, *J. Nanosci. Nanotechno.* **12**, 7604-7618 (2012).
6. S. K. Lai, Brief history of ETOX^{TM} NOR Flash memory, *J. Nanosci. Nanotechno.* **12**, 7597-7603 (2012).
7. M. Lenzlinger and E. H. Snow, Fowler-Nordheim tunneling into thermally grown SiO_2, *J. Appl. Phys*. **40**, 278-283 (1969).
8. M. F. Hung, Y. C. Wu, and J. H. Chen, 2-bit operation based on modulated Fowler-Nordheim tunneling in charge-trapping Flash memory cell, *Appl. Phys. Lett*. **100**, 052107-3 (2012).
9. R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, Introduction to flash memory, *P. IEEE*. **91**, 489-502 (2003).
10. L.-J. Liu, K. S. L. Chang, Y. C. Jian, T. K. Wang, and M. J. Tsai, Performance enhancement in p-channel charge-trapping flash memory devices with Si/Ge super-lattice channel and band-to-band tunneling induced hot-electron injection, *Thin Solid Films* **533**, 1-4 (2013).
11. G. Zhang, W. J. Yoo, and C. H. Ling, Hot-electron capture for CHEI programming in SONOS-type Flash memory using high-K trapping layer, *IEEE T. Electron Dev.* **55**, 1502-1510 (2008).
12. Y. Zhang and D. S. Ang, Non-classical hot-electron mechanism and its implications on the reliability and scalability of the high-K dielectric N-MOS Flash memory cell, *Microelectron. Eng*. **84**, 1929-1933 (2007).
13. S. H. Lo, D. A. Buchanan, Y. Taur, and W. I. Wang, Quantum mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFETs, *IEEE T. Electron. Dev.* **18**, 209-211 (1997).
14. Y. Yamauchi, Y. Kamakura, T. Matsuoka, and N. Ueda, Source-side injection single-polysilicon split-gate Flash memory, *Jpn. J. Appl. Phys*. **53**, 034201-10 (2014).
15. S. Aritome, S.-J. Whang, K.-H. Lee, D.-G. Shin, B.-Y. Kim, M.-S. Kim, J.-H. Bin, J.-H. Han, S.-J. Kim, B.-M. Lee, Y.-K. Jung, S.-Y. Cho, C.-H. Shin, H.-S. Yoo, S.-M. Choi, K. Hong, S. Park, and S.-J. Hong, A novel three-dimensional dual control-gate with surrounding floating-gat (DC-SF) NAND flash cell, *Solid State Electron*. **79**, 166-171 (2013).
16. S. K. Lai, Flash memories: Successes and challenges, *IBM J. RES. DEV.* **52**, 529-535 (2008).
17. C.-Y. Lu, K.-Y. Hsieh, and R. Liu, Future challenges of Flash memory technologies, *Microelectron Eng*. **86**, 283-286 (2009).
18. L. Wang, C. D. Wright, M. M. Aziz, C.-H. Yang, and G.-W. Yang, Optimisation of readout performance of phase-change probe memory in terms of capping layer and probe tip, *Electron. Mater. Lett*. **10**, 1045-1049 (2014).
19. C. Miccoli, C. C. Monzio, L. Chiavarone, S. Beltrami, A. L. Lacaita, A. S. Spinelli, and A. Visconti, Reliability characterization issues for nanoscale Flash memories: A case study on 45-nm NOR devices, *IEEE T. Device. Mat. Re*. **13**, 362-369 (2013).
20. K. Kanda, N. Shibata, T. Hisada, K. Isobe, M. Sato, Y. Shimizu, and R. Yamashita, A 19 nm 112.8 mm 64 Gb Multi-level Flash memory with 400 Mbit/sec/pin 1.8 V toggle model interface, *IEEE J. Solid-St Circ.*, **48**, 159-167 (2013).
21. F. Yoshihisa, Review of emerging new solid-state Non-volatile memory, *Jpn. J. Appl. Phys*. **52**, 040001-11 (2013).
22. A. N. Broers, Resolution limits for electron beam lithography, *IBM. J. Res. Rev.* **32**, 502-513 (1988).
23. X. M. Yang, Directed block copolymer assembly versus electron beam lithography for bit-patterned media with areal density of 1 Terabit/inch^2 and beyond, *Acs Nano*. **3**, 1844-1858 (2009).
24. D. Suwandi, Y. Whulanza, and J. Istiyanto, Visible light maskless photolithography for biomachining application, *Appl. Mech. Mater*. **493**, 552-557 (2014).
25. H. Lan and H. Liu, UV-nanoimprint lithography: structure, materials and fabrication of flexible molds, *J. Nanosci. Nanotechno*. **13**, 3145-3172 (2013).
26. I. Ichimura, F. Maeda, K. Osato, K. Yamamoto, and Y. Kasami, Optical disk recording using a GaN blue-violet laser diode, *Jpn. J. Appl. Phys*. **39**, 937-942 (2000).
27. K. Yamamoto, K. Osato, I. Ichimura, F. Maeda and T. Watanabe, 0.8-numerical-aperture two-element objective lens for the optical disk, *Jpn. J. Appl. Phys*. **36**, 456-459 (1996).
28. H. J. Borg and R. V. Woudenberg, Trends in optical recording, *J. Magn. Magn. Mater*. **193**, 519-525 (1999).
29. Y. V. Martynov, B. Zijp, J. Aarts, J.-P. Baartman, G. Rosmalen, J. Schleipen, and H. Houten, High numerical aperture optical recording: active tilt correction or thin cover layer?, *Jpn. J. Appl. Phys*. **38**, 1786-1792 (1999).
30. J.-G. Kim, W.-C. Kim, H.-W. Hwang, W.-H. Shin, K.-S. Park, N.-C. Park, H. Yang, and Y.-P. Park, Anti-shock air gap control for SIL-based near-field recording system, *IEEE T. Magn*. **45**, 2244-2247 (2009).

31. D. Kwak, J. Park, K. Kim, Y. Yim, S. Ahn, Y. Park, J. Kim, W. Jeong, J. Kim, M. Park, B. Yoo, S. Song, H. Kim, J. Sim, S. Kwon, B. Hwang, H.-K. Park, S. Kim, Y. Lee, H. Shin, N. Yim, K. Lee, M. Kim, Y. Lee, J. Park, S. Park, J. Jung, and K. Kinam, Integration technology of 30 nm generation multi-level NAND Flash for 64 Gb NAND Flash memory, *IEEE VLSI Tech*. 12-13 (2007).
32. Y. Ban, A. Miloslavsky, K. Lucas, S.-H. Choi, C.-H. Park, and D. Z. Pan, Layout decomposition of self-aligned double patterning for 2D random logic patterning, *Proc. SPIE.* **7974**, 79740L-15 (2011).
33. M. Wei, R. Banerjee, L. Zhang, A. Masad, S. Reidy, J. Ahn, H. Chao, C. Lim, T. Castro, O. Karpendo, M. Ru, R. Fastow, A. Brand, X. Guo, J. Gorman, W. J. McMahon, B. J. Woo, and A. Fazio, A scalable self-aligned contact NOR flash technology, *IEEE VLSI Tech*. 226-227 (2007).
34. J. Javanifard, T. Tanadi, H. Giduturi, K. Loe, R. L. Melcher, S. Khabiri, N. T. Hendrickson, A. D. Proescholdt, D. A. Ward, and M. A. Taylor, A 45 nm self-aligned-contact process 1Gb NOR Flash with 5 MB/s program speed, *IEEE ISSCC*, 424-624 (2008).
35. D. Shum, J. R. Power, R. Ullmann, E. Suryaputra, K. Ho, J. Hsiao, and L. C. Tran, Highly reliable flash memory with self-aligned split-gate cell embedded into high performance 65 nm CMOS for automotive and smartcard applications, *IEEE IMW*, 1-4 (2012).
36. H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y. Fukuzumi, M. Sato, Y. Nagata, Y. Matsuoka, Y. Iwata, H. Aochi, and A. Nitayama, Bit cost scalable technology with punch and plug process for ultra high density Flash memory, *IEEE VLSI*, 14-15 (2007).
37. R. Katsumata, M. Kito, Y. Fukuzumi, M. Kido, H. Tanaka, Y. Komori, M. Ishiduki, J. Matsunami, T. Fujiwara, Y. Nagata, L. Zhang, Y. Iwata, R. Kirisawa, H. Aochi, and A. Nitayama, Pipe-shaped BiCS Flash memory with 16 stacked layers and multi-level-cell operation for ultra high density storage devices, *IEEE VLSI*, 136-137 (2009).
38. J. Jang, H. S. Kim, W. Cho, H. Cho, J. Kim, S. I. Shim, Y. Jang, J. H. Jeong, B. K. Son, D. W. Kim, K. Kim, J. J. Shim, J. S. Lim, K. H. Kim, S. Y. Yi, J. Y. Lim, D. Chung, H. C. Moon, S. Hwang, J. W. Lee, Y. H. Son, U. I. Chung, and W. S. Lee, Vertical cell array using TCAT (Terabit cell array transistor) technology for ultra high density NAND Flash memory, *IEEE VLSI*, 192-193 (2009).
39. J. Kim, A. J. Hong, S. M. Kim, E. B. Song, J. H. Park, J. Han, S. Choi, D. Jang, J. T. Moon, and K. L. Wang, Novel vertical-stacked-array-transistor (VSAT) for ultra-high-density and cost-effective NAND Flash memory devices and SSD (Solid state drive), *IEEE VLSI*, pp. 186-187 (2009).
40. W. Kim, S. Choi, J. Sung, T. Lee, C. Park, H. Ko, J. Jung, I. Yoo, and Y. Park, Multi-layered vertical gate NAND Flash overcoming stacking limit for terabit density storage, *IEEE VLSI*, pp. 188-189 (2009).
41. C. H. Hung, H. T. Lue, K. P. Chang, C. P. Chen, Y. H. Hsiao, S. H. Chen, Y. H. Shih, K. Y. Hsieh, M. Yang, J. Lee, S. Y. Wang, T. Yang, K. C. Chen, and C. Y. Lu, A highly scalable vertical gate (VG) 3D NAND with high program disturb immunity using a novel PN diode decoding structure, *IEEE VLSI*, pp. 68-69 (2011).
42. S. H. Chen, H. T. Lue, Y. H. Shih, C. F. Chen, T. H. Hsu, Y. R. Chen, Y. H. Hsiao, S. C. Huang, K. Chang, C. C. Hsieh, G. R. Lee, A. Chuang, C. W. Hu, C. J. Chiu, L. Y. Lin, H. J. Lee, F. N. Tsai, C. C. Yang, T. H. Yang, and C. Y. Lu, A highly scalable 8-layer vertical gate 3D NAND with split-page bit line layout and efficient binary-sum MiLC (minimal incremental layer cost) staircase contacts, *IEEE IEDM*, pp. 2.3.1-4 (2012).
43. J. Kim, A. J. Hong, S. M. Kim, K-S. Shin, E. B. Song, Y. Hwang, F. Xiu, K. Galatsis, C. O. Chui, R. N. Candler, S. Choi, J.-T. Moon and K. L. Wang, A stacked memory device on logic 3D technology for ultra-high-density data storage, *Nanotechnology* **22**, 254006-11 (2011).
44. R. D. Sherman, L. M. Middleman, and S. M. Jacobs, Electron transport processes in conductor-filled polymer, *Poly. Eng. Sci*. **23**, 36-46 (1983).
45. S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, A silicon nanocrystals based memory, *Appl. Phys. Lett*. **68**, 1377-1379 (1996).
46. C. H. Lee, J. Meteer, V. Narayanan, and E. C. Kan, Self-assembly of metal nanocrystals on ultrathin oxide for nonvolatile memory applications, *J. Electron. Mater.* **34**, 1-11 (2005).
47. E. Kapetanakis, P. Normand, D. Tsoukalas, K. Beltsios, J. Stoemenos, S. Zhang, and J. van den Berg, Charge storage and interface states effects in Si-nanocrystal memory obtained using low-energy Si^+ implantation and annealing, *Appl. Phys. Lett*. **77**, 3450-3453 (2000).
48. C. H. Chen, T. C. Chang, I. H. Liao, P. B. Xi, J. Hsieh, J. Chen, T. Huang, S. M. Sze, U. S. Chen, and J. R. Chen, Tungsten oxide/tungsten nanocrystals for nonvolatile memory devices, *Appl. Phys. Lett*. **92**, 013114-3 (2008).
49. T.-C. Chang, F.-Y. Jian, S.-C. Chen, and Y.-T. Tsai, Developments in nanocrystal memory, *Mater Today*, **14**, 608-615 (2011).
50. S. K. Ray, S. Maikap, W. Banerjee, and S. Das, Nanocrystals for silicon-based light-emitting and memory devices, *J. Phys. D: Appl. Phys*. **46**, 153001-31 (2013).
51. M. L. Ostraat, J. W. De Blauwe, M. L. Green, L. D. Bell, M. L. Brongersma, J. Casperson, R. C. Flagan, and H. A. Atwater, Synthesis and characterization of aerosol silicon nanocrystal nonvolatile floating-gate memory devices, *Appl. Phys. Lett*. **79**, 433-435 (2001).
52. S. Tiwari, J. A. Wahl, H. Silva, F. Rana, and J. J. Welser, Small silicon memories: Confinement, single-electron, and interface state considerations, *Appl. Phys. A*. **4**, 403-414 (2000).

53. C. H. Kao, C. S. Lai, C. S. Huang, and K. M. Fan, Ge nanocrystal charge trapping devices fabricated by one-step oxidation on poly-SiGe, *Appl. Surf. Sci*. **255**, 2512-2516 (2008).
54. C. Bonafos, M. Carrada, G. Benassayag, S. Schamm-Chardon, J. Groenen, V. Paillard, B. Pecassou, A. Claverie, P. Dimitrakis, E. Kapetanakis, V. Ioaannou-Sougleridis, P. Normand, B. Sahu, and A. Slaoui, Si and Ge nanocrystals for future memory devices, *Mater. Sci. Semicon. Proc*. **15**, 615-626 (2012).
55. J. D. Blauwe, Nanocrystal nonvolatile memory devices, *IEEE T. Nanotechnol.* **1**, 72-77 (2002).
56. Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, Effects of traps on charge storage characteristics in metal-oxide-semiconductor memory structures based on silicon nanocrystals, *J. Appl. Phys*. **84**, 2358-2360 (1998).
57. F. M. Yang, T. C. Chang, P. T. Liu, U. S. Chen, P. H. Yeh, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Lou, Nickel nanocrystals with HfO_2 blocking oxide for nonvolatile memory application, *Appl. Phys. Lett*. **90**, 222104-3 (2007).
58. F. M. Yang, T. C. Chang, P. T. Liu, P. H. Yeh, Y. C. Yu, J. Y. Lin, S. M. Sze, and J. C. Lou, Memory characteristics of Co nanocrystal memory device with HfO_2 as blocking oxide, *Appl. Phys. Lett*. **90**, 132102-3 (2007).
59. Z. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, Metal nanocrystal memories-part I: Device design and fabrication, *IEEE T. Electron Dev*. **49**, 1606-1613 (2002).
60. W. Banerjee, S. Maikap, T.-C. Tien, W.-C. Li, and J.-R. Yang, Impact of metal nano layer thickness on tunnelling oxide and memory performance of core-shell iridium-oxide nanocrystals, *J. Appl. Phys*. **110**, 074309-7 (2011).
61. J. J. Lee and D.-L. Kwong, Metal nanocrystal memory with high-k tunneling barrier for improved data retention, *IEEE T. Electron. Dev*. **52**, 507-511 (2005).
62. H. Zhou, B. Li, Z. Yang, N. Zhan, D. Yang, R. K. Lake, and J. L. Liu, $TiSi_2$ nanocrystal metal oxide semiconductor field effect transistor memory, *IEEE T. Nanotechnol*. **10**, 499-505 (2011).
63. C. Bonafos, M. Carrada, G. Benassayag, S. Schamm-Chardon, J. Groenen, V. Paillard, B. Pecassou, A. Claverie, P. Dimitrakis, E. Kapetanakis, V. Ioannou-Sougleridis, P. Normand, B. Sahu, and A. Slaoui, Si and Ge nanocrystals for future memory devices, *Mater. Sci. Semicon. Proc*. **15**, 615-626 (2012).
64. Y.-H. Lin and C.-H. Chien, HfO_2 nanocrystal memory on SiGe channel, *Solid State Electron*. **80**, 5-9 (2013).
65. S.-M. Yang, C.-H. Chien, J.-J. Huang, and F. Tan, Non-volatile flash memory devices using CeO_2 nanocrystal trapping layer for two-bit per cell applications, *Jpn. J. Appl. Phys*. **46**, 3291-3295 (2007).
66. S. Maikap, T. Y. Wang, P. J. Tzeng, C. H. Lin, T. C. Tien, L. S. Lee, and M. J. Tsai, Band offsets and charge storage characteristics of atomic layer deposited high-k HfO_2/TiO_2 multilayers, *Appl. Phys. Lett*. **90**, 262901-3 (2007).
67. S. Jayanti, X. Yang, R. Suri, and V. Misra, Ultimate salability of TaN metal floating gate with incorporation of high-K blocking dielectrics for Flash memory applications, *IEEE IEDM*, pp. 5.3.1-4 (2010).
68. P. Blomme and J. V. Houdt, Scalability study of fully planarized hybrid floating gate Flash memory cells with high-K IPD, *IEEE IMW*, pp. 1-4 (2012).
69. S. Aritome and T. Kikkawa, Scaling challenge of self-aligned STI cell (SA-STI cell) for NAND Flash memories, *Solid State Electron*. **82**, 54-62 (2013).
70. M. Bhaisare, A. Misra, M. Waikar, and A. Kottantharayil, High quality Al_2O_3 dielectric films deposited by pulsed-DC reactive sputtering technique for high-K applications, *Nanosci. Nanotechno. Lett*. **4**, 645-650 (2012).
71. C.-H. Lee, S.-H. Hur, Y.-C. Shin, J.-H. Choi, D.-G. Park, and K. Kim, Charge-trapping device structure of SiO_2/SiN/high-K dielectric Al_2O_3 for high-density Flash memory, *Appl. Phys. Lett*. **86**, 152908-4 (2005).
72. G. Congedo, A. Lamperti, L. Lamagna, and S. Spiga, Stack engineering of TANOS charge-trap Flash memory cell using high-kappa ZrO_2 grown by ALD as charge trapping layer, *Microelectron. Eng*. **88**, 1174-1177 (2011).
73. T.-H. Hsu, H.-T. Lue, Y.-C. King, J.-Y. Hsieh, E.-K. Lai, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, A high-performance body-tied FinFET bandgap engineered SONOS (BE-SONOS) for Nand-type Flash memory, *IEEE T. Electron. Dev*. **28**, 443-445 (2007).
74. H.-T. Lue, S.-C. Lai, T.-H. Hsu, Y.-H. Hsiao, P.-Y. Du, S.-Y. Wang, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, A critical review of charge-trapping NAND Flash devices, *IEEE ICSICT*, pp. 807-810 (2008).
75. S. C. Lai, H.-T. Lue, M.-J. Yang, J.-Y. Hsieh, S.-Y. Wang, T.-B. Wu, G.-L. Luo, C.-H. Chien, E.-K. Lai, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, MA BE-SNONS: a bandgap engineered SONOS using metal gate and Al_2O_3 blocking layer to overcome erase saturation, *IEEE NVSMW*, pp. 88-89 (2007).
76. H.-T. Lue, S.-C. Lai, T.-H. Hsu, P.-Y. Du, S.-Y. Wang, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, Modeling of barrier-engineered charge-trapping NAND Flash devices, *IEEE Trans. Dev. Mater. Re*. **10**, 222-232 (2010).
77. P. Blomme, M. Rosmeulen, A. Cacciato, M. Kostermans, C. Vrancken, S. V. Aerde, T. Schram, I. Debusschere, M. Jurczak, and J. V. Houdt, Novel dual layer floating gate structure as enabler of fully planar Flash memory, *IEEE VLSI*, pp. 129-130 (2010).
78. H.-T. Lue, Y.-H. Hsiao, K.-Y. Hsieh, S.-Y. Wang, T. Yang, K.-C. Chen, and C.-Y. Lu, Scaling feasibility study of planar thin floating gate (FG) NAND Flash devices and size effect challenges beyond 20 nm, *IEEE IEDM*, pp. 9.2.1-4 (2011).
79. G. Dong, N. Xie, and T. Zhang, On the use of soft-decision error-correction codes in NAND Flash memory, *IEEE T. Circuits. Syst*. **58**, 429-439 (2011).

80. K. Kim, Technology challenges for deep-nano semiconductor, *IEEE IMW*, pp. 1-2 (2010).
81. B. Chen, X. Zhang, and Z. Wang, Error correction for multi-level NAND Flash memory using Reed-Solomon codes, *IEEE SiPS*, pp. 94-99 (2008).
82. J. S. Meena, S. M. Sze, U. Chand, and T.-Y. Tseng, Overview of emerging non-volatile memory technologies, *Nanoscale. Res. Lett*. **9**, 526-558 (2014).
83. S. J. Whang, K. H. Lee, D. G. Shin, B. Y. Kim, M. S. Kim, J. H. Bin, J. H. Han, S. J. Kim, B. M. Lee, Y. K. Jung, S. Y. Cho, C. H. Shin, H. S. Yoo, S. M. Choi, K. Hong, S. Aritome, S. K. Park, and S. J. Hong, Novel 3-dimensional dual control-gate with surrounding floating-gate (DC-SF) NAND flash cell for 1Tb file storage application, *IEEE IEDM*, pp. 29.7.1-29.7.4 (2010).
84. S. Aritome, NAND Flash innovations, *IEEE Solid-State Circuits Magazine.* **5**, 21-29 (2013).
85. Y. Fujisaki, Overview of emerging semiconductor non-volatile memories, *IEICE Electron. Exp*. **9**, 908-925 (2012).
86. D. S. Jeong, R. Thomas, R. S. Katiyar, J. F. Scott, H. Kohlstedt, A. Petraru, and C. S. Hwang, Emerging memories: resistive switching mechanisms and current status, *Rep. Prog. Phys*. **75**, 076502-31 (2012).
87. L. V. Hai, M. Takahashi, and S. Sakai, Downsizing of Ferroelectric-gate field-effect-transistors for Ferroelectric-NAND Flash memory cells, *IEEE IMW*, pp. 1-4 (2011).
88. X. Zhang, M. Takahashi, K. Takeuchi, and S. Sakai, 64kbit Ferroelectric-gate-transistor-integrated NAND Flash memory with 7.5V program and long data retention, *Jpn. J. Appl. Phys*. **51**, 04DD01-7 (2012).
89. S. Sakai and R. Ilangovan, Metal-Ferroelectric-Insulator-Semiconductor Memory FET with long retention and high endurance, *IEEE Electron. Dev. Lett*. **25**, 369-371 (2004).
90. H. Shiga, Y. Toshiba, D. Takashima, S. Shiratake, K. Hoya, T. Miyakawa, R. Ogiwara, R. Fukuda, R. Takizawa, K. Hatsuda, F. Matsuoka, Y. Nagadomi, D. Hashimoto, H. Nishimura, T. Hioka, S. Doumae, S. Shimizu, M. Kawano, T. Taguchi, Y. Watanabe, S. Fujii, T. Ozaki, H. Kanaya, Y. Kumura, Y. Shimojo, Y. Yamada, Y. Minami, S. Shuto, K. Yamakawa, S. Yamazaki, I. Kunishima, T. Hamamoto, A. Nitayama, and T. Furuyama, A 1.6GB/s DDR2 128Mb chain FeRAM with scalable octal bitline and sensing schemes, *IEEE ISSCC*, pp. 464-465 (2009).
91. Y. K. Hong, D. J. Jung, S. K. Kang, H. S. Kim, J. Y. Jung, H. K. Koh, J. H. Park, D. Y. Choi, S. E. Kim, W. S. Ann, Y. M. Kang, H. H. Kim, J.-H. Kim, W. U. Jung, E. S. Lee, S. Y. Lee, H. S. Jeong, and K. Kim, 130 nm technology 0.25 μm^2, 1T1C FRAM cell for SoC (System-on-a-Chip)-friendly applications, *IEEE VLSI*, pp. 230-231 (2007).
92. J. Wang, J. B. Neaton, H. Zheng, V. Nagarajan, S. B. Ogale, B. Liu, D. Viehland, V. Vaithyanathan, D. G. Schlom, U. V. Waghmare, N. A. Spaldin, K. M. Rabe, M. Wuttig, and R. Ramesh, Epitaxial $BiFeO_3$ multiferroic thin film heterostructures, *Science* **299**, 1719-1722 (2003).
93. I. Hiroshi, Impurity substitution effects in $BiFeO_3$ thin films-from a viewpoint of FeRAM applications, *Curr. Appl. Phys*. **12**, 603-611 (2012).
94. D. Y. Zhou, J. Muller, J. Xu, S. Knebel, D. Brauhaus, and U. Schroder, Insights into electrical characteristics of silicon doped hafnium oxide ferroelectric thin films, *Appl. Phys. Lett.* **100**, 082905-4 (2012).
95. T. S. Boscke, J. Muller, D. Brauhaus, U. Schroder, and U. Bottger, Ferroelectricity in hafnium oxide thin films, *Appl. Phys. Lett*. **99**, 102903-3 (2011).
96. B. H. Park, B. S. Kang, S. D. Bu, T. W. Noh, J. Lee, and W. Jo, Lanthanum-substituted bismuth titanate for use in non-volatile memories, *Nature* **401**, 682-684 (1999).
97. Y. Fujisaki, K. Iseki, and H. Ishiwara, Significant enhancement of $Bi_{3.45}La_{0.75}Ti_3O_{12}$ Ferroelectricity derived by sol-gel method, *Jpn. J. Appl. Phys*. **42**, L267-9 (2003).
98. H. J. Fan, S. Kawasaki, J. M. Gregg, A. Langner, T. Leedham, and J. F. Scott, Concentric metallic-piezoelectric microtube arrays, *Proc. MRS.* **1071**, F01-07 (2008).
99. M. Miyake, J. F. Scott, X. J. Lou, F. D. Morrison, T. Nonaka, S. Motoyama, T. Tatsuta, and O. Tsuji, Submicron three-dimensional trenched electrodes and capacitors for DRAMs and FRAMs: Fabrication and electrical testing, *J. Appl. Phys*. **104**, 064112-7 (2008).
100. T. P. Ma and J.-P. Han, Why is nonvolatile ferroelectric memory field-effect transistor still elusive?, *IEEE Electron. Dev. Lett*. **23**, 386-388 (2002).
101. T. S. Boscke, J. Muller, D. Brauhaus, U. Schroder, and U. Bottger, Ferroelectricity in hafnum oxide: CMOS compatible ferroelectric field effect transistors, *IEEE IEDM*, 24.5.1-24.5.4 (2011).
102. M. H. Park, H. J. Kim, Y. J. Kim, W. Lee, H. K. Kim, and C. S. Hwang, Effect of forming gas annealing on the ferroelectric properties of $Hf_{0.5}Zr_{0.3}O_2$ thin films with and without Pt electrodes, *Appl. Phys. Lett*. **102**, 112914-4 (2013).
103. S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, and T. Mikolajick, Incipient ferroelectricity in Al-doped HfO_2 thin films, *Adv. Funct. Mater*. **22**, 2412-2417 (2012).
104. J. Muller, E. Yurchuk, T. Schlosser, J. Paul, R. Hoffmann, S. Muller, D. Martin, S. Slesazeck, P. Polakowski, J. Sundqvist, M. Czernohorsky, K. Seidel, P. Kucher, R. Boschke, M. Trentzsch, K. Gebauer, U. Schroder, and T. Mikolajick, Ferroelectricity in HfO_2 enables nonvolatile data storage in 28 nm HKMG, *IEEE VLSI*, pp. 25-26 (2012).
105. J. Muller, T. S. Boscke, D. Brauhaus, U. Schroder, U. Bottger, J. Sundqvist, P. Kucher, T. Mikolajick, and L. Frey, Ferroelectric $Zr_{0.5}Hf_{0.5}O_2$ thin films for nonvolatile memory applications, *Appl. Phys. Lett*. **99**, 112901-3 (2011).
106. J. Muller, U. Schroder, T. S. Boscke, I. Muller, U. Botter, L. Wilde, J. Sundqvist, M. Lemberger, P. Kucher, T.

Mikolajick, and L. Frey, Ferroelectricity in yttrium-doped hafnium oxide, *J. Appl. Phys*. **110**, 114113-5 (2011).
107. X. Zhang, M. Takahashi, K. Takeuchi, and S. Sakai, 64 kbit Ferroelectric-gate-transistor-integrated NAND Flash memory with 7.5 V program and long data retention, *Jpn. J. Appl. Phys*. **51**, 04DD01-7 (2012).
108. S. Horiuchi and Y. Tokura, Organic ferroelectrics, *Nat. Mater*. **7**, 357-366 (2008).
109. R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, and D. M. De Leeuw, High-performance solution-processed polymer ferroelectric field-effect transistors, *Nat. Mater*. **4**, 243-248 (2005).
110. G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, D. M. De Leeuw, R. C. G. Naber, and P. W. M. Blom, All-polymer ferroelectric transistors, *Appl. Phys. Lett*. **87**, 092903-3 (2005).
111. B. H. Kim, C. W. Byun, S.-M. Yoon, S. H. Yang, S.-W. Jung, M. K. Ryu, S.-H. K. Park, C.-S. Hwang, K.-I. Cho, O.-S. Kwon, E.-S. Park, H. C. Oh, K.-H. Kim, and K. C. Park, Oxide-thin-film-transistor-based ferroelectric memory array, *IEEE Electron. Dev. Lett*. **32**, 324-326 (2011).
112. S. Raghavan, I. Stolichnov, N. Setter, J.-S. Heron, M. Tosun, and A. Kis, Long-term retention in organic ferroelectric-graphene memories, *Appl. Phys. Lett*. **100**, 023507-3 (2012).
113. W. Fu, Z. Xu, X. Bai, C. Gu, and E. Wang, Intrinsic memory function of carbon nanotube-based ferroelectric field-effect transistor, *Nano Lett*. **9**, 921-925 (2009).
114. D.-W. Fu, H.-L. Cai, Y. Liu, Q. Ye, W. Zhang, Y. Zhang, X.-Y. Chen, G. Giovannetti, M. Capone, J. Li, and R.-G. Xiong, Diisopropylammonium Bromide is a high-temperature molecular ferroelectric crystal, *Science* **339**, 425-428 (2013).
115. H.-Y. Ye, Y. Zhang, S.-I. Noro, K. Kubo, M. Yoshitake, Z.-Q. Liu, H.-L. Cai, D.-W. Fu, H. Yoshikawa, K. Awaga, R.-G. Xiong, and T. Nakamura, Molecule-displacive ferroelectricity in organic supramolecular solids, *Sci. Reports*. **3**, 2249-6 (2013).
116. A. S. Tayi, A. K. Shveyd, A. C.-H. Sue, J. M. Szarko, B. S. Rolczynski, D. Cao, T. J. Kennedy, A. A. Sarjeant, C. L. Stern, W. F. Paxton, W. Wu, S. K. Dey, A. C. Fahrenbach, J. R. Guest, H. Mohseni, L. X. Chen, K. L. Wang, J. F. Stoddart, and S. I. Stupp, Room-temperature ferroelectricity in suramolecular networks of charge-transfer complexes, *Nature*. **488**, 485-489 (2012).
117. W. H. Butler, X.-G. Zhang, T. Schulthess, and J. M. Maclarem, Spin-dependent tunneling conductance of Fe/MgO/Fe sandwiches, *Phys. Rev. B*. **63**, 054416-12 (2001).
118. J. Mathon and A. Umerski, Theory of tunneling magnetoresistance of an epitaxial Fe/Mgo/Fe(001) junction, *Phys. Rev. B*. **63**, 220403-4 (2001).
119. S. Yuasa, T. Katayama, T. Nagahama, A. Fukushima, H. Kubota, Y. Suzuki, and K. Ando, Giant room-temperature magnetoresistance in single-crystal Fe/MgO/Fe magnetic tunnel junctions, *Nat. Mater*. **3**, 868-871 (2004).
120. S. S. P. Parkin, C. Kaiser, A. Panchula, P. M. Rice, B. Hughes, M. Samant, and S.-H. Yang, Giant tunneling magnetoresistance at room temperature with MgO (100) tunnel barriers, *Nat. Mater*. **3**, 862-867 (2004).
121. D. D. Djayaprawira, K. Tsunekawa, M. Nagai, H. Maehara, S. Yamagata, N. Watanabe, S. Yuasa, Y. Suzuki, and K. Ando, 230% room-temperature magnetoresistance in CoFeB/Mgo/CoFeB magnetic tunnel junctions, *Appl. Phys. Lett*. **86**, 092502-3 (2005).
122. J. Hayakawa, S. Ikeda, F. Matsukura, H. Takahashi, and H. Ohno, Dependence of giant tunnel magnetoresistance of sputtered CoFeB/MgO/CoFeB magnetic tunnel junctions on MgO barrier thickness and annealing temperature, *Jpn. J. Appl. Phys*. **44**, 587-589 (2005).
123. T. Kawahara, K. Ito, R. Takemura, and H. Ohno, Spin-transfer torque RAM technology: review and prospect, *Microelectron Reliab*. **52**, 613-627 (2012).
124. S. Ikeda, J. Hayakawa, Y. Ashizawa, Y. M. Lee, K. Miura, H. Hasegawa, M. Tsunoda, F. Matsukura, and H. Ohno, Tunnel magnetoresistance of 604% at 300K by suppression of Ta diffusion in CoFeB/Mgo/CoFeB pseudo-spin-valves annealed at high temperature, *Appl. Phys. Lett*. **93**, 082508-3 (2008).
125. H. Liu, D. Bedau, D. Backes, J. A. Katine, J. Langer, and A. D. Kent, Ultrafast switching in magnetic tunnel junction based orthogonal spin transfer devices, *Appl. Phys. Lett*. **97**, 242510-3 (2010).
126. B. Prince, Trends in scaled and nanotechnology memories, *IEEE NVMSTS*, pp. 55-61 (2005).
127. I. L. Prejbeanu, S. Bandiera, J. A. Herault, R. C. Sousa, B. Dieny, and J. P. Nozieres, Thermally assisted MRAMs: ultimate scalability and logic functionalities, *J. Phys. D: Apply. Phys*. **46**, 074002-16 (2013).
128. I. L. Prejbeanu, R. C. Sousa, B. Dieny, J.-P. Nozieres, S. Bandiera, J. A. Herault, Q. Stainer, L. Lornbard, C. Ducruet, Y. Conraux, and K. Mackay, Scalability and logic functionalities of TA-MRAMs, *IEEE NEWCAS*, pp. 1-4 (2013).
129. I. L. Prejbeanu, M. Kerekes, R. C. Sousa, H. Sibuet, O. Redon, B. Dieny, and J. P. Nozieres, Thermally assisted MRAM, *J. Phys. Condens. Matter*. **19**, 165218-23 (2007).
130. B. Dieny, R. Sousa, S. Bandiera, M. C. Souza, S. Auffret, B. Rodmacq, J. P. Nozieres, J. Herault, E. Gapihan, I. L. Prejbeanu, C. Ducruet, C. Portemont, K. Mackay, and B. Cambou, Extend scalability and functionalities of MRAM based on thermally assisted writing, *IEEE IEDM*, 1.3.1-4 (2011).
131. J. C. Slonczewske, Current-driven excitation of magnetic multi-layers, *J. Magn. Mater*. **159**, L1-L7 (1996).
132. E. Chen, D. Apalkov, A. D. Smith, A. Khvalkovskiy, D. Lottis, K. Moon, V. Nikitin, A. Ong, X. Tang, S. Watts, R. Kawakami, M. Krounbi, S. A. Wolf, S. J. Poon, J. W. Lu, A. W. Ghosh, M. Stan, W. Butler, T. Mewes, S. Gupta, C.

K. A. Mewes, P. B. Visscher, and R. A. Lukaszew, Progress and prospects of spin transfer torque random access memory, *IEEE T. Magn*. **48**, 3025-3030 (2012).
133. K. C. Chun, H. Zhao, J. D. Harms, T. H. Kim, J. P. Wang, and C. H. Kim, A scaling roadmap and performance evaluation of in-plane and perpendicular MTJ based STT-MRAMs for high-density cache memory, *IEEE J. Solid-St Circ*, **48**, 598-610 (2013).
134. W. Kim, J. H. Jeong, Y. Kim, W. C. Lim, J. H. Kim, J. H. Park, H. J. Shin, Y. S. Park, K. S. Kim, S. H. Park, Y. J. Lee, K. W. Kim, H. J. Kwon, H. L. Park, H. S. Ahn, S. C. Oh, J. E. Lee, S. O. Park, S. Choi, H. K. Kang, and C. Chung, Extended scalability of perpendicular STT-MRAM towards sub-20 nm MTJ mode, *IEEE IEDM*, pp. 531-534 (2011).
135. E. Chen, D. Apalkov, Z. Diao, A. D. Smith, D. Druist, D. Lottis, V. Nikitin, X. Tang, S. Watts, S. A. Wolf, A. W. Ghosh, J. W. Lu, S. J. Poon, M. Stan, W. H. Butler, S. Gupta, C. K. A. Mewes, T. Mewes, and P. B. Visscher, Advances and future prospects of spin-transfer torque random access memory, *IEEE T. Magn*. **46**, 1873-1878 (2010).
136. A. V. Khvalkovskiy, D. Apalkov, S. Watts, R. Chepulskii, R. S. Beach, A. Ong, X. Tang, A. D. Smith, W. H. Butler, P. B. Visscher, D. Lottis, E. Chen, V. Nikitin, and M. Krounbi, Basic principles of STT-MRAM cell operation in memory arrays, *J. Phys. D: Appl. Phys*. **46**, 074001-20 (2013).
137. R. F. Pearson, Application of magneto-optic effects in magnetic materials, *Contemp. Phys*. **14**, 201-211 (1973).
138. R. Leuschner, U. K. Klostermann, H. Park, F. Dahmani, R. Dittrich, C. Grigis, K. Herman, S. Mege, C. Park, M. C. Clech, G. Y. Lee, S. Bournat, L. Altimime, and G. Mueller, Thermal select MRAM with a 2-bit cell capability for beyond 65 nm technology node, *IEEE IEDM*, pp. 1-4 (2006).
139. K.-S. Kim, B. K. Cho, and T. W. Kim, Switching and reliability issues of magnetic tunnel junctions for high-density memory device, *Curr. Appl. Phys*. **6**, e86-e91 (2006).
140. N. D. Rizzo, D. Houssameddine, J. Janesky, R. Whig, F. B. Mancoff, M. L. Schneider, M. Deherrera, J. J. Sun, K. Nagel, S. Deshpande, H.-J. Chia, S. M. Alam, T. Andre, S. Aggarwal, and J. M. Slaughter, A fully functional 64Mb DDR3 ST-MRAM built on 90nm CMOS technology, *IEEE T. Magn*. **49**, 4441-4446 (2013).
141. L. Wang, C.-H. Yang, S. Gai, and J. Wen, Current status and future prospects of conventional recording technologies for mass storage applications, *Curr. Nanosci*. **10**, 638-659 (2014).
142. L. Wang and S. Gai, The next generation mass storage devices-physical principles and current status, *Contemp. Phys*. **55**, 75-93 (2014).
143. J.-M. Hu, Z. Li, L.-Q. Chen, and C.-W. Nan, High-density magnetoresistive random access memory operation gate ultralow voltage at room temperature, *Nature* **2**, 1-8 (2011).
144. S. R. Ovshinsky, Reversible electrical switching phenomena in disordered structures, *Phys. Rev. Lett.* **21**, 1450-1453 (1968).
145. S. Maitrejean, G. Ghezzi, E. Gourvest, G. B. Beneventi, A. Fantini, N. Pashkov, G. Navarro, A. Roule, F. Fillot, P. Noe, S. Lhostis, O. Cueto, C. Jahan, J. F. Nodin, A. Persico, M. Armand, L. Dussault, C. Valle, P. Michallon, R. Morel, A. Brenac, M. Audier, J. Rary, F. Hippert, L. Perniola, V. Sousa, and B. D. Salvo, Phase change memories challenges: a material and process perspective, *IEEE IITC*, 1-3 (2012).
146. N. Yamada, E. Ohno, N. Akahira, K. Nishiuchi, K. Nagata, and M. Takao, High speed overwritable phase change optical disk material, *Jpn. J. Appl. Phys*. **26**, 61-66 (1987).
147. N. Yamada, E. Ohno, K. Nishiuchi, N. Akahira, and M. Takao, Rapid-phase transitions of GeTe-Sb_2Te_3 pseudobinary amorphous thin films for an optical disk memory, *Jpn. J. Appl. Phys*. **69**, 2849-2856 (1991).
148. N. Yamada, Potential of Ge-Sb-Te phase-change optical discs for high data rate recording, *Proc. SPIE*. **3109**, 28-37 (1997).
149. T. Ohta, Phase-change optical memory promotes the DVD optical disk, *J. Optoelecon. Adv. Mater*. **3**, 609-626 (2001).
150. A. V. Kolobov, P. Fons, J. Tominaga, and T. Uruga, Why DVDs work the way they do: The nanometer-scale mechanism of phase change in Ge-Sb-Te alloys, *J. Non-Cryst. Solids*. **352**, 1612-1615 (2006).
151. A. Rong, D. Y. Huang, Y. Lu, Z. Zhang, L. Shi, and R. Wang, Thermal-induced phase-change ODS and photo-excite bistable state-change DVD-RAM, *Proc. ISOP*, pp. 74-81 (1996).
152. K. Nagata, T. Saimi, S. Furukawa, K. Nishiuchi, N. Yamada, and N. Akahira, 4.7 GB phase change optical disk for an authoring system of digital versatile disc, *Jpn. J. Appl. Phys*. **37**, 2236-2240 (1998).
153. X. S. Miao, T. C. Chong, L. P. Shi, P. K. Tan, and F. Li, New additional layer to realize initialization-free function for digital versatile disk random access memory disk, *Jpn. J. Appl. Phys*. **39**, 729-732 (2000).
154. A. V. Kolobov, P. Fons, A. I. Frenkel, A. L. Ankudinov, J. Tominaga, and T. Uruga, Understanding the phase-change mechanism of rewritable optical media, *Nature. Mater*. **3**, 703-708 (2004).
155. M. Wuttig and N. Yamada, Phase-change materials for rewriteable data storage, *Nature. Mater*. **6**, 824-832 (2007).
156. N. Yamada, R. Kojima, M. Uno, T. Akiyama, H. Kitaura, K. Narumi, and K. Nishiuchi, Phase-change material for use in rewritable dual-layer optical disk, *Proc. ISOP*. 2002, 55-63.
157. G. F. Zhou, Materials aspects in phase change optical

recording, *Mater. Sci. Eng: A*. **301**, 73-80 (2001).
158. Y. C. Her, W. T. Tu, and M. H. Tsai, Phase transformation and crystallization kinetics of a-Ge/Cu bilayer for blue-ray recording under thermal annealing and pulsed laser irradiation, *J. Appl. Phys*. **111**, 043503-6 (2012).
159. S. Ou, S. Chen, Y. Lin, C. Wang, and T. Kuo, NiGe thin films for write-once blue laser media, *IEEE T. Magn*. **50**, 1-4 (2014).
160. J. Kim, I. Hwang, H. Kim, and J. Tominaga, Signal characteristics of super-resolution near-field structure disk with 100 GB capacity, *Jpn. J. Appl. Phys*. **44**, 3609-3611 (2004).
161. L. Shi, T. C. Chong, P. K. Tan, J. Li, X. Hu, X. Miao, and Q. Wang, Investigation on super-resolution near-field blu-ray-type phase-change optical disk with Sb_2Te_3 mask layer, *Jpn. J. Appl. Phys*. **44**, 3615-3619 (2005).
162. S. Raoux, C. T. Rettner, J. L. J. Sweet, A. J. Kellock, T. Topuria, P. M. Rice, and D. C. Miller, Direct observation of amorphous to crystalline phase transitions in nanoparticle arrays of phase change materials, *J. Appl. Phys*. **102**, 094305-8 (2007).
163. H. S. Wong, S. Raoux, S. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, and K. E. Goodson, Phase change memory, *Proc. IEEE*, **98**, 2201-2227 (2010).
164. B. Gleixner, A. Pirovano, J. Sarkar, F. Ottogalli, E. Tortorelli, M. Tosi, and R. Bez, Data retention characterization of phase-change memory arrays, *IEEE IRPS*, pp. 542-546 (2007).
165. G. Brune, P. Merkelbach, C. Schlockermann, M. Salinga, M. Wuttig, T. D. Happ, and M. Kund, Nanosecond switching in GeTe phase change memory cells, *Appl. Phys. Lett*. **95**, 043108-3 (2009).
166. M. J. Shu, I. Chatzakis, Y. Kuo, P. Zalden, and A. M. Lindenberg, Ultrafast sub-threshold photo-induced response in crystalline and amorphous GeSbTe thin films, *Appl. Phys. Lett*. **102**, 201903-3 (2013).
167. W. Gawelda, J. Siegel, C. N. Afonso, V. Plausinaitiene, A. Abrutis, and C. Wiemer, Dynamics of laser-induced phase switching in GeTe films, *J. Appl. Phys*. **109**, 123102-7 (2011).
168. Y. Liu, M. M. Aziz, A. Shalini, C. D. Wright, and R. J. Hicken, Crystallization of $Ge_2Sb_2Te_5$ films by amplified femtosecond optical pulses, *J. Appl. Phys*. **112**, 123526-14 (2012).
169. L. Perniola, V. Sousa, A. Fantini, E. Arbaoui, A. Bastard, M. Armand, A. Fargeix, C. Jahan, J.-F. Nodin, A. Persico, D. Blachier, A. Toffoli, S. Loubriat, E. Gourvest, G. B. Beneventi, H. Feldis, S. Maitrejean, S. Lhostis, A. Roule, O. Cueto, G. Reimbold, L. Poupinet, T. Billon, B. D. Salvo, D. Bensahel, P. Mazoyer, R. Annunziata, P. Zuliani, and F. Boulanger, Electrical behavior of phase-change memory cells based on GeTe, *IEEE Electron Dev Lett*. **31**, 488-490 (2010).
170. R. Kojima, S. Okabayashi, T. Kashihara, K. Horal, T. Matsunaga, E. Ohno, N. Yamada, and T. Ohta, Nitrogen doping effect on phase change optical disks, *Jpn. J. Appl. Phys*. **37**, 2098-2103 (1998).
171. R. Kojima and N. Yamada, Acceleration of crystallization speed by Sn addition to Ge-Sb-Te phase-change recording material, *Jpn. J. Appl. Phys*. **40**, 5930-5937 (2001).
172. S. F. Chen, J. K. Chen, and T. P. Chen, Effects of Bi on crystallization in Ge-Sb-Te-Bi, *Mater. Sci. Technol*. **24**, 501-504 (2008).
173. J. H. Sung, C. G. Lee, Y. Z. You, Y. K. Lee, and J. Y. Kim, Bi-Ge-Sb-Te films for reversible phase-change optical recording, *Sol. St. Phen.* **118**, 293-298 (2006).
174. H. Kusada, T. Hosaka, R. Kojima, and N. Yamada, Effect of excess Sb on $GeTe\text{-}Sb_2Te_3\text{-}Bi_2Te_3$ recording films, *Proc. PCOS*, pp. 32-35 (2006).
175. P. K. Khulbe, T. Hurst, M. Horie, and M. Mansuripur, Crystallization behavior of Ge-doped eutectic $Sb_{70}Te_{30}$ films in optical disks, *Appl Optics*. **41**, 6220-6229 (2002).
176. K. Kifune, Y. Kubota, T. Matsunaga, and N. Yamada, Extremely long period-stacking structure in the Sb-Te binary system, *Acta Crystallogr B*. **61**, 492-497 (2005).
177. T. Matsunaga, J. Akola, S. Kohara, T. Honma, K. Kobayashi, E. Ikenaga, and R. Kojima, From local structure to nanosecond recrystallization dynamics in AgInSbTe phase-change materials, *Nature Mater*. **10**, 129-134 (2011).
178. H. Tashiro, M. Harigaya, Y. Kageyama, K. Ito, M. Shinotsuka, K. Tani, and S. Emura, Structural analysis of Ag-In-Sb-Te phase-change material, *Jpn. J. Appl. Phys*. **41**, 3758-3759 (2002).
179. L. V. Pieterson, M. H. R. Lankhorst, M. V. Schijndel, A. E. T. Kuiper, and J. H. J. Roosen, Phase-change recording materials with a growth-dominated crystallization mechanism: A materials overview, *J. Appl. Phys*. **97**, 083520-7 (2005).
180. J. Kalb, F. Spaepen, and M. Wuttig, Atomic force microscopy measurements of crystal nucleation and growth rates in thin films of amorphous Te alloys, *Appl. Phys. Lett*. **84**, 5240-5242 (2004).
181. J. Kalb, F. Spaepen, and M. Wuttig, Kinetics of crystal nucleation in undercooled droplets of Sb- and Te-based alloys used for phase change recording, *J. Appl. Phys*. **98**, 054910-7 (2005).
182. S. Lai and T. Lowrey, OUM-A 180 nm nonvolatile memory cell element technology for stand alone and embedded applications, *IEEE IEDM*, pp. 36.5.1-4 (2001).
183. S. Raoux, W. Welnic, and D. Ielmini, Phase change materials and their application to nonvolatile memories, *Chem. Rev.* **10**, 240-267 (2010).
184. A. Anbarasu and M. Wuttig, Understanding the structure and properties of phase change materials for data storage application, *J. Indian Inst. Sci*. **91**, 259-274 (2011).
185. A. Kolobov and M. Popescu, Phase-change memory: science and applications, *Phys. Stat. Sol. (b)*. **249**, 1824-

1826 (2012).
186. A. Kolobov, P. Fons, J. Tominaga, A. I. Frenkel, A. L. Ankudinov, and T. Uruga, Local structure of Ge-Sb-Te and its modification upon the phase transition, *J. Ovonic Res*. **1**, 21-24 (2005).
187. A. L. Lacaita and D. J. Wouters, Phase-change memories, *Phys. Stat. Sol. (a)*. **205**, 2281-2297 (2008).
188. W. Welnic and M. Wuttig, Reversible switching in phase-change materials, *Mater Today* **11**, 20-27 (2008).
189. D. Adler, H. K. Henisch, and N. Mott, The mechanism of threshold switching in amorphous alloys, *Rev. Mod. Phys*. **50**, 209-220 (1978).
190. D. Adler, M. S. Shur, M. Silver and S. R. Ovshinsky, Threshold switching in chalcogenide-glass thin films, *J. Appl. Phys*. **51**, 3289-3310 (1980).
191. D. Adler, M. S. Shur, M. Silver, and S. R. Ovshinsky, Reply to "Comment on 'Threshold switching in chalcogenide-glass thin films'", *J. Appl. Phys*. **56**, 579-580 (1984).
192. A. Redaelli, A. Pirovano, A. Benvenuti, and A. L. Lacaita, Threshold switching and phase transition numerical models for phase change memory simulations, *J. Appl. Phys*. **103**, 111101-19 (2008).
193. D. Ielmini and Y. G. Zhang, Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices, *J. Appl. Phys*. **102**, 054517-13 (2007).
194. V. G. Karpov, Y. A. Kryukov, S. D. Savransky, and I. V. Karpov, Nucleation switching in phase change memory, *Appl. Phys. Lett*. **90**, 123504-3 (2007).
195. K. Kim, G. Jeong, H. Jeong, and S. Y. Lee, Emerging memory technologies, *IEEE ICICC*, pp. 423-426 (2005).
196. Y. H. Ha, J. H. Yi, H. Horii, J. H. Park, S. H. Joo, S. O. Park, U.-I. Chung, and J. T. Moon, An edge contact type cell for phase change RAM featuring very low power consumption, *IEEE VLSI*, pp. 175-176 (2003).
197. F. Pellizzer, A. Pirovano, F. Ottogalli, M. Magistretti, M. Scaravaggi, P. Zuliani, M. Tosi, A. Benvenuti, P. Besana, S. Cadeo, T. Marangon, R, Morandi, R. Piva, A. Spandre, R. Zonca, A. Modelli, E. Varesi, T. Lowrey, A. Lacaita, G Casagrande, P. Cappelletti, and R. Bez, Novel µtrench phase-change memory cell for embedded and stand-alone non-volatile memory applications, *IEEE VLSI*, pp. 18-19 (2004).
198. F. Pellizzer, A. Benvenuti, B. Gleixner, Y. Kim, B. Johnson, M. Magistretti, T. Marangon, A. Pirovano, R. Bez, and G. Atwood, A 90nm phase change memory technology for stand-alone non-volatile memory applications, *IEEE VLSI*, pp. 122-123 (2006).
199. S. J. Ahn, Y. N. Hwang, Y. J. Song, S. H. Lee, S. Y. Lee, J. H. Park, C. W. Jeong, K. C. Ryoo, J. M. Shin, Y. Fai, J. H. Oh, G. H. Koh, G. T. Jeong, S. H. Joo, S. H. Choi, Y. H. Son, J. C. Shin, K. Kim, H. S. Jeong, and K. Kinam, Highly reliable 50 nm contact cell technology for 256Mb PRAM, *IEEE VLSI*, pp. 98-99 (2005).
200. Y. J. Song, K. C. Ryoo, Y. N. Hwang, C. W. Jeong, D. W. Lim, S. S. Park, J. I. Kim, J. H. Kim, S. Y. Lee, J. H. Kong, S. J. Ahn, S. H. Lee, J. H. Park, J. H. Oh, Y. T. Oh, J. S. Kim, J. M. Shin, Y. Fai, G. H. Koh, G. T. Jeong, R. H. Kim, H. S. Lim, I. S. Park, H. S. Jeong, and K. Kinam, Highly reliable 256Mb PRAM with advanced ring contact technology and novel encapsulating technology, *IEEE VLSI*, pp. 118-119 (2006).
201. T. D. Happ, M. Breitwisch, A. Schrott, J. B. Philipp, M. H. Lee, R. Cheek, T. Nirschi, M. Lamorey, C. H. Ho, S.-H. Chen, C. F. Chen, E. Joseph, S.Zaidi, G. W. Burr, B. Yee, Y. C. Chen, S. Raoux, H. L. Lung, R. Bergmann, and C. Lam, Novel one-mask self-heating pillar phase change memory, *IEEE VLSI*, pp. 120-121 (2006).
202. M. H. R. Lankhorst, B. W. S. M. M. Ketalaars, and R. A. M. Wolters, Low-cost and nanoscale non-volatile memory concept for future silicon chips, *Nature Mater*. **4**, 347-352 (2005).
203. D. Mantegazza, D. Ielmini, E. Varesi, A. Pirovano, and A. L. Lacaita, Statistical analysis and modeling of programming and retention in PCM arrays, *IEEE IEDM*, pp. 311-314 (2007).
204. Y. C. Chen, C. T. Rettner, S. Raoux, G. W. Burr, S.-H. Chen, R. M. Shelby, M. Salinga, W. P. Risk, T. D. Happ, G. M. McClelland, M. Breitwisch, A. Schrott, J. B. Philipp, M. H. Lee, R. Cheek, T. Nirschi, M. Lamorey, C. F. Chen, E. Joseph, S. Zaidi, B. Yee, H. L. Lung, R. Bergmann, and C. Lam, Ultra-thin phase-change bridge memory device using GeSb, *IEEE IEDM*, pp. 1-4 (2006).
205. Y. N. Hwang, S. H. Lee, S. J. Ahn, S. Y. Lee, K. C. Ryoo, H. S. Hong, H. C. Koo, F. Yeung, J. H. Oh, H. J. Kim, W. C. Jeong, J. H. Park, H. Horii, Y. H. Ha, J. H. Yi, G. H. Koh, G. T. Jeong, H. S. Jeong, and K. Kinam, Writing current reduction for high-density phase-change RAM, *IEEE IEDM*, pp. 37.1.1-4 (2003).
206. M. Breitwisch, T. Nirschi, C. F. Chen, Y. Zhu, M. H. Lee, M. Lamorey, G. W. Burr, F. Joseph, A. Schrott, J. B. Philipp, R. Cheek, T. D. Happ, S.-H. hen, S. Zaidi, P. Flaitz, J. Bruley, R. Dasaka, B. Rajendran, S. Rossnage, M. Yang, Y. C. Chen, R. Bergmann, H. L. Lung, and C. Lam, Novel lithography-independent pore phase change memory, *IEEE VLSI*, pp. 100-101 (2007).
207. W. S. Chen, C. Lee, D. S. Chao, Y. C. Chen, F. Chen, C. W. Chen, R. Yen, M. J. Chen, W. H. Wang, T. C. Hsiao, J. T. Yesh, S. H. Chiou, M. Y. Liu, T. C. Wang, L. L. Chein, C. Huang, N. T. Shih, L. S. Tu, D. Huang, T. H. Yu, M. J. Kao, and M. Tsai, A novel cross-spacer phase change memory with ultra-small lithography independent contact area, *IEEE IEDM*, pp. 319-322 (2007).
208. D. H. Im, J. I. Lee, S. L. Cho, H. G. An, D. H. Kim, I. S. Kim, H. Park, D. H. Ahn, H. Horii, S. O. Park, U-I. Chung, and J. T. Moon, A unified 7.5nm dash-type confined cell for high performance PRAM device, *IEEE*

IEDM, pp. 1-4 (2008).
209. M. J. Kang, T. J. Park, Y. W. Kwon, D. H. Ahn, Y. S. Kang, H. Jeong, S. J. Ahn, Y. J. Song, B. C. Kim, S. W. Nam, H. K. Kang, G. T. Jeong, and C. H. Chung, PRAM cell technology and characterization in 20nm node size, *IEEE IEDM*, pp. 3.1.1-4 (2011).
210. Y. Sasago, M. Kinoshita, T. Morikawa, K. Kurotsuchi, S. Hanzawa, T. Mine, A. Shima, Y. Fujisaki, H. Kume, H. Moriya, N. Takaura, and K. Torii, Cross-point phase change memory with $4F^2$ cell size driven by low-contact-resistivity poly-Si diode, *IEEE VLSI*, pp. 24-29 (2009).
211. Y. Fujisaki, Review of emerging new solid-state non-volatile memories, *Jpn. J. Appl. Phys*. **52**, 040001-11 (2013).
212. T. C. Chong, L. P. Shi, R. Zhao, P. K. Tan, J. M. Li, H. K. Lee, X. S. Miao, A. Y. Du, and C. H. Tung, Phase change random access memory cell with superlattice-like structure, *Appl. Phys. Lett*. **88**, 122114-3 (2006).
213. R. Annunzita, P. Zuliani, M. Borghi, G. D. Sandre, L. Scotti, C. Prelini, M. Tosi, I. Tortorelli, and F. Pellizzer, Phase change memory technology for embedded non volatile memory applications for 90nm and beyond, *IEEE IEDM*, pp. 1-4 (2009).
214. Y. Choi, I. Song, M.-H. Park, H. Chung, S. Chang, B. Cho, J. Kim, Y. Oh, D. Kwon, J. Sunwoo, J. Shin, Y. Rho, C. Lee, M-G. Kang, J. Lee, Y. Kwon, S. Kim, J. Kim, Y.-J. Lee, Q. Wang, S. Cha, S. Ahn, H. Horil, J. Lee, K. Kim, H. Joo, K. Lee, Y.-T. Lee, J. Yoo, and G. Jeong, A 20nm 1.8V 8Gb PRAM with 40MB/s program bandwidth, *IEEE ISSCC*, pp. 46-48 (2012).
215. F. Xiong, A. D. Liao, D. Estrada, and E. Pop, Low-power switching of phase-change materials with carbon nanotube electrodes, *Science* **332**, 568-570 (2011).
216. J. Liang, R. G. D. Jeyasingh, H-Y. Chen, and H.-S. P. Wong, A 1.4 μA reset current phase change memory cell with integrated carbon nanotube electrodes for cross-point memory application, *IEEE VLSIT*, pp. 100-101 (2011).
217. I. S. Kim, S. L. Cho, D. H. Im, E. H. Cho, D. H. Kim, G. H. Oh, D. H. Ahn, S. O. Park, S. W. Nam, J. T. Moon, and C. H. Chung, High performance PRAM cell scalable to sub-20nm technology with below $4F^2$ cell size, extendable to DRAM applications, *IEEE VLSIT*, pp. 203-204 (2010).
218. T. Nirschi, J. B. Philipp, T. D. Happ, G. W. Burr, B. Rajendran, M. H. Lee, A. Schrott, M. Yang, M. Breitwisch, C. F. Chen, E. Joseph, M. Larnorey, R. Cheek, S.-H. Chen, S. Zaidi, S. Raoux, Y. C. Chen, Y. Zhu, R. Bergmann, H. L. Lung, and C. Lam, Write strategies for 3 and 4-bit multi-level phase-change memory, *IEEE IEDM*, pp. 461-464 (2007).
219. S. Braga, A. Cabrini, and G. Torelli, Dependence of resistance drift on the amorphous cap size in phase change memory arrays, *Appl. Phys. Lett*. **94**, 092112-3 (2009).
220. Y. Sasago, M. Kinoshita, T. Morikawa, K. Kurotsuchi, S. Hanzawa, T. Mine, A. Shima, Y. Fujisaki, H. Kume, H. Moriya, N. Takaura, and K. Torii, Cross-point phase change memory with $4F^2$ cell size driven by low-contact-resistivity poly-Si diode, *IEEE VLSI*, pp. 24-25 (2009).
221. K. DerChang, S. Tang, I. V. Karpov, R. Dodge, B. Klehn, J. A. Kalb, J. Strand, A. Diaz, N. Leung, J. Wu, S. Lee, T. Langtry, K-W. Chang, C. Pagagianni, J. Lee, J. Hirst, S. Erra, E. Flores, N. Righos, H. Castro, and G. Spadini, A stackable cross point phase change memory, *IEEE IEDM*, 1-4 (2009).
222. G. Tallarida, N. Huby, B. K. Kotowska, S. Spiga, M. Arcari, G. Csaba, P. Lugli, A. Redaelli, and R. Bez, Low temperature rectifying junctions for crossbar non-volatile memory devices, *IEEE IMW*, pp. 1-3 (2009).
223. K.-L. Lin, T.-H. Hou, Y.-J. Lee, J.-H. Lin, J.-W. Chang, J. Shien, C.-T. Chou, W.-H. Chang, W.-Y. Jang, and C.-H. Lin, Low-reset unipolar HfO_2 RRAM and tunable resistive-switching mode via interface engineering, *IEEE ISDRS*, pp. 1-2 (2011).
224. C. Chen, S. Gao, G.-S. Tang, C. Song, F. Zeng, and F. Pan, Cu-embedded AlN-based nonpolar nonvolatile resistive switching memory, *IEEE Electron Dev Lett*. **33**, 1711-1713 (2012).
225. T. W. Hickmott, Low-frequency negative resistance in thin anodic oxide films, *J. Appl. Phys*. **33**, 2669-2682 (1962).
226. K. L. Chopra, Avalanche-induced negative resistance in thin oxide films, *J. Appl. Phys*. **36**, 184-187 (1965).
227. G. Dearnaley, A. M. Stoneham, and D. V. Morgan, Electrical phenomena in amorphous oxide films, *Rep. Prog. Phys*. **33**, 1129-1191 (1970).
228. Y. Lin, L. Jiang, R. Zhao, and C.-W. Nan, High-permittivity core/shell structured NiO-based ceramics and their dielectric response mechanism, *Phys. Rev. B*. **72**, 014103-6 (2005).
229. T.-C. Mo, H.-W. Wang, S.-Y. Chen, and Y.-C. Yeh, Synthesis and dielectric properties of polyaniline/titanium dioxide nanocomposites, *Ceram Int*. **34**, 1767-1771 (2008).
230. D.-H. Kuo, C.-C. Lai, and T.-Y. Su, Dielectric behavior of Nb_2O_5-doped TiO_2/epoxy thick films, *Ceram Int*. **30**, 2177-2181 (2004).
231. J. Koo, Y. Kim, and H. Jeon, ZrO_2 gate dielectric deposited by plasma-enhanced atomic layer deposition method, *Jpn. J. Appl. Phys*. **41**, 3043-3046 (2002).
232. A. Sawa, T. Fujii, M. Kawasaki, and Y. Tokura, Hysteretic current-voltage characteristics and resistance switching at a rectifying $Ti/Pr_{0.7}Ca_{0.3}MnO_3$ interface, *Appl. Phys. Lett*. **85**, 4073-4075 (2004).
233. M. Fujimoto, H. Koyama, M. Konagai, Y. Hosoi, K. Ishihara, S. Ohnishi, and N. Awaya, TiO_2 anatase nanolayer on TiN thin film exhibiting high-speed bipolar resistive switching, *Appl. Phys. Lett.* **89**, 223509-223511 (2006).
234. K. M. Kim, D. S. Jeong, and C. S. Hwang, Nanofilamen-

tary resistive switching in binary oxide system; a review on the present status and outlook, *Nanotechnology* **22**, 254002-17 (2011).
235. H. Y. Jeong, J. Y. Lee, and S.-Y. Choi, Interface-engineered amorphous TiO_2-based resistive memory devices, *Adv. Funct. Mater*. **20**, 3912-3917 (2010).
236. Y. Sakotsubo, M. Terai, S. Kotsuji, Y. Saito, M. Tada, Y. Yabe, and H. Hada, A new approach for improving operating margin of unipolar ReRAM using local minimum of reset voltage, *IEEE VLSI*, pp. 87-88 (2010).
237. I. G. Baek, C. J. Park, H. Ju, D. J. Seong, H. S. Ahn, J. H. Kim, M. K. Yang, S. H. Song, E. M. Kim, S. O. Park, C. H. Park, C. W. Song, G. T. Jeong, S. Choi, H. K. Kang, and C. Chung, Realization of vertical resistive memory (VRRAM) using cost effective 3D process, *IEEE IEDM*, pp. 31.8.1-4 (2011).
238. X. J. Liu, S. M. Sadaf, S. Park, S. Kim, E. Cha, D. Lee, G-Y. Jung, and H. Hwang, Complementary resistive switching in Niobium oxide-based resistive memory devices, *IEEE Electron. Dev. Lett*. **34**, 235-237 (2013).
239. J. Bae, I. Hwang, Y. Jeong, S-O. Kang, S. Hong, J. Son, J. Choi, J. Kim, J. Park, M-J. Seong, Q. Jia, and H. P. Bae, Coexistence of bi-stable memory and mono-stable threshold resistance switching phenomena in amorphous NbO_x films, *Appl. Phys. Lett*. **100**, 062902-4 (2012).
240. Y. T. Li, S. B. Long, M. H. Zhang, Q. Liu, L. B. Shao, S. Zhang, Y. Wang, Q. Y. Zuo, and M. Liu, Resistive switching properties of Au/ZrO_2/Ag structure for low-voltage nonvolatile memory applications, *IEEE Electron Dev. Lett*. **31**, 117-119 (2010).
241. M.-C. Wu, Y.-W. Lin, W.-Y. Jang, C.-H. Lin, T.-Y. Tseng, Low-power and highly reliable multilevel operation in ZrO_2 1T1R RRAM, *IEEE Electron Dev. Lett*. **32**, 1026-1028 (2011).
242. Y.-T. Li, S.-B. Long, H.-B. Lu, Q. Liu, Q. Wang, Y. Wang, S. Zhang, W.-T. Lian, S. Liu, and M. Liu, Investigation of resistive switching behaviours in WO_3-based RRAM devices, *Chinese Phys B*. **20**, 017305-7 (2011).
243. D. S. Shang, L. Shi, J. R. Sun, B. G. Shen, F. Zhuge, R. W. Li, and Y. G. Zhao, Improvement of reproducible resistance switching in polycrystalline tungsten oxide films by in situ oxygen annealing, *Appl. Phys. Lett*. **96**, 072103-3 (2011).
244. D.-S. Shang, L. Shi, J.-R. Sun, and B.-G. Shen, Local resistance switching at grain and grain boundary surfaces of polycrystalline tungsten oxide films, *Nanotechnology* **22**, 254008-7 (2011).
245. W. T. Wu, J. J. Wu, and J. S. Chen, Resistive switching behavior and multiple transmittance states in solution-processed tungsten oxide, *ACS Appl. Mater. Interface* **3**, 2626-2621 (2011).
246. S. Zhang, S. B. Long, Q. Liu, Q. Wang, and M. Liu, Resistive switching characteristics of MnOx-based ReRAM, *ECS T*, **18**, 901-906 (2009).
247. M. K. Yang, J.-W. Park, T. K. Ko, and J.-K. Lee, Bipolar resistive switching behavior in Ti/MnO_2/Pt structure for nonvolatile memory devices, *Appl. Phys. Lett*. **95**, 042105-3 (2009).
248. C.-Y. Lin, C.-Y. Liu, C.-C. Lin, and T. Y. Tseng, Current status of resistive nonvolatile memories, *J. Electroceram*. **21**, 61-66 (2008).
249. S.-G. Park, B. M. Kope, and Y. Nishi, Impact of oxygen vacancy ordering on the formation of a conductive filament in TiO_2 for resistive switching memory, *IEEE Electron. Dev. Lett*. **32**, 197-199 (2011).
250. J. J. Yang, M. D. Picket, X. M. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, Memristive switching mechanism for metal/oxide/metal nanodevices, *Nature Nanotechnol*. **3**, 429-433 (2008).
251. X. Liu, I. Kim, M. Siddik, S. M. Sadaf, K. P. Biju, S. Park, and H. Hwang, Resistive switching mechanism of a $Pr_{0.7}Ca_{0.3}MnO_3$-based memory device and assessment of its suitability for nano-scale applications, *J. Korean. Phys. Soc*. **59**, 497-500 (2011).
252. S. Q. Liu, N. J. Wu, and A. Ignatiev, Electric-pulse-induced reversible resistance change effect in magnetoresistive films, *Appl. Phys. Lett*. **76**, 2749-2751 (2000).
253. P. W. M. Blom, R. M. Wolf, J. F. M. Cillessen, and M. P. C. M. Krijn, Ferroelectric schottky diode, *Phys. Rev. Lett*. **73**, 2107-2110 (1994).
254. P. Maksymovych, S. Jesse, P. Yu, R. Ramesh, A. P. Baddorf, and S. V. Kalinin, Polarization control of electron tunneling into ferroelectric surfaces, *Science* **324**, 1421-1425 (2009).
255. S. Duhalde, M. Villafuerte, G. Juarez, and S. P. Heluani, Electric field-driven resistive switching in magnetoresistive $La_{0.5}Ca_{0.5}MnO_3$ thin films, *Physica B* **354**, 11-15 (2004).
256. R. Dong, Q. Wang, L. D. Chen, D. S. Shang, T. L. Chen, X. M. Li, and W. Q. Zhang, Retention behavior of the electric-pulse-induced reversible resistance change effect in Ag-$La_{0.7}Ca_{0.3}MnO_3$-Pt Sandwiches, *Appl. Phys. Lett*. **86**, 172107-3 (2005).
257. K. Szot, W. Speier, G. Bihlmayer, and R. Waser, Switching the electrical resistance of individual dislocations in single-crystalline $SrTiO_3$, *Nature Mater*. **5**, 312-320 (2006).
258. C. H. Cheng, A. Chin, and F. S. Yeh, Ultralow-power Ni/GeO/STO/TaN resistive switching memory, *IEEE Electron Dev Lett*. **31**, 1020-1022 (2010).
259. A. Beck, J. G. Bednorz, C. Gerber, C. Rossel, and D. widmer, Reproducible switching effect in thin oxide films for memory applications, *Appl. Phys. Lett*. **77**, 139-141 (2000).
260. C.-C. Lin, C.-C. Lin, B.-C. Tu, J.-S. Yu, C.-H. Lin, and T.-Y. Tseng, Resistive switching properties of $SrZrO_3$-based memory films, *Jpn. J. Appl. Phys*. **46**, 2153-2156 (2007).
261. Y. Fujisaki, Review of emerging new solid-state non-vol-

atile memories, *Jpn. J. Appl. Phys*. **46**, 2153-2156 (2007).
262. A. Odagawa, H. Sato, I. H. Inoue, H. Akoh, M. Kawasaki, and Y. Tokura, Colossal electroresistance of a $Pr_{0.7}Ca_{0.3}MnO_3$ thin film at room temperature, *Phys. Rev. B*. **70**, 224403-4 (2004).
263. S. Tsui, A. Baikalov, J. Cmaidalka, Y. Y. Sun, Y. Q. Wang, Y. Y. Xue, C. W. Chu, L. Chen, and A. J. Jacobson, Field-induced resistive switching in metal-oxide interfaces, *Appl. Phys. Lett*. **85**, 317-319 (2004).
264. C. Papagianni, Y. B. Nian, Y. Q. Wang, N. J. Wu, and A. Ignatiev, Impedance study of reproducible switching memory effect, *IEEE NVMT*, pp. 125-128 (2004).
265. A. Q. Jiang, C. Wang, K. J. Jin, X. B. Liu, J. F. Scott, C. S. Hwang, T. A. Tang, H. B. Lu, and G. Z. Yang, A resistive memory in semiconducting $BiFeO_3$ thin-film capacitors, *Adv. Mater*. **23**, 1277-1281 (2011).
266. R. Waser, R. Dittmann, G. Staikov, and K. Szot, Redox-based resistive switching memories-nanoionic mechanisms, prospects, and challenges, *Adv. Mater*. **21**, 2632-2663 (2009).
267. F. Pan, C. Chen, Z.-S. Wang, Y.-C. Yang, J. Yang, and F. Zeng, Nonvolatile resistive switching memories-characteristics, mechanisms and challenges, *Prog. Nat. Sci*. **20**, 1-15 (2010).
268. M. Kund, G. Beitel, C.-U. Pinnow, T. Rohr, J. Schumann, R. Symanczyk, K.-D. Ufert, and G. Muller, Conductive bridging RAM (CBRAM): an emerging non-volatile memory technology scalable to sub 20nm, *IEEE IEDM*, pp. 754-757 (2005).
269. M. N. Kozicki, M. Park, and M. Mitkova, Nanoscale memory elements based on solid-state electrolytes, *IEEE T. Nanotechnol*. **4**, 331-338 (2005).
270. T. Sakamoto, H. Sunamura, H. Kawaura, T. Hasegawa, T. Nakayama, and M. Aono, Nanometer-scale switches using copper sulfide, *Appl. Phys. Lett*. **82**, 3032-3034 (2003).
271. J. Park, W. Lee, M. Choe, S. Jung, M. Son, S. Kim, S. Park, J. Shin, D. Lee, M. Siddik, J. Woo, G. Choi, E. Cha, T. Lee, and H. Hwang, Quantized conductive filament formed by limited Cu source in sub-5nm era, *IEEE IEDM*, pp. 3.7.1-4 (2011).
272. T. Sakamoto, N. Banno, N. Iguchi, H. Kawaura, H. Sunamura, S. Fujieda, K. Terabe, T. Hasegawa, and M. Aono, A Ta_2O_5 solid-electrolyte switch with improved reliability, *IEEE VLSI*, pp. 38-39 (2007).
273. T. Lee and Y. Chen, Organic resistive nonvolatile memory materials, *MRS Bull.* **37**, 144-149 (2012).
274. Z. J. Donhauser, B. A. Mantooth, K. F. Kelly, L. A. Bumm, J. D. Monnell, J. J. Stapleton, D. W. Price Jr, A. M. Rawlett, D. L. Allara, J. M. Tour, and P. S. Weiss, Conductance switching in single molecules through conformational changes, *Science*, **292**, 2303-2307 (2001).
275. A. Bandyopadhyay and A. J. Pal, Multilevel conductivity and conductance switching in supramolecular structures of an organic molecule, *Appl. Phys. Lett.* **84**, 999-1001 (2004).
276. B. C. Das and A. J. Pal, Switching between different conformers of a molecule: Multilevel memory elements, *Org. Electron*. **1**, 39-44 (2008).
277. C. N. Lau, D. R. Stewart, R. S. Williams, and M. Bockrath, Direct observation of nanoscale switching centers in metal/molecule/metal structures, *Nano Lett*. **4**, 569-572 (2004).
278. Y. Yang, J.-Y. Uuyang, L.-P. Ma, R. J.-H. Tseng, and C.-W. Chu, Electrical switching and bistability in organic/polymeric thin films and memory devices, *Adv. Fun. Mater*. **16**, 1001-1014 (2006).
279. S. H. Kim, K. S. Yook, J. Jang, and J. Y. Lee, Correlation of memory characteristics of polymer bistable memory devices with metal deposition process, *Synth. Met*. **158**, 861-864 (2008).
280. H. S. Majumdar, A. Bandyopadhyay, A. Bolognesi, and A. J. Pal, Memory device applications of a conjugated polymer: role of space charges, *J. Appl. Phys*. **91**, 2433-2437 (2002).
281. S. L. Lim, D. Qi, E. Y. H. Teo, C. X. Zhu, D. S. H. Chan, E. Tang, and K. G. Neoh, Conformation-induced electrical bistability in non-conjugated polymers with pendant carbazole moieties, *Chem. Mater*. **19**, 5148-5157 (2007).
282. D.-I. Son, J.-H. Kim, D.-H. Park, W. K. Choi, F. Li, J. H. Ham, and T. W. Kim, Nonvolatile flexible organic bistable devices fabricated utilizing CdSe/ZnS nanoparticles embedded in a conducting poly N-vinylcarbazole polymer layer, *Nanotechnology* **19**, 055204-5 (2008).
283. D. T. Simon, M. S. Griffo, R. A. DiPietro, S. A. Swanson, and S. A. Carter, Admittance spectroscopy of polymer-nanoparticle nonvolatile memory devices, *Appl. Phys. Lett*. **89**, 133510-133512 (2006).
284. Y. Song, Q. D. Ling, S. L. Lim, E. Y. H. Teo, Y. P. Tan, L. Li, E. T. Kang, D. S. H. Chan, and C. X. Zhu, Electrically bistable thin-film device based on PVK and GNPs polymer material, *IEEE Electron. Dev. Lett*. **28**, 107-110 (2007).
285. P. Y. Lai and J. S. Chen, Electrical bistability and charge transport behavior in Au nanoparticle/poly(N-vinylcarbazole) bybrid memory devices, *Appl. Phys. Lett*. **93**, 153305-153307 (2008).
286. W. J. Joo, T. L. Choi, K. H. Lee, and Y. Chung, Study on threshold behavior of operation voltage in metal filament-based polymer memory, *J. Phys. Chem B*. **111**, 7756-7760 (2007).
287. S. Sivaramakrishnan, P. J. Chia, Y. C. Yeo, L. L. Chua, and P. K. Ho, Controlled insulator-to-metal transformation inprintable polymer composites with nanometal clusters, *Nature Mater*. **6**, 149-155 (2007).
288. A. Carbone, B. K. Kotowska, and D. Kotowski, Space-charge-limited current fluctuations in organic semiconductors, *Phys. Rev. Lett*. **95**, 236601-4 (2005).
289. E. I. Kamitsos, C. H. Tzinis, and W. M. Jr. Risen, Raman

study of the mechanism of electrical switching in Cu TCNQ films, *Solid. State. Commun*. **42**, 561-565 (1982).
290. C. W. Chu, J. Ouyang, J. H. Tseng, and Y. Yang, Organic donor-acceptor system exhibiting electrical bistability for use in memory devices, *Adv. Mater*. **17**, 1440-1443 (2005).
291. E. Y. H. Teo, Q. D. Ling, Y. Song, Y. P. Tan, W. Wang, E. T, Kang, D. S. H. Chan, and C. X. Zhu, Non-volatile WORM memory device based on an acrylate polymer with electron donating carbazole pendant groups, *Org. Electron*. **7**, 173-180 (2006).
292. E. Linn, R. Rosezin, C. Kugeler, and R. Waser, Complementary resistive switches for passive nanocrossbar memories, *Nature Mater*. **9**, 403-406 (2010).
293. J. J. Yang, M.-X. Zhang, J. P. Strachan, F. Miao, M. D. Pickett, R. O. Kelley, G. M. Ribeiro, and R. S. Williams, High switching endurance in TaO_x memristive devices, *Appl. Phys. Lett*. **97**, 232102-3 (2010).
294. C. Kugeler, J. Zhang, S. H. Eifert, S. K. Kim, and R. Waser, Nanostructured resistive memory cells based on 8-nm-thin TiO_2 films deposited by atomic layer deposition, *J. Vac. Sci. Technol. B*. **29**, 01AD01-05 (2011).
295. C. Ho, C. Hsu, C. Chen, J. Liu, C. Wu, C. Huang, C. Hu, and F. Yang, 9 nm half-pitch functional resistive memory cell with 1 mA programming current using thermally oxidized sub-stoichiometric WO_x film, *IEEE IEDM*, pp. 19.1.1-4 (2010).
296. B. Govoreanu, G. S. Kar, Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I. P. Radu, L. Goux, S. Clima, R. Degraeve, N. Jossart, H. Bender, L. Altimimi, D. J. Wouters, J. A. Kittl, and M. Jurczak, $10 \times 10\ nm^2$ Hf/HfO × crossbar resistive RAM with excellent performance, reliability and low-energy operation, *IEEE IEDM*, pp. 31-36 (2011).
297. A. C. Torrezan, J. P. Strachan, G. Medeiros-Ribeiro, and R. S. Williams, Sub-nanosecond switching of a tantalum oxide memristor, *Nanotechnology* **22**, 485203-7 (2011).
298. B. J. Choi, A. C. Torrezan, K. J. Norris, F. Miao, J. P. Strachan, M.-X. Zhang, D. A. A. Ohlberg, N. P. Kobayashi, J. J. Yang, and R. S. Williams, Electrical performance and scalability of Pt dispersed SiO_2 nanometallic resistance switch, *Nano Lett.* **13**, 3213-3217 (2013).
299. C. H. Cheng, C. Y. Tsai, A. Chin, and F. S. Yeh, High performance ultra-low energy RRAM with good retention and endurance, *IEEE IEDM*, pp. 448-451 (2010).
300. M-J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. B. Kim, C. J. Kim, D. H. Seo, S. Seo, U. I. Chung, I. K. Yoo, and K. Kim, A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta_2O_{5-x}/TaO_{2-x} bilayer structures, *Nature. Mater*. **10**, 625-630 (2011).
301. S. Gao, F. Zeng, C. Chen, G.-S. Tang, Y. Lin, Z. Zheng, C. Song, and F. Pan, Conductance quantization in a Ag filament-based polymer resistive memory, *Nanotechnology* **24**, 335201-7 (2013).
302. Y. Wang, Q. Liu, S. Long, W. Wang, Q. Wang, M. Zhang, S. Zhang, Y. Li, Q. Zuo, J. Yang, and M. Liu, Investigation of resistive switching in Cu-doped HfO_2 thin film for multilevel non-volatile memory applications, *Nanotechnology* **21**, 045202-5 (2010).
303. C. L. He, Z. W. Shi, L. C. Zhang, W. Yang, R. Yang, D. X. Shi, and G. Y. Zhang, Multilevel resistive switching in planar grapheme/SiO_2 nanogap structures, *ACS Nano*. **6**, 4214-4221 (2012).
304. F. Pan, S. Gao, C. Chen, C. Song, and F. Zeng, Recent progress in resistive random access memories: Materials, switching mechanisms, and performance, *Mater. Sci. Eng R*. **83**, 1-59 (2014).
305. H. Yamada, V. Garcia, S. Fusil, S. Boyn, M. Marinova, A. Gloter, and A. Barthelemy, Giant electroresistance of super-tetragonal $BiFeO_3$-based ferroelectric tunnel junctions, *ACS Nano*. **7**, 5385-5390 (2013).
306. H. Noguchi, K. Kushida, K. Ikegami, K. Abe, E. Kitagawa, S. Kashiwada, C. Kamata, A. Kawasumi, H. Kara, and S. Fujita, A 250-MHz 255b-I/O 1-Mb STT-MRAM with advanced perpendicular MTJ based dual cell for nonvolatile magnetic caches to reduce active power of processors, *IEEE VLSI*, pp. 108-109 (2013).
307. F. Xiong, M.-H. Bae, Y. Dai, A. D. Liao, A. Behnam, E. Carrion, S. Hong, D. Ielmini, and E. Pop, Nanowire phase change memory with carbon nanotube electrodes, *IEEE DRC*, pp. 215-216 (2012).
308. J. J. Yang, D. B. Strukov, and D. R. Stewart, Memristive devices for computing, *Nature Nanotechnol*. **8**, 13-24 (2013).
309. H. Y. Chen, S. M. Yu, B. Gao, P. Huang, J. F. Kang, and H.-S. P. Wong, HfO_x based vertical resistive random access memory for cost-effective 3D cross-point architecture without cell selector, *IEEE IEDM*, pp. 497-500 (2012).