Electron. Mater. Lett., Vol. 10, No. 6 (2014), pp. 1045-1049
DOI: 10.1007/s13391-014-4021-x

Optimisation of Readout Performance of Phase-Change Probe Memory in Terms of Capping Layer and Probe Tip

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(received date: 14 January 2014 / accepted date: 5 March 2014 / published date: 10 November 2014)

The capping layer and the probe tip that serve as the protective layer and the recording tool, respectively, for phase-change probe memory play an important role on the writing performance of phase-change probe memory, thus receiving considerable attention. On the other hand, their influence on the readout performance of phase-change probe memory has rarely been reported before. A three-dimensional parametric study based on the Laplace equation was therefore conducted to investigate the effect of the capping layer and the probe tip on the resulting reading contrast for the two cases of reading a crystalline bit from an amorphous matrix and reading an amorphous bit from a crystalline matrix. The results indicated that a capping layer with a thickness of 2 nm and an electrical conductivity of 50 $\Omega^{-1}m^{-1}$ is able to provide an appropriate reading contrast for both the cases, while satisfying the previous writing requirement, particularly with the assistance of a platinum silicide probe tip.

Keywords: capping layer, probe tip, reading contrast, phase-change probe memory, readout

1. INTRODUCTION

A drastic increase in the amount of information created and reproduced in digital form has been recently witnessed. Digital data growth has resulted in the breaking of the Zettabyte barrier in 2012, and a growth factor of 300 from 2005 to 2020 is predicted.[1] This extent of growth urgently demands a remarkable increase in the storage capacity of the currently used mass storage devices. Unfortunately, the current mainstream forms of storage technologies such as magnetic hard disks, optical storage discs, and Flash memory suffer from the super paramagnetic limit,[2,3] optical diffraction limit,[4,5] and device scaling limits,[6,7] respectively. Therefore, considerable research has been performed to develop new alternative memory technologies, to satisfy consumer and industry requirements. Phase-change probe memory, a promising emerging storage technology, has recently gained enormous interest because of its ability to provide ultra-high density under ultra-low energy consumption conditions within an ultra-short time scale.[8-20] In phase-change probe memory, recording is realised by injecting a pulse of electrical current from the conductive tip into the chalcogenide alloy, particularly $Ge_2Sb_2Te_5$ (GST) media. This pulse facilitates the phase transformation between amorphous and crystalline states according to Joule heating, and a change in the electrical resistivity in these two phases can be detected by means of the readout current, which is used to achieve the readout process. Figure 1 shows the principles of the writing and readout processes of phase-change probe memory.

A typical phase-change probe memory system consists of a recording tip and a storage media stack, as shown in Fig. 2. It is obvious that the probe tip plays an important role in

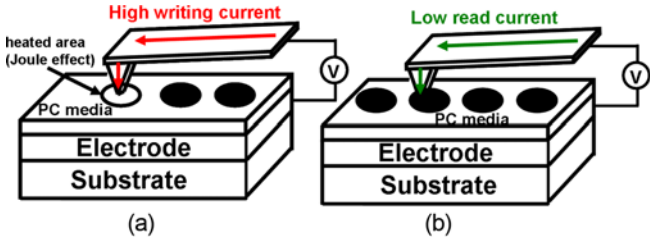

Fig. 1. Schematic of phase-change probe memory when operated in (a) the writing mode and (b) the readout mode.

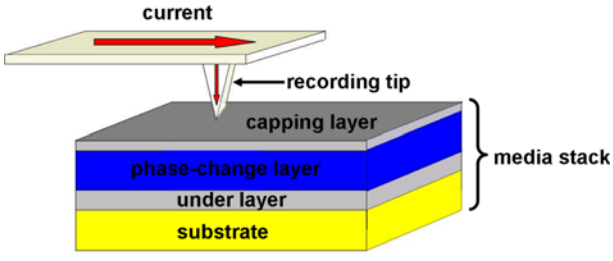

Fig. 2. Typical architecture of phase-change probe memory.

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determining the achievable density of phase-change probe memory that significantly depends on the electrical contact area between the probe tip and phase-change media.[21] Therefore, a probe tip that has a high electrical conductivity and fairly low thermal conductivity with a small diameter electrical contact is essential to achieve high-density recording under low energy consumption conditions.[22] The media stack comprises a GST layer that is sandwiched by a capping layer and an under layer, which are deposited on silicon (Si) substrate. The capping layer can not only protect the GST layer from wear and corrosion, but also strongly influence the resulting electric field and temperature distribution inside the GST layer.[8,10,11] As suggested by previous studies,[8,10,11] a thin diamond-like-carbon (DLC) capping layer with high mechanical hardness, relatively high electrical conductivity, and fairly low thermal conductivity is required in order to generate a sufficiently high temperature in the GST layer for the required phase transformation while keeping the energy consumption low. It should be noted that the aforementioned specifications are applicable only to the optimisation of the writing performance of phase-change probe memory, whereas their utility for optimising the subsequent readout performance after the writing process has rarely been assessed. In this study, to assess the effect of the capping layer and probe tip on the resulting readout signal, and thus to provide phase-change probe memory with an optimal readout performance, a three-dimensional (3D) readout model has been developed. The readout signal is evaluated by varying the electrical conductivity and thickness of the capping layer as well as the electrical conductivity of the probe tip, as discussed below.

2. EXPERIMENTAL PROCEDURE

Two readout configurations are taken into account here, i.e. reading a crystalline bit from an amorphous matrix and reading an amorphous bit from a crystalline matrix. The simulated crystalline bit is assumed to have a cylindrical shape with a diameter of 20 nm that extends through the entire GST layer. On the other hand, the amorphous bit also has a 20 nm diameter but is assumed to be of a semi-ellipsoidal shape located on the top portion of the GST layer. The bit shapes and diameter adopted for this study are based on previous writing simulations.[8,10,11] The readout potential is considered as 2 V to eliminate any re-writing effect on the previously written bit. The electrical conductivities of the crystalline bit and amorphous bit are assigned to be 1000 $\Omega^{-1}m^{-1}$ and 0.1 $\Omega^{-1}m^{-1}$, respectively. The thickness and electrical conductivity of the DLC capping layer investigated here vary from 2 nm to 5 nm and 1 $\Omega^{-1}m^{-1}$ to 10000 $\Omega^{-1}m^{-1}$ to cover the range of possible values reported in the literature.[23-26] Two types of commercial probe tips, i.e. the DLC tip with an electrical conductivity of 3.3×10^4 $\Omega^{-1}m^{-1}$ and the platinum silicide (PtSi) tip with an electrical conductivity of 3.3×10^6 $\Omega^{-1}m^{-1}$, are used in the simulation because of their superior characteristics compared to other commercial probe tips.[27,28] The tip diameter is assumed to be 20 nm, which may prove challenging for fabrication but is already well established.[21] Note that a parameter that is often used to compare readout signals with very different average values is the reading contrast, defined as $I_{max} - I_{min}/I_{max} + I_{min}$ (where I_{max} and I_{min} denote the maximum and minimum readout currents during the readout process, respectively). The Laplace equation has been introduced into this model exclusively to calculate the resulting readout current that is subsequently converted to the reading contrast. Figure 3 shows the simulation geometry for the two configurations.

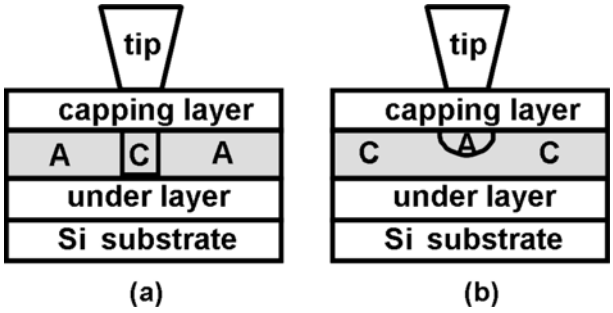

Fig. 3. Cross section of the readout configuration having (a) a crystalline bit extending through the entire thickness and (b) an amorphous bit localised on the top portion of GST layer. The thickness and electrical conductivity of the under layer are 10 nm and 100 $\Omega^{-1}m^{-1}\Omega^{-1}m^{-1}$, respectively. The thickness of GST layer is 30 nm.

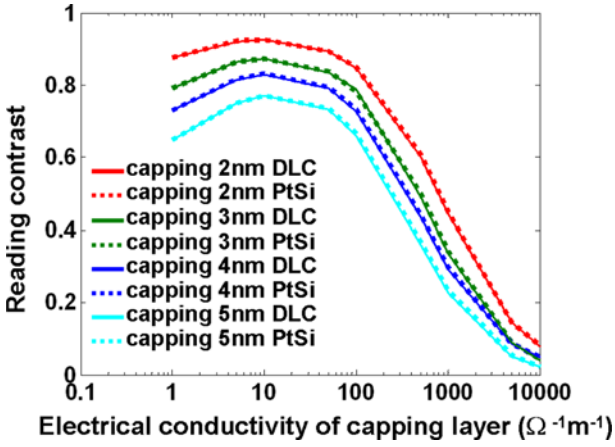

Fig. 4. Reading contrast as a function of the probe tip, capping layer electrical conductivity, and capping layer thickness for a single crystalline bit extending through the entire thickness.

3. RESULTS AND DISCUSSION

The reading contrast for reading a single crystalline bit from the surrounding amorphous matrix based on the

geometry in Fig. 3(a) is presented in Fig. 4 for different thicknesses and electrical conductivities of the capping layer as well as for different tips.

As seen in Fig. 4, the reading contrast is increased by reducing the thickness of the capping layer, as this would decrease the spreading resistance, thus allowing for a higher readout current signal. A 2-nm-thick capping layer with an electrical conductivity of 10 $\Omega^{-1}m^{-1}$ would result in a reading contrast of approximately 0.92. It should however be noted that a reading contrast higher than 0.5 can be achieved by using even a 5-nm-thick capping layer, giving confidence in applying the thick capping layer (thickness > 5 nm) to probe technology, as the feasibility of fabricating a uniform, very thin capping layer (thickness < 2 nm) is uncertain.[29] In addition, the reading contrast exhibits an interesting trend with the changing electrical conductivity of the capping layer. The reading contrast increases when the electrical conductivity of the capping layer varies from 1 $\Omega^{-1}m^{-1}$ to 10 $\Omega^{-1}m^{-1}$, subsequently decreasing when the capping layer electrical conductivity ranges from 10 $\Omega^{-1}m^{-1}$ to 10000 $\Omega^{-1}m^{-1}$. Obviously, the initial increase in the reading contrast is expected as the spreading resistance of the capping layer is reduced, inducing a higher readout signal. When the electrical conductivity of the capping layer increases further, the amount of the leakage current through the crystalline bit (in this case, the tip is on the surface of the amorphous region) is also increased owing to the formation of a short circuit. Therefore, the magnitude difference between I_{min} and I_{max} decreases along with the increase in the electrical conductivity of the capping layer, thus resulting in a decrease in the reading contrast. It is noteworthy that reading contrast is unaffected by the type of tips. This is because the resistance of the both the DLC and the PtSi tips is significantly less than that of the phase-change stack and thus has a little influence on the distribution of the voltage drop across the GST layer.

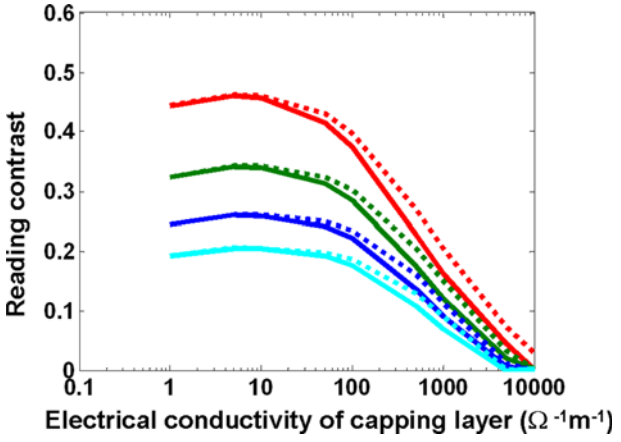

Fig. 5. Reading contrast as a function of the probe tip, capping layer electrical conductivity, and capping layer thickness for a single amorphous bit on the top portion of the GST layer. Figure legend is as for Fig. 4.

In addition to the above study, the reading contrast for reading an amorphous bit from the crystalline background using the configuration in Fig. 3(b) was also investigated by varying the thickness and the electrical conductivity of the capping layer under the use of DLC tip and PtSi tips.

As shown in Fig. 5, the maximum reading contrast obtained from reading an amorphous bit on the top portion of the GST layer is approximately 0.48, compared to the value of 0.92 obtained for the crystalline bit extending through the entire GST thickness. In addition, the reading contrast is reduced by increasing the thickness of the capping layer, similar to the observation in the previous case. Figure 5 also indicates that the relationship between the reading contrast and the electrical conductivity of the capping layer is slightly different when using different probe tips. For both tips, the reading contrast is increased when the electrical conductivity of the capping layer increased from 1 $\Omega^{-1}m^{-1}$ to 10 $\Omega^{-1}m^{-1}$. This is expected as increasing the electrical conductivity of the capping layer can lead to a higher readout current. When the electrical conductivity of the capping layer is above 10 $\Omega^{-1}m^{-1}$, the readout contrast starts to decrease. This decrease in the readout contrast can still be attributed to the current leakage through the crystalline matrix when the tip is on the top of the amorphous bit. It should be also noted that for a capping layer, there is no difference between the reading contrast values observed with the PtSi tip and DLC tips when the electrical conductivity of the capping layer is less than approximately 5 $\Omega^{-1}m^{-1}$, whereas the reading contrast of the PtSi tip is greater than that of the DLC tip when the electrical conductivity of the capping layer is greater than 5 $\Omega^{-1}m^{-1}$. Note that the capping layer properties such as thickness and thermal conductivity, remain same for both probes. This is because the spreading resistance is mainly determined by the capping layer whose electrical conductivity is less than 5 $\Omega^{-1}m^{-1}$, and in this case, the electrical conductivity of the tip plays a minor role in determining the readout current. When the electrical conductivity of the capping layer exceeds 5 $\Omega^{-1}m^{-1}$, the influence of the capping layer on the spreading resistance is lessened and thus the probe tip starts to make a noticeable contribution to the spreading resistance.

The comparison between Figs. 4 and 5 clearly reveals that using a thinner capping layer is required to achieve a higher reading contrast for both configurations, while the capping layer should not be very electrically conductive, since this would cause a reduction on the reading contrast. In addition, using a probe tip with a high electrical conductivity when combined with an appropriate electrical conductivity of the capping layer can also bring about some positive effects on the reading contrast. According to above analysis, a capping layer with a thickness of 2 nm and an electrical conductivity between 10 $\Omega^{-1}m^{-1}$ and 100 $\Omega^{-1}m^{-1}$ are able to provide

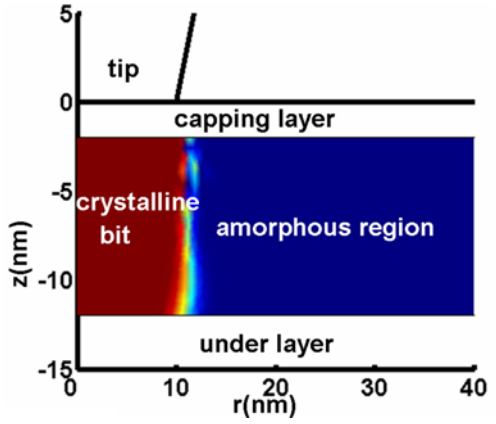

Fig. 6. Crystalline bit realised using the designed optimal media stack by a 5 V pulse of 100 ns duration. The thickness and electrical conductivity of the capping layer are 2 nm and 50 $\Omega^{-1}m^{-1}$, respectively, and the PtSi tip is used for recording bits. Other parameters can be obtained from.[8]

maximum reading contrast for both configurations, particularly with the help of the PtSi probe tip. However, because a relatively high electrical conductivity of the capping layer is usually desired for achieving satisfactory writing performance by reducing the power consumption, the optimal electrical conductivity of the capping layer is chosen here to be 50 Ω^{-1} m^{-1}, which is an intermediate value between 10 $\Omega^{-1}m^{-1}$ and 100 $\Omega^{-1}m^{-1}$.

Although the utilisation of this proposed probe system allows for optimisation of the readout performance, the capability of bit writing using the same probe system has yet to be examined. In this study, the write performance of the designed probe system has been investigated using a previously developed computational model consisting of the (time-resolved) Laplace equation, heat conduction equation, and Johnson-Mehl-Avrami-Kolmogorov (JMAK) equation,[30] resulting in the diagram shown in Fig. 6. Circular symmetry is assumed in this model so that a full 3D- simulation reduces to two dimensions. Figure 6 clearly shows that a perfectly cylindrical crystalline bit with a diameter of approximately 20 nm that extends through the entire recording layer has been produced. This allows for tera bit per square inch storage density in conjunction with a good readout signal. At the same time, the power consumed by the writing process to write such a bit is around 0.13 mW, indicating a remarkably lower power consumption compared to the thermo-mechanical probe storage (3 mW)[31] and thermal probe storage (0.5 mW)[18] for bits of approximately the same size.

4. CONCLUSIONS

The readout performance of phase-change probe memory has been studied in terms of the reading contrast by varying the thickness and electrical conductivity of the capping layer for two different probe tips. The results showed that using a capping layer with a thickness of 2 nm and an electrical conductivity of 50 $\Omega^{-1}m^{-1}$ in conjunction with a PtSi tip, can provide maximum reading contrast for both reading a crystalline bit from an amorphous matrix and reading an amorphous bit from a crystalline matrix. The write capability of this optimal probe system to provide ultra-high recording density with ultra-low power consumption in an ultra-fast time duration was also demonstrated.

ACKNOWLEDGEMENTS

The authors acknowledge the financial supports of the National Natural Science Foundation of China (grant No. 61201439, 61272077) and the Technical Funding Program of National Human Resource Ministry of China for returned oversea Chinese scholars.

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