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Resistive Switching and Current Conduction Mechanism in Full Organic Resistive Switch with the Sandwiched Structure of Poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate)/Poly(4-vinylphenol)/Poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate)

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The paper reported the fabrication of full organic resistive switch (FORS) with the sandwich structure of poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate)(PEDOT:PSS)/poly(4-vinylphenol)(PVP)/poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate)(PEDOT:PSS). The fabricated FORS elucidated reversible bipolar resistive switching behavior at higher operational voltage between −20 V and +30 V. The switching mechanism in the FORS device was attributed to the hole injection through PEDOT:PSS electrode and filling of trap sites in the PVP sandwiched layer by the limited injection. Current conduction mechanisms were concluded and supported by the charge transport governing physical laws. The dominant current conduction mechanism in the fabricated FORS was attributed to the transition from trap-limited space charge limited current (SCLC) conduction to trap-free SCLC conduction mechanism. The robustness of the fabricated FORS was tested over 100 multiple voltage sweeps.

Keywords: Bipolar resistive switching, current conduction mechanism, organic resistive switch

1. INTRODUCTION

Resistive switches have rigorously been researched to be employed in device application due to their fast switching speed, small size, and simple device structure.[1-10] Organic materials sandwiched between two electrodes, whose resistance could be modulated by the external voltage source having the potential to store at least two stable states, are the promising candidates for the next generation organic memory and electrical switching applications.[11,12] Healthy efforts have been exercised in literature to review the materials, structures, characteristics, and mechanism of organic resistive memory devices.[11,13,14] Organic resistive switches have been fabricated based on four device structures: (1) single layer structure containing only single organic layer,[15] (2) bilayer structure containing two different organic materials,[16] (3) trilayer structure containing nano-traps buried between two organic materials,[17] and (4) polymer-nanoparticle (NP) composite structure with NP-traps randomly distributed throughout the entire host layer.[18] To show the resistive switching characteristics, each of the four organic structures is implemented by sandwiching between two metallic/conducting electrodes. Metallic electrodes limit the promising feasibility of the organic resistive switches to be employed in electronic industry at their full potential regarding the perspective of organic material advantages. So, engineering of the full organic devices has always been in great demand in electronic applications by virtue of their simple device structure, low fabrication cost, printability, and flexibility.

In this research work, the fabrication of full organic resistive switch (FORS) was realized with all of its layers (electrodes as well as switching layer) as organic as opposed to the conventional organic resistive devices in which the electrode-materials were inorganic (metallic or ITO etc). Although hybrid resistive switches (structure containing organic as well as inorganic materials) have been reported in literature but to date, no one has reported FORS devices for resistive switching and memory applications. The fabricated FORS device has great potential to revolutionize the electronics industry by shifting the inorganic/hybrid devices to their organic counterparts. In consequence, the electronic devices would not face fabrication limitations such as high temperature deposition, high capital cost, lack of printability and flexibility etc. This paper reports the fabrication of FORS devices by spin coating of two polymers: poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) and poly(4-vinylphenol) (PVP) on a polyimide (PI) substrate. PEDOT:PSS is a conjugated polymer consisted of two polymeric chains: poly(3,4-ethylenedioxythiophene) (PEDOT) and poly(styrenesulfonate) (PSS). PEDOT:PSS has been known as transparent and conductive in nature in polymeric

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science.[19-22] PEDOT:PSS was used as conducting top and bottom electrodes for the FORS fabrication in this study. Poly(4-vinylphenol) (PVP) is another common polymer being used as a dielectric, a cross-linking agent and has also been used as a switching layer in resistive switching memory applications.[23-26] PVP was employed as a switching layer between two PEDOT:PSS electrodes for the fabrication of the FORS in this research work.

The resistance of the PVP layer, sandwiched between two conducing PEDOT:PSS electrodes, was modulated by the semiconductor device analyzer to elucidate the resistive switching behavior in the fabricated FORS. The robustness of the stable resistive switching was evidenced through stressing the device with multiple voltage sweeps. Resistive switching mechanism was described in the fabricated FORS devices. The current conduction behavior, governing the device resistance, was concluded based on slopes calculation in the double logarithmic graphs. The current conduction mechanisms were validated through physical current conduction laws. The suggested resistive switching mechanism was correlated with the concluded current conduction behavior in the fabricated FORS.

2. EXPERIMENTAL PROCEDURE

Chemically modified PEDOT:PSS ink with isopropanol and deionized water[19] was used to deposit the top and bottom conducting electrodes. The switching layer between two PEDOT:PSS electrodes was deposited by the PVP polymeric ink purchased from Sigma-Aldrich.

The reported FORS device, as shown in Fig. 1, was fabricated by spin coating process. Initially the bottom electrode was deposited by spin coating the PEDOT:PSS ink on the PI substrate at 700 rpm. The sample was cured at 110°C for 1 h. After curing process, the sandwich layer was deposited by spin coating the PVP polymeric ink on the PEDOT:PSS bottom electrode at the same parameters listed above. Again, curing of the deposited sample was performed at 110°C for 1 h. The top PEDOT:PSS electrodes were deposited on the PVP layer by drop casting in a circular shapes with a diameter of around 1500 μm. Finally, the samples were subjected to heat treatment for 110°C for 1 h.

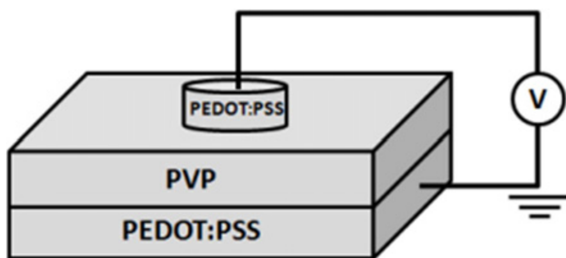

Fig. 1. Schematic diagram of the FORS device with the sandwiched structure of PEDOT:PSS/PVP/PEDOT:PSS.

3. RESULTS AND DISCUSSION

3.1 Physically layer characterization

Cross-sectional image of the fabricated device on the PI substrate was taken by using SEM system (JSM-6700F, JEOL Ltd, Japan) as shown in Fig. 2. In the field emission scanning electron microscope (FESEM) image, PEDOT:PSS (bottom electrode) is the first layer on the PI substrate. The second layer in the image is the PVP layer (active layer) on the PEDOT:PSS layer. The top layer is the PEDOT:PSS layer on the PVP layer serving as a top electrode in the FORS sandwich structure. The thickness of each of the three layers, i.e., PEDOT:PSS layer (bottom electrode), PVP layer (switching layer), and PEDOT:PSS (top electrode), is around 1 μm. There, the total thickness of the fabricated FORS is around 3 μm as shown in the inset of Fig. 2.

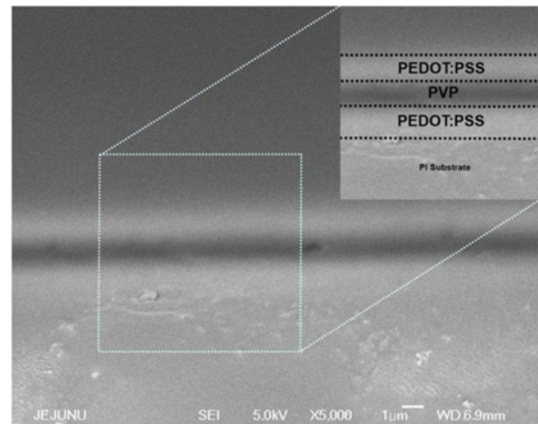

Fig. 2. Cross-sectional FESEM image of the FORS device with the sandwiched structure of PEDOT:PSS/PVP/PEDOT:PSS.

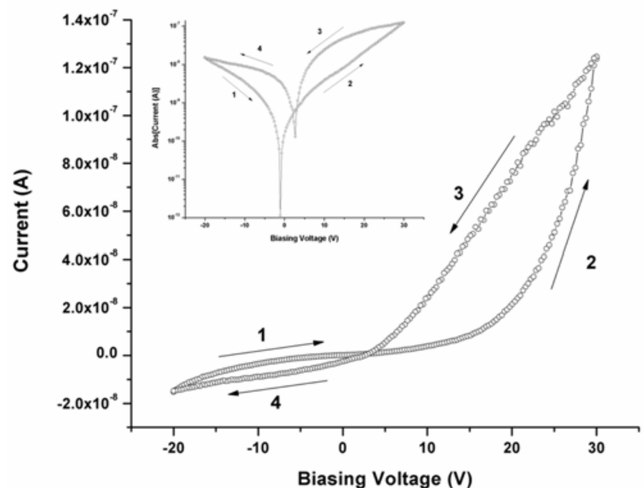

Fig. 3. *I-V* analysis of the PEDOT:PSS/PVP/PEDOT:PSS sandwiched device. The inset shows the semi-log graph PEDOT:PSS/PVP/PEDOT:PSS sandwiched device.

3.2 Resistive switching

Current-voltage (*I-V*) measurements of the fabricated device were performed by an Agilent B1500A semiconductor device analyzer. All of the electrical characterization was done by forcing the top electrode with the voltage source and grounding the bottom electrode. Figure 3 shows the *I-V* measurement of the FORS device. *I-V* curves were obtained by double sweeping the voltage from −20 to +30 V. In the forward direction of the voltage polarity, the device exhibited low conductivity state/high resistance state (HRS)/OFF state. At around +20 V, the device changed its OFF state into ON state/low resistance state (LRS)/high conductivity state. In the reverse direction of the voltage sweep, the device started in the ON state and switched back into OFF state at around −20 V. The exhibited *I-V* hysteresis with two distinct states can be exploited to use the fabricated FORS for bistable memory applications. It can be noticed that the device offers different memory window on both the positive side and negative side of the voltage polarity. This feature can be utilized to use the fabricated device in two different scenarios.

PEDOT:PSS contact is known as an efficient hole injection layer due to its work function (~ 5.1 eV)[27] where as it acts as a high barrier for the electron transport. So, the switching phenomenon in the fabricated FORS could be attributed to the hole injection by the top PEDOT:PSS electrode into the PVP layer and the trapping of mobile carriers (holes) within the PVP layer. As noticed, the top electrode was forced with negative as well as positive polarities, while the bottom electrode was grounded during all the measurements. During the application of negative polarity on top PEDOT:PSS electrode, only small amount of current was flown into the FORS device because PEDOT:PSS is not efficient electron transport material. While in the application of positive potential on top PEDOT:PSS electrode, significant current was flown due to the hole injection role of PEDOT:PSS contact as compared to that of negative potential. So, the discussed phenomenon bestowed different current intensity on both sides of the voltage polarity and produced asymmetric *I-V* characteristics in the fabricated FORS even though both the electrodes are of same material as evident in Fig. 3. The semi-log graph is shown in the inset of Fig. 3 that shows OFF/ON ratio around 10 : 1 which provides sufficient margin to distinguish between two states. It can also be noticed in *I-V* curve that there is off-set current for both voltage polarities. This is due to the charge trapping in the polymeric layer as noticed in literature.[15] In the fabricated FORS device, the carriers were injected through PEDOT:PSS top electrode and were trapped within the PVP layer due to the presence of trap sites in it, that produced off-set effect in the *I-V* curve. Due to the off-set effect, the current did not drop to zero at zero voltage as noticed in the inset of Fig. 3.

Effect of sweeping rate was checked in the *I-V* charac-

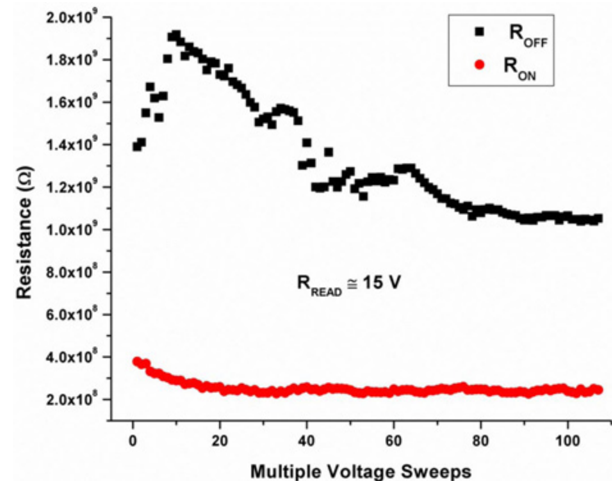

Fig. 4. The graph shows the endurance test for the PEDOT:PSS/PVP/PEDOT:PSS sandwiched device at a reading voltage (V_{READ}) of +15 V over 100 cycles.

teristics of the fabricated FORS. It was found that the sweeping rate has no noticeable effect on the *I-V* characteristics: neither on the switching voltage nor on the OFF/ON ratio. Sweeping rate was defined by the delay time during *I-V* measurements. The delay time was varied from 10 ms to 100 ms with the voltage step-size of 300 mV. A lower delay time resulted in higher sweeping rate and vice versa. The robustness of the device was tested against multiple voltage stresses, the device performed exceptionally well over 100 voltage sweeps as shown in Fig. 4. Initially, the resistance of the device in its HRS fluctuated but it settled down after 40 voltage sweeps. It can also be noticed that the LRS is more stable than the HRS throughout the endurance test as shown in Fig. 4. The fluctuating trend in the endurance test might be attributed to the inherited traps sites and defects created in the PVP film due to the printing process. The fluctuation in *I-V* curves settled down after 40 voltage sweeps. The average resistances in ON and OFF states of the device were calculated to be 3×10^8 Ω and 1.1×10^9 Ω respectively. The reading voltage (V_{READ}) used to find the OFF and ON state of the device was around +15 V.

The fabricated switch took a large voltage to elucidate resistive switching behavior because of low conductivity of the PEDOT:PSS electrode. The conductive materials having low work functions usually take large voltage for charge injections. This shortcoming could be downplayed by doping the PEDOT:PSS polymer or employing other techniques to enhance its conductivity.[20-22]

3.3 Current conduction mechanism

As noticed in *I-V* curve of the fabricated FORS device as shown in Fig. 3, the negative polarity on top electrode resulted in a minute current. As compared to that of negative potential, the positive potential on top electrode produced a

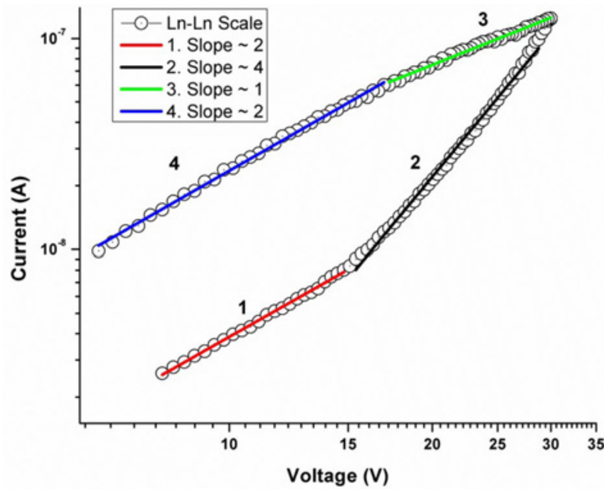

Fig. 5. Double logarithmic *I-V* graph of the PEDOT:PSS/PVP/PEDOT:PSS sandwiched device in a positive cycle of the sweeping voltage indicating different current conduction mechanisms in the forward and reverse direction of the voltage polarity.

sufficient high amount of current due to the efficient hole injection role of PEDOT:PSS top electrode. So, the current conduction mechanisms were analyzed only for the positive potential on top electrode.

The current conduction mechanisms in the fabricated FORS were analyzed based on slope calculation by straight line fitting in double logarithmic scale as depicted in Fig. 5, and were supported by the physical laws governing the current conduction mechanism. Four different current conduction mechanisms were suggested underlying bistable resistive switching in the fabricated FORS.

In the HRS of FORS device, the conduction mechanism of current is attributed to the space charge limited current (SCLC) conduction up to 15 V (region 1 in Fig. 5). As the holes were injected by the positive potential on top electrode and thereby the accumulation of carriers near the electrode resulted in a space charge buildup. Mutual repulsion among the injected charges limited the further injection of charge carriers into the sample, the resulting current is known as SCLC. Carrier injection electrode (PEDOT:PSS top electrode) is one of the main reasons that arises the SCLC. The injected current in the fabricated sample decreased by several orders due to the presence of traps in the polymer layer (PVP sandwiched layer). The observed phenomenon is quite in line with the reported literature.[14] The SCLC trap limited regime is controlled by the traps in the PVP layer via thermally activated hopping conduction as reported in literature.[15,28-30] In this regime, the current density is obeyed by the Mott-Gurney law as described below in Eq. (1):

$$J = \frac{9\varepsilon\varepsilon_0\mu\Theta V^2}{d^3} \tag{1}$$

where ε is the dielectric constant of the switching polymer, ε_0 is the permittivity of the free space, μ is the hole carrier mobility, Θ is the trapping fraction, V is the applied potential, and d is the thickness of the switching polymeric layer.

Once sufficient amount of traps were filled by the mobile carriers, eventually carrier were trapped within the switching PVP polymeric layer. Then, the current in the switching layer was injected due to the trap-charge limited current (TCLC) conduction. Above 15 V (region 2 in Fig. 5) in the HRS of the FORS, TCLC conduction mechanism was found to be the governing conduction mechanism for charge injection into the polymeric layer. In the TCLC conduction, the current increased exponentially and the onset of the trap-filled voltage resulted in the density of traps as observed in literature.[31,32] Assuming the trapped hole carrier density >> free hole carrier density, the *J-V* characteristic is given by the following governing Eq. (2):

$$J = q^{1-l}\mu N_v\left(\frac{2l+1}{l+1}\right)^{l+1}\left(\frac{l}{l+1}\frac{\varepsilon\varepsilon_0}{H_b}\right)^l\frac{V^{l+1}}{d^{2l+1}} \tag{2}$$

where J is the current density, V is the applied potential, q is the elementary charge, d is the thickness of the material film, μ is the hole carrier mobility, N_v is the effective density of states, ε is the dielectric constant of the material, ε_0 is the permittivity of the free space, H_b is the density of traps at the edge of valance band, and l determines the distribution of traps in the band gap.

In some of the reported literature, an abrupt jump of current by several orders of magnitude was reported after SCLC trap limited regime in the *I-V* curves which is not considered as normal behavior in SCLC conduction.[15,33,34] In contrast to the reported literature, an exponential increase in current was observed after SCLC trap limited regime in the fabricated FORS device that is termed as TCLC conduction.

In the reverse direction of the voltage polarity, the fabricated FORS was operated in the LRS and it was found that the conduction mechanism was dominated by the ohmic conduction (region 3 in Fig. 5) because of the thermal excited mobile carriers hopping from one isolated state to the next as reported in literature.[15,28-30] In this region, the current density J can be described by the following governing Eq. (3):

$$J = \frac{qn_0\mu V}{d} \tag{3}$$

where q is the elementary charge of the carrier, n_0 is the density of free carriers, μ is the carrier mobility, V is the applied voltage, and d is the thickness of the polymeric layer.

In the LRS of the FORS, below 20 V (region 4 in Fig. 5), the fabricated device followed exceptionally well the proportional regime of I to V^2. So, the fabricated FORS device followed trap free SCLC conduction because of the filling of

traps through mobile carriers. Trap free SCLC conduction mechanism is usually common after TCLC conduction as reported in literature.[15,28-30] So, the current was injected in the switching layer of PVP during the LRS of FORS due to the trap free SCLC conduction mechanism.

Based upon the above analysis, the fabricated FORS exhibited reversible resistive switching in the forward direction of voltage polarity in the HRS of device due to the transition from trap-limited SCLC to TCLC conduction mechanism, and then in the reverse direction of voltage polarity during the LRS of device from ohmic current conduction to the trap-free SCLC conduction mechanism. So overall, the fabricated FORS exhibited the reversible resistive switching effects due to the transition from the trap-limited SCLC (during HRS) to the trap-free SCLC (during LRS). The non-ideal measuring conditions and more than one current conduction mechanisms involved for charge injection into the PVP polymeric layer ultimately led to the existence of some non-linearities in the perfect line fitting of both the HRS and LRS of the fabricated FORS.

4. CONCLUSIONS

Bistable resistive switching effects were demonstrated in the FORS with the sandwich structure of PEDOT:PSS/PVP/PEDOT:PSS. Robustness of the fabricated device was scrutinized over 100 voltage sweeps. Four different current conduction mechanisms were found and analyzed through slope calculation. Overall the fabricated resistive device exhibited bistable resistive switching in the transition of trap-limited space charge limit current conduction during the OFF-state of the device to the trap-free space charge current conduction during its ON-state.

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