Electronic Materials Letters, Vol. 8, No. 2 (2012), pp. 169-174
DOI: 10.1007/s13391-012-2031-0

Numerical Study on Passive Crossbar Arrays Employing Threshold Switches as Cell-Selection-Devices

Doo Seok Jeong,* Hyung-Woo Ahn, Su-Dong Kim, Myunggi An, Suyoun Lee, and Byung-ki Cheong

Electronic Materials Research Center, Korea Institute of Science and Technology, Seoul 136-791, Korea

(received date: 5 January 2012 / accepted date: 21 February 2012 / published date: April 2012)

A read-out voltage margin of crossbar-array-based passive non-volatile memory employing one threshold switch and one memory switch (resistor) (1TS1R) unit structure was numerically evaluated for the worst-case pattern with respect to the row and column number of a crossbar array. The threshold switching behavior of amorphous GeSe, which has been recently reported by Jeong *et al*., was taken for the evaluation of the 1TS1R crossbar array. The calculation results identified that a pull-up voltage is of importance because of the highly non-linear current-voltage behavior of amorphous GeSe in the high resistance state.

Keywords: thresholds switching, crossbar arrays, chalcogenides, memory switching

1. INTRODUCTION

One of the most important concerns for memory devices is how to achieve the “readable” binary values “1” and “0” in a single bit element while meeting the integrated circuit’s mottos: *small, cheap, fast, and reliable*. Dynanic random access memory (DRAM) has been meeting all the important requirements since the beginning of its development. However, the design rule for DRAM is becoming very severe, e.g., the lateral feature size is expected to shrink down to 21 nm in 2016.[1] Due to the inherent scaling down problem of capacitance-based memory devices including DRAM, meeting this requirement appears to be very hard. Furthermore, the volatile nature of data in DRAM consumes enormous energy and energy consumption is expected to increase at a very high rate. Therefore, replacing the current DRAM technology with a non-volatile memory having small cell size, high speed, and reliability is regarded as a viable solution to these problems. There have been many suggested future nonvolatile memories *viz.* ferroelectric RAM (FRAM), magnetic RAM (MRAM), resistive RAM (RRAM), and phase-change RAM (PRAM), which can achieve the two binary values by the inherent physical behavior of each material. Among them, RRAM and PRAM are the most promising candidates due to their structural simplicity and easier down scaling owing to the working principle of resistance-based RAMs. So far, an enormous number of materials, e.g., binary transition metal oxides (TMOs) such as TiO_2,[2-4] NiO,[5] CuO,[6] complex oxides such as $Pb(Zr_x,Ti_{1-x})O_3$,[7] $(Pr,Co)MnO_3$,[8] and several chalcogenides such as $Ge_xSb_yTe_z$,[9] In_2Te_3,[10] As_2Te_3,[11] CuS,[12] have been found to be resistive switching materials.

The basic unit of RRAM is one transistor and one resistor (1T1R) that can be fabricated on a $6F^2$ or $8F^2$ scheme, where F means the minimum feature size. Besides this 1T1R unit cell, a crossbar-array-based passive element architecture is regarded as a means to increase integration density, satisfying a design rule of $4F^2$. Furthermore, passive crossbar arrays are stackable so that when n layers are stacked a design rule of $4F^2/n$ can be achieved. In this crossbar array scheme cell-selection-devices are inevitably necessary to prevent misreading the binary value written in each cell. When one cell in the high resistance state (HRS) is embedded in cells in a low resistance state (LRS), the so-called worst case pattern, the information stored in the cell is barely readable due to the so-called sneak current flowing through other LRS cells surrounding the HRS cell.[13] Moreover, to cut off the power consumption of the crossbar array, it is necessary to place a selection device in series with a memory switch (MS).

So far, some possible selection devices, e.g., p-n diode, asymmetric metal-insulator-metal (MIM) diodes, and Zener or breakdown diodes, have been suggested.[3,14] P-n and asymmetric MIM diodes are based on their asymmetric current-voltage (*I-V*) behavior, and thus this asymmetric *I-V* behavior allows current of one polarity to flow through the diodes. As is well known, there are two types of MSs, i.e., unipolar and bipolar. Diodes are suitable for crossbar arrays based on uipolar switches. For bipolar MS-based crossbar

*Corresponding author: dsjeong@kist.re.kr
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arrays Zener or breakdown diodes among the aforementioned candidates are available because both polarities of an applied voltage are necessary for reversible switching between the LRS and HRS. Therefore, it turns out that the choice of selection devices is limited depending upon the type of MSs.

Threshold switching phenomena in amorphous chalcogenides are expected to be applied to cell-selection devices due to their volatile resistive switching characteristics. Threshold switching is known to occur without being dependent on the polarity of the applied voltage, and thus it is available for both unipolar- and bipolar-type MSs. Moreover, the read-out process for a MS together with a threshold switch (TS) is non-destructive so that no additional voltage application is necessary for the recovery. In fact, Kau *et al.* have demonstrated the possible application of TSs to cell-selection devices.[15] As-Te-Ge-Si-based amorphous chalcogenide materials are well known to exhibit threshold switching behavior.[16] A recent publication by Jeong *et al.* has reported threshold switching behavior in amorphous GeSe with inert top- and bottom-electrode (Pt), which is very fast (< 40 nsec.) and highly resistive in the off-state.

There have been several publications on the read-out voltage margin calculation (for the worst-case pattern) of passive crossbar arrays utilizing different unit structures, e.g. 1R,[13] complementary resistive switches (CRS),[17] a highly resistive resistor and one memory switch (1S1R),[18] and one diode and one memory switch (1D1R).[19] However, to our best knowledge no crossbar arrays employing cell-selection devices of highly non-linear *I-V* behavior have been theoretically dealt with. In this paper, we introduce a method for the calculation of read-out voltage margins of 1TS1R-based crossbar arrays, where TSs exhibit non-linear *I-V* characteristics. We employ a Pt/GeSe/Pt system as an example of a TS in the 1TS1R-based crossbar array. (see Ref. [20]).

2. EXPERIMENTAL

2.1 Modeling of non-linear *I-V* behavior in a Pt/GeSe/Pt TS

A typical current density vs. voltage (J-V) curve of a Pt/GeSe/Pt TS in the sub-threshold regime (off-state) is plotted in Fig. 1 (grey filled squares). This measurement was done by applying a staircase voltage sweep with a delay time of 1 msec. The thicknesses of the GeSe and Pt films were 100 nm and 50 nm, respectively. The detail of the sample fabrication procedures has been reported elsewhere.[21] According to the voltage- and temperature-domain analysis shown in Ref. [21], the J-V behavior can be nicely fitted using an empirical form of $J = J_0 V e^{-(E_A - \alpha V)/k_B T}$. J_0, E_A, α, k_B, and T denote a coefficient, an activation energy, a voltage coefficient, the Boltzmann coefficient, and temperature, respectively. By applying voltage pulses in the sub-threshold voltage range

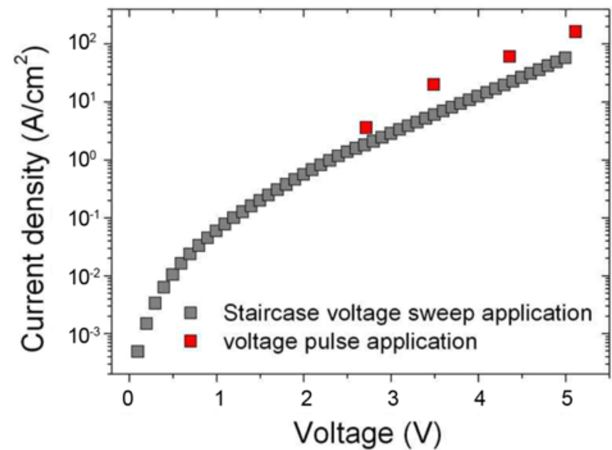

Fig. 1. J-V behavior of a Pt/GeSe/Pt threshold switch up to 5 V, which was measured by applying a staircase voltage sweep with a delay time of 1 msec. (static measurement). The red filled squares were obtained by applying a voltage pulse of 200 nsec. pulse width.

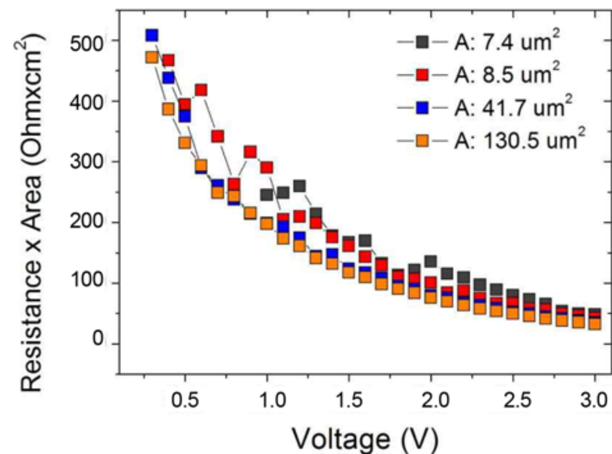

Fig. 2. R × A behavior with respect to the applied voltage to Pt/GeSe/Pt TSs of different pad-sizes. This plot exhibits non-linear *I-V* behavior of the TSs.

we obtained current values responding to voltage pulses, and thus resistance values. The comparison of the pulse-responding currents and those measured using a static staircase voltage sweep is shown in Fig. 1. As shown in Fig. 1, no serious time-dependent resistance-change takes place in the system, although there are small deviations.

It was identified that the average resistance of the TS scales with the pad-size as resistance multiplied by pad-size (R × A) for different pad-sizes almost falls into a single curve as depicted in Fig. 2. This implies that current transport through the TS is homogeneous over the pad-area. The resistance vs. voltage behavior of the TS in the sub-μm^2 pad-size regime can therefore be estimated. Then, the average off-state resistance of the TS is $R_{off}^{TS} = VA^{-1}J_0^{-1}e^{(E_A - \alpha V)/k_B T}$, where A denotes the pad-size.

The *I-V* behavior of an on-state TS shows weak "assigned" voltage dependence. Because in the on-state the applied voltage is divided by the load resistor and on-state TS and the on-state resistance is comparable to the load resistor, a voltage assigned to the TS is remarkably different from the applied one. At this moment, the degree of non-linearity of the *I-V* behavior in the on-state cannot therefore be estimated in a wide voltage range.

The pad-size dependence of the on-state resistance is mysterious. Unlike the off-state resistance, the on-state resistance does not scale well with the pad-size,[20] and thus the on-resistance in the sub-μm^2 pad-size regime is not easily predictable. Nevertheless, the non-linearity and non-scaling on-state resistance are unlikely of great importance for evaluating a read-out voltage margin for the worst-case pattern, which is determined by the sneak current in the 1TS1R-based crossbar array.

2.2 Calculation of a read-out voltage margin for the worst-case pattern

A read-out voltage margin for the worst-case pattern is of great importance because the pattern allows the most sneak current through unselected cells around the selected one. The worst-case pattern arises from a selected cell, whose MS is in the high resistance state (HRS), and all the neighboring cells, whose MSs are in the low resistance state (LRS). In this case, the read-out voltage margin is most likely attributed to the sneak current rather than the current through the selected cell. We evaluated a read-out voltage margin of a crossbar array (1TS1R) for the worst-case pattern for different parameters, e.g. wordline and bitline numbers, and pull-up voltages. This calculation was done for the all-bitline-pull-up scheme as explained by Flocke and Noll.[13] For simplicity, the line resistance was not taken into consideration.

If the TSs are implemented within a passive crossbar array, the read-out voltage margin can be significantly improved. In this crossbar array, a TS is in serial connection with a MS. The resistance of each cell can therefore be described as the summation of the resistances of the MS (R^M), $R^M \in \{R^M_H, R^M_L\}$, and the TS (R^{TS}), $R^{TS} \in \{R^{TS}_{off}, R^{TS}_{on}\}$. $R^M_H(R^{TS}_{off})$ and $R^M_L(R^{TS}_{on})$, meaning the resistances of the MS (TS) in the HRS (off-state) and the LRS (on-state), respectively.

By regarding the J-V behavior of the Pt/GeSe/Pt TS, which is shown in Fig. 1, the read-out voltage margin ΔV for the worst-case pattern was evaluated in an $M \times N$ crossbar array where M was set to be equal to N. That is, one selected MS in the array is in the HRS and the rest of the MN-1 MSs are in the LRS. In this case, due to sneak current the read voltage margin falls below the minimum value for the successful read-out so that misreading the binary value stored in the HRS MS inevitably occurs. In the all-bitline-pull-up scheme for the worst-case pattern the selected HRS cell has a resistance of $R^M_H + R^{TS}_{on}$, the LRS cells of the selected wordline $R^M_L + R^{TS}_{on}$, and the unselected cells $R^M_L + R^{TS}_{off}$. As a matter of fact, a similar calculation has been done and the details have been reported elsewhere.[13,17] However, due to the nonlinear J-V behavior of the Pt/GeSe/Pt TS in the sub-threshold regime, the resistance cannot be regarded as a constant as assumed in the previous calculations. Indeed, the non-linearity makes defining a particular off-resistance value of the TS, i.e., R^{TS}_{off}, impossible.

The equivalent circuit of a crossbar array for the worst-case pattern in the all-bitline-pull-up scheme is illustrated in Fig. 3(a). Because of the non-linear J-V characteristics of the TS it is impossible to analytically evaluate voltage distribution at each node of the array under a certain pull-up voltage (V_{pu}). R_1 and R_2 in Fig. 3(a) depend upon the voltage difference between V_1 and V_2 and between V_2 and V_3, respectively. As both R_1 and R_2 are expected to be given by a function of $R_n = R^M_{on} + |V_{n+1} - V_n| A^{-1} J_0^{-1} e^{[E_A - \alpha |V_{n+1} - V_n|]/k_B T}$, where $n = 1$, 2, we can use this formula for the voltage evaluation. Voltages at three different nodes (V_1, V_2, and V_3) can be calculated using the Kirchhoff's circuit law (KCL), i.e., the summation of currents flowing into and out of each

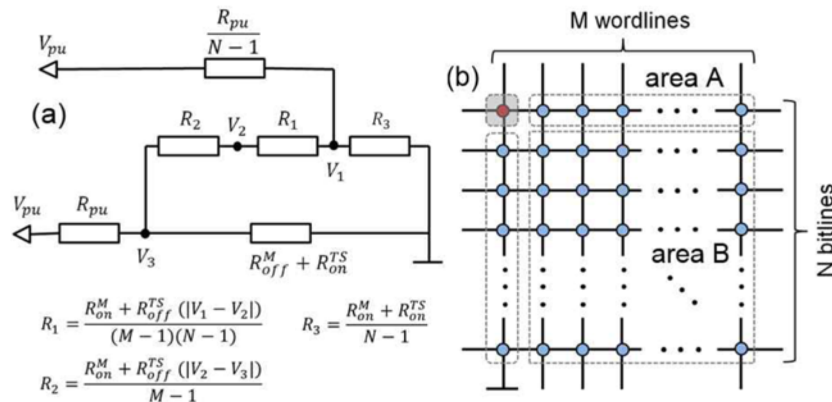

Fig. 3. (a) Equivalent circuit of a read scheme of the all-bitline-pull-up case. (b) A schematic of a crossbar array of the worst case pattern. The top/left cell is selected to read, whose MS is in the HRS, and the rest MN-1 cells' MSs in the LRS. R_1(R_2) is of the summation of all the cells in parallel in area A(B). (V_1 and V_2) and (V_2 and V_3) are the voltages at the two terminals of the equivalent resistor R_1 and R_2, respectively.

node is zero, if R_1 and R_2 are defined. R_1 and R_2 rely upon the voltage drops along them and vice versa. Therefore, one should solve self-consistent equations for the evaluation of V_1, V_2, and V_3. These equations can be solved using an iterative method. The voltage difference $|V_1-V_2|$ approximately corresponds to the voltage drop along R_1, the lumped cell resistors in area B depicted in Fig. 3(b), and the voltage difference $|V_2-V_3|$ the voltage drop along R_2, lumped cell resistors in area A. V_3 is a read voltage for the selected cell.

Using the KCL at the three nodes in Fig. 3(b), the following three equations can be derived.

$$\left\{(N-1)(R_{pu}^{-1}+R_3^{-1})+\frac{(M-1)(N-1)}{R_1(|V_1-V_2|)+(N-1)R_2(|V_2-V_3|)}\right\}V_1 -\frac{(M-1)(N-1)}{R_1(|V_1-V_2|)+(N-1)R_2(|V_2-V_3|)}V_2=(N-1)R_{pu}^{-1}V_{pu} \quad (1)$$

$$\frac{(M-1)(N-1)}{R_1(|V_1-V_2|)+(N-1)R_2(|V_2-V_3|)}V_1 -\left\{\frac{(M-1)(N-1)}{R_1(|V_1-V_2|)+(N-1)R_2(|V_2-V_3|)}+R_{pu}^{-1}+(R_{off}^{M}+R_{on}^{TS})^{-1}\right\}V_2 -R_{pu}^{-1}V_{pu} \quad (2)$$

and

$$(N-1)R_2(|V_2-V_3|)V_1+R_1(|V_1-V_2|)V_2 -\{R_1(|V_1-V_2|)+(N-1)R_2(|V_2-V_3|)\}V_3=0 \quad (3)$$

These simultaneous equations were numerically solved using the Newton-Raphson method as an iterative method.[22] The HRS-to-LRS ratio of each memory element in the crossbar array was set 10^3 and the HRS resistance 10^3 ohms.

3. RESULTS AND DISCUSSION

A read-out voltage margin (ΔV) normalized to a pull-up voltage (V_{pu}) for various pull-up voltages of the crossbar array is plotted with regard to the number of bitlines (wordlines) [see Fig. 4(a)]. For this calculation a J-V curve of the TS was taken from Fig. 1. This calculation was done for a line width of 20 nm.

The voltage margin (ΔV) remarkably decreases with the number of wordlines above a certain number as previously reported by Flocke and Noll,[13] and Linn *et al*.[17] Of course, by increasing the HRS-to-LRS ratio of the MS one can retard the decrease in the voltage margin, however, the contribution has been found to be trivial.[13,17] Implementing the TS in the crossbar array greatly retards the voltage margin decrease as shown in Fig. 4(a). Owing to the non-linear J-V behavior, the read-out voltage margin is affected by a pull-up

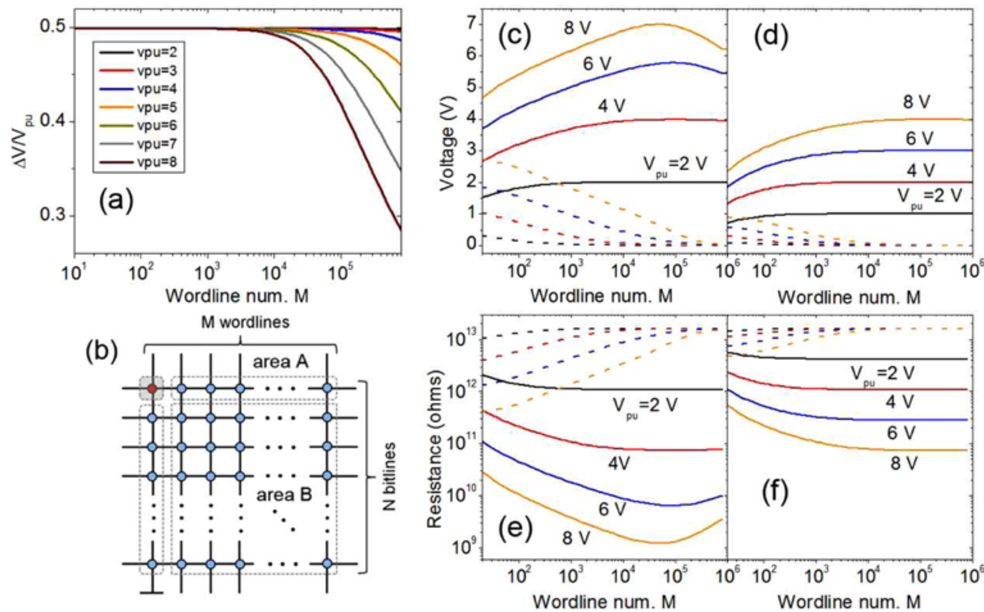

Fig. 4. (a) Read-out voltage margin normalized to a pull-up voltage for various pull-up voltages with respect to the number of wordlines (bitlines) in a crossbar array. The on- and off-state resistances of the MS was assumed to be 10^3 and 10^6 ohms, respectively. And the on-state resistance of the TS was set 10^3 ohms. (b) A schematic of the crossbar array of the worst case pattern. The selected top/left cell is in the HRS and the rest cells in the LRS. Area A and B include the cells between the read bitline and floated wordlines and those between the unread bitlines and floated wordlines. For the worst-case pattern with the off-state TS of the selected cell, voltages applied across the two terminals of R_1 of area B (dashed line) and R_2 of area A (solid line) for various pull-up voltages are plotted in (c). Data corresponding to the worst-case pattern with the on-state TS of the selected cell are plotted in (d). The lumped resistance of the cells in area A (solid line) and B (dashed line), which corresponds to the voltage drop shown in (c) and (d), is plotted in (e) and (f), respectively.

voltage unlike other model systems utilizing selection devices of a constant off-resistance, i.e. linear J-V behavior.

As noticed in Fig. 4(a), lower pull-up voltages are favorable for larger bitline (wordline) numbers. This aspect arises from the non-linearity exhibiting lower resistances with higher voltages as can be seen in Fig. 2. Therefore, the resistance of the unselected cells becomes higher with the lowering of the pull-up voltage, which consequently leads to a higher read-out voltage margin. This gives rise to a restriction on the choice of the TS implemented within the array in terms of the threshold voltage of the TS, which should be as low as possible to maintain the voltage margin.

A voltage drop through R_2 of area A designated in Fig. 4(b) relies upon the resistance state of the selected cell, either $R_H^M + R_{on}^{TS}$ or $R_L^M + R_{on}^{TS}$. Fig. 4(c) shows a voltage (solid line) applied through R_2 (area A) and a voltage (dashed line) through R_1 (area B) with respect to the number of bitlines for the worst-case pattern with the off-state TS of the selected cell. When the TS is switched on, i.e. on-state, the voltages are assigned to R_1 and R_2, which are plotted in Fig. 4(d). The lumped resistances of area A and B, which correspond to the voltage drop shown in Figs. 4(c) and (d), are plotted in Figs. 4(d) and (e), respectively.

The calculation results note that the voltage drop along the lumped cells in area A. which are sandwiched between the read bitline and floated wordlines (unselected) is comparable to the pull-up voltage so that the TSs of the cells in area A can be accidently switched on. In Fig. 4(c), it can be noticed that the difference between voltages assigned to the selected cell and unselected cells increases with the pull-up voltage. This implies that higher pull-up voltages are favorable to the optional operation of the selected cell. Therefore, the aforementioned preference of lower pull-up voltages for higher read-out voltage margins, as depicted in Fig. 4(a), is restricted within the range of a pull-up voltage that guarantees the optional operation. Therefore, a pull-up voltage should be carefully chosen so as not to switch on the threshold switches in area A, considering the possible distribution of the TS voltage. As shown in Fig. 4(d), a voltage assigned to the cells in area A is approximately half a pull-up voltage, and thus the off-state resistance of a TS exhibiting non-linear J-V behavior needs to be assessed at $V_{pu}/2$.

4. CONCLUSIONS

We introduced a numerical method to evaluate voltage distribution in a passive crossbar array utilizing 1TS1R unit cells with particular emphasis on the worst-case pattern in the all-bitline-pull-up scheme. This calculation method can be differentiated from previously introduced ones in the sense that selection devices having non-linear J-V behavior, e.g. diode and TS, can be taken into account in the calculation. As a calculation result, we found several restrictions of TS property for the reliable read-out operation of the worst-case pattern, for example, that optimized pull-up voltages should be neither high enough to decrease the read-out voltage margin nor low enough to degrade the selectivity.

ACKNOWLEDGEMENTS

This research was supported by a grant from the Fundamental R&D Program for Core Technology of Materials (grant no. 2M29150) funded by the Ministry of Knowledge Economy, Republic of Korea.

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