Arabian Journal for Science and Engineering (2022) 47:14983–14988
https://doi.org/10.1007/s13369-022-07338-8

RESEARCH ARTICLE-ELECTRICAL ENGINEERING

A Novel Tunable Grounded Positive and Negative Active Inductor Simulator and Impedance Multiplier

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Received: 29 September 2021 / Accepted: 16 December 2021 / Published online: 9 October 2022

Abstract
His paper presents a new tunable positive and negative active inductor simulator and positive and negative capacitance and resistance multiplier. The proposed designs use only one second-generation voltage-mode conveyor (VCII+), one OTA and two passive elements. Applications to the proposed designs in the design of different types of filters are also presented. The functionality of the designs is confirmed using simulation and experimentally.

Keywords Active inductor · Tunable impedance multiplier · Integrated circuits · Negative impedance · Filters · Compensation

1 Introduction

Active inductors simulator and impedance scaling circuits play essential role in many applications. This include but not limited to active filters, oscillators, phase shifters, etc. [1–3]. Simulated inductors offers some advantages such as integration, low area, and high quality factor. There are many designs available in the literature. The recent design in [1] used a single second-generation voltage-mode conveyor and three passive components. The drawback of this design is that it requires two identical resistors to obtain a lossless active inductor and not suitable for very low frequency applications. The design in [2] is complex because it uses three CFOA and four passive elements. In [3], a CFOA based design is used with three passive elements and the capacitor is floating which is not preferable. The drawback of this design is that it is lossy inductor.Other applications, required impedance multiplier to scale up a capacitance or resistance for very low frequency applications such as filters for biomedical systems where large capacitance or resistance are needed [4]. There are many designs in the open literature. The design in [5] used three OTAs to design a capacitance multiplier. In [6], a MOSFET-based impedance multiplier is presented. The drawback of this design is that it is not tunable. A three current-controlled current amplifier approach is presented in [7]. The design is limited to capacitance and resistance multiplier. The design in [8] used current mirror aspect ratio for capacitance multiplier and hence no tunability. A universal immittance simulator is presented in [9] where three CCIIs are used with three to four passive elements. A current-Conveyor based approach for R and C multiplier only is presented in [10]. The design in [11] uses three OTAs and two equal values capacitors to implement capacitance multiplier only. In [12], a differential amplifier-based capacitance multiplier only is presented. The design in [13] is a capacitance multiplier only. References [14, 15] present current mirror-based capacitance multipliers in which the tunability is not possible. The design in [16] used CCII and OTA to implement capacitor and resistor multiplier only. In [17], a grounded inductor simulator is presented. The design used two CFOA and four passive elements. The design in [18] used VCII to implement capacitance multiplier only and it uses floating capacitor. In [19], one INIC and one IVIC and three passive elements were used to simulate grounded active inductor. The design in [20], used two inverting buffers and one CCII and three passive element one of them is a floating capacitor to simulate grounded inductor. A modified MD VCC and three passive element were used to implement a lossy active inductor is presented in [21].

This paper presents a novel, tunable positive and negative active inductor simulator and positive and negative capacitance and resistance multiplier. The rest of the paper is

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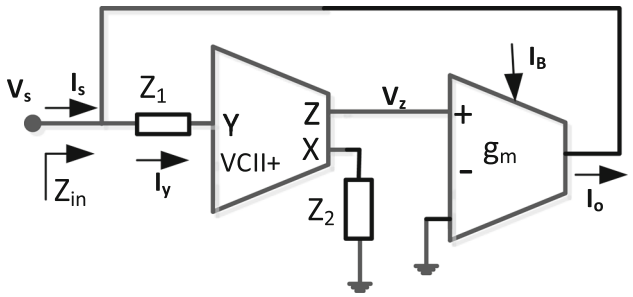

Fig. 1 Circuit diagram of the proposed design

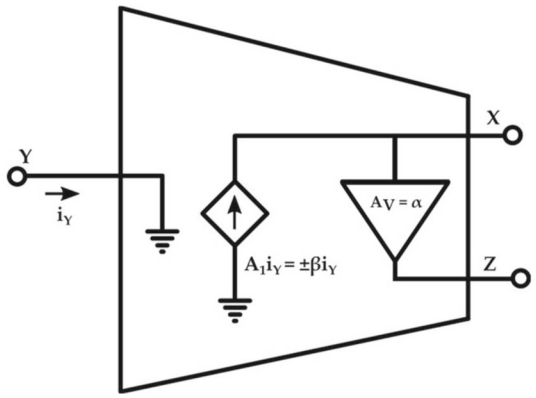

Fig. 2 Voltage-mode conveyor

organized as a follows: The proposed design is presented in Sect. 2. Simulation and experimental results are presented in Sect. 3. The paper conclusion is presented in Sect. 4.

2 Proposed Design

The proposed design is shown in Fig. 1. It consists of a second-generation voltage-mode conveyor (VCII+), operational transconductance amplifier (OTA) and only two passive components.

The relationship between voltage and currents terminals of VCII are represented as:

$$i_x = \pm\beta i_y,\ V_z = \alpha V_x,\ V_y = 0 \tag{1}$$

where β and α are current gain.

The terminal characteristic of the VCII are: high impedance at X node and low impedance at Y and Z nodes (Fig. 2).

with reference to Fig. 1, the input impedance is given by:

$$Z_{\text{in}} = \frac{V_s}{I_s} = \frac{V_s}{I_y - I_o} \tag{2}$$

$$i_0 = V_Z \times g_m = i_x Z_2 g_m = -i_y Z_2 g_m \tag{3}$$

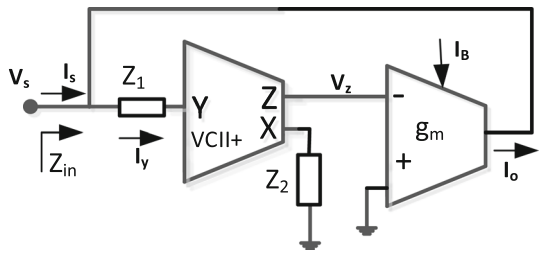

Fig. 3 Circuit diagram negative impedance simulator and resistance multiplier

But, $i_y = V_s/Z_1$, then the input impedance is written as:

$$Z_{in} = \frac{Z_1}{1 + Z_2 g_m} \tag{4}$$

where, $g_m = 20 \times I_{\text{B}}$ is the OTA transconductance and I_{B} is the OTA bias current.

From Eq. (4), the circuit can be used to implement a tunable grounded active inductor and capacitance multiplier as follows:

1. *Active inductor simulator*

If $Z_1 = R_1$, and $Z_2 = \frac{1}{sC_2}$, the input impedance is given by:

$$Z_{\text{in}} = sC_2 \frac{R_1}{20 \times I_{\text{B}}} = sL \tag{5}$$

where $L = C_2 \frac{R_1}{20 \times I_{\text{B}}}$ Eq. (5) implements a tunable inductor and the value of the inductance is controlled using R_1 and I_{B}.

2. *Capacitance multiplier*

If $Z_1 = \frac{1}{sC_1}$ and $Z_2 = R_2$, then the input impedance is given by:

$$Z_{\text{in}} = \frac{1}{sC_1(1 + 20 \times R_2 I_{\text{B}})} \tag{6}$$

The original capacitance is multiplied by $(1 + 20 \times R_2 I_{\text{B}})$ and can be tuned using R_2 and I_{B}. The modified circuit in Fig. 1 is shown in Fig. 3 and used to implement a tunable positive and negative resistance multiplier, negative active inductor simulator and negative capacitance multiplier as follows:

With reference to Fig. 3, the input impedance Z_{in} is given by:

$$Z_{\text{in}} = \frac{Z_1}{1 - Z_2 g_m} \tag{7}$$

3. Resistance multiplier

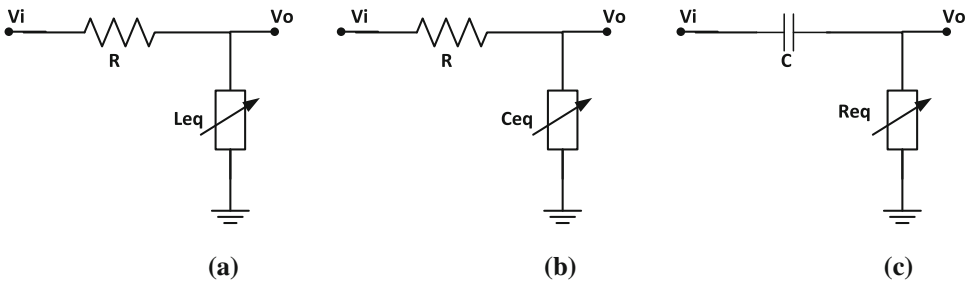

Fig. 4 Circuits used to confirm the functionality of the proposed design

From (7), if $Z_2 g_m < 1$, then Z_1 will be scaled up.

If $Z_1 = R_1$ (the resistance to be scaled up), $Z_2 = R_2$, then the input impedance is given by:

$$Z_{\text{in}} = \frac{R_1}{(1 - 20 \times R_2 I_{\text{B}})} \tag{8}$$

And $0 \leq 20 \times R_2 I_{\text{B}} < 1$.

4. Negative resistance

From Eq. 7, if $Z_2 g_m > 1$, then a negative tunable resistance multiplier is obtained:

If $Z_1 = R_1$ (the resistance to be scaled up), $Z_2 = R_2$, then the input impedance is given by:

$$Z_{\text{in}} = \frac{R_1}{(-20 \times R_2 I_{\text{B}})} \tag{9}$$

5. Negative active inductor simulator

If $Z_1 = R_1$ and, $Z_2 = \frac{1}{sC_2}$, $Z_2 g_m > 1$, then a negative active inductor is obtained and is given by:

$$Z_{\text{in}} = -sC_2 \frac{R_1}{20 \times I_{\text{B}}} \tag{10}$$

6. Negative capacitance multiplier

If $Z_1 = \frac{1}{sC_1}$, and $Z_2 = R_2$, $Z_2 g_m > 1$, then the input impedance is given by:

$$Z_{\text{in}} = -\frac{1}{sC_1(20 \times R_2 I_{\text{B}})} \tag{11}$$

3 Simulation and Experimental Results

3.1 Simulation Results

To confirm the functionality of the proposed designs, the active inductor and the capacitor multiplier are used in the design of high pass, low pass filters, respectively. The resistance multiplier is used in the design of high pass filter as shown in Fig. 4. Multisim professional is used where AD844 is configured as VCII + and LM13700 (OTA). The circuit is powered with $V_{\text{CC}} = -V_{\text{SS}} = 5$ V.

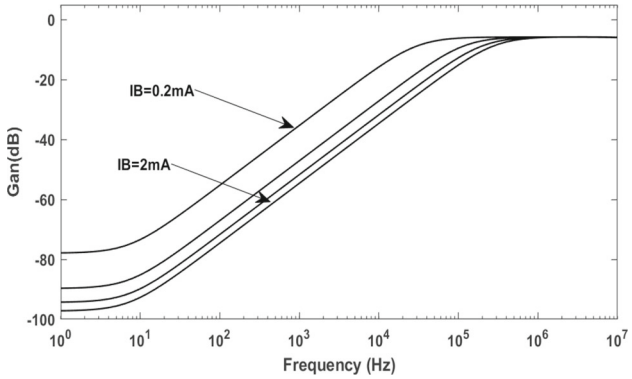

Fig. 5 Frequency response for the high pass filter using the active inductor

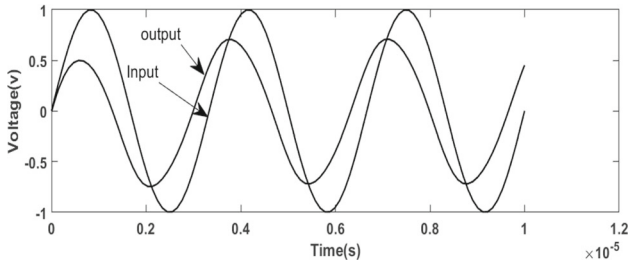

Fig. 6 Transient response of the high pass filter using the active inductor

a. *Active inductor*

For the active inductor, the high pass filter circuits shown in Fig. 4a is simulated with $R = 1$ kΩ and the active impedance parameters are $R_1 = 10$ kΩ, $C_2 = 1$ nF. The OTA bias current was varied from 0.2 to 2 mA. The inductance will vary from 0.5mH to 5 m. Plots of the frequency response of the filter are shown in Fig. 5. It is evident from the plot that the active inductor is functioning properly.

The transient analysis was carried out using 300 kHz input signal with 1 V amplitude and a bias current of 1 mA. The simulation results shown in Fig. 6 confirm that the active inductor is working properly.

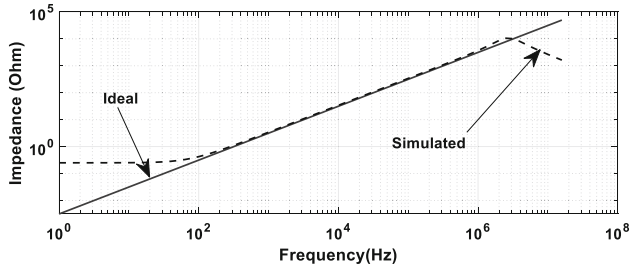

Fig. 7 Active inductor frequency range

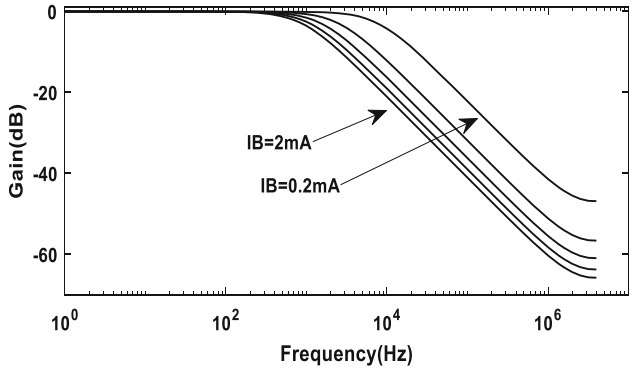

Fig. 8 The frequency response of the low pass filter using the proposed capacitance multiplier

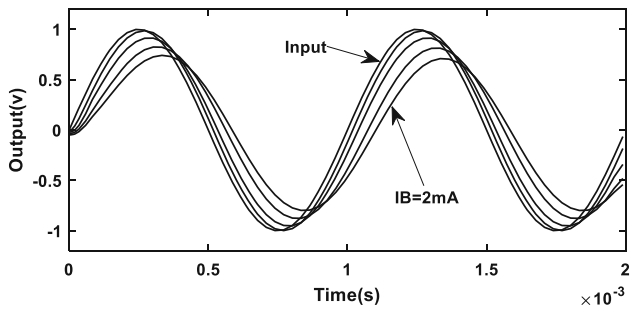

Fig. 9 Transient response for the low pass filter using the proposed capacitance multiplier

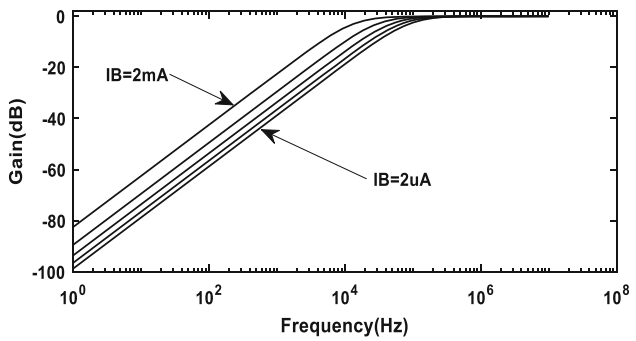

Fig. 10 Frequency response for high pass filter using resistance multiplier

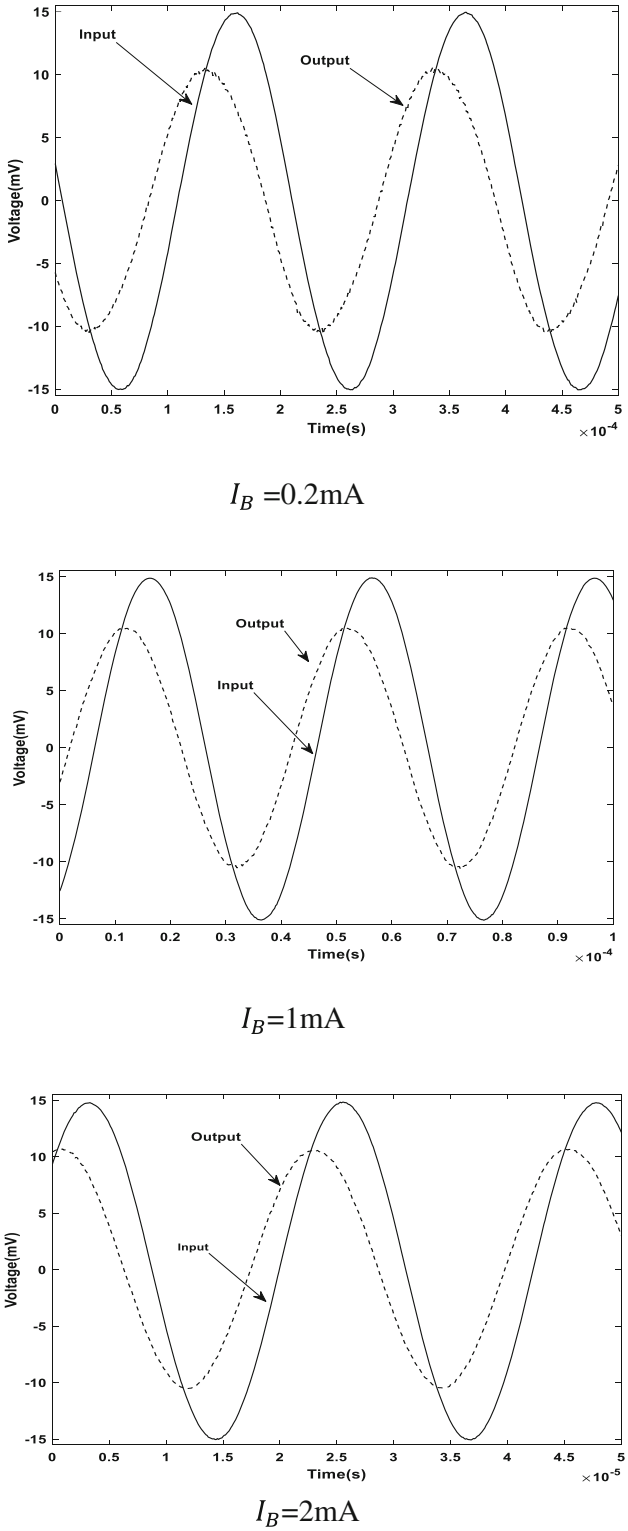

Fig. 11 Experimental results for the high pass filter transient response for different bias current

The active inductor will work properly in the range of 100 Hz to 1 MHz as shown in Fig. 7. The frequency range can be changed by varying the value of the capacitance used.

b. *Capacitance multiplier*

To test the functionality of the proposed capacitance multiplier, the proposed C-multiplier is used in the design of an

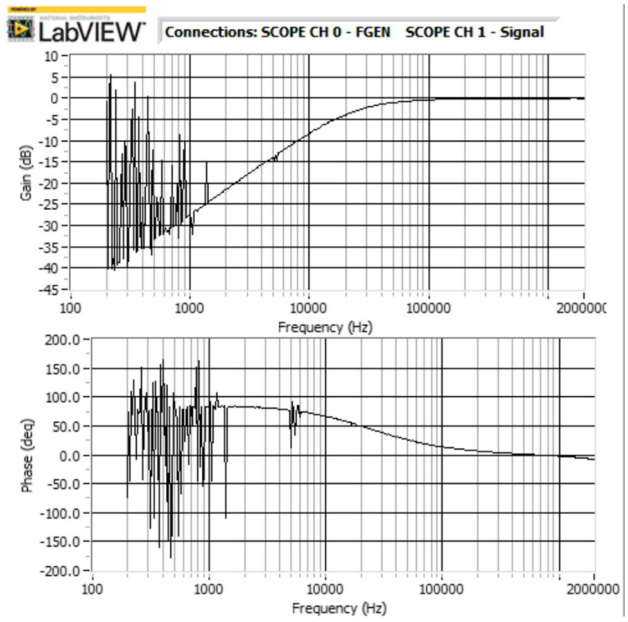

Fig. 12 Experimental results for the high pass filter frequency response

RC low pass filter with $R = 1\,\text{k}\Omega$, $R_1 = 10\,\text{k}\Omega$ and C = 1 nF. The bias current of the OTA is varied from 0.2 to 2 mA. Plots of the frequency response of the filter are shown in Fig. 8. It is evident from the plots that the filter is working properly with tunable − 3 dB frequency.

The transient analysis for the low pass filter is carried out using the same components. The simulation results shown in Fig. 9 indicates that the circuit is working properly.

c. *Resistance multiplier*

The proposed resistance multiplier is used in the design of an RC high pass filter. In this design, $Z_1 = R_1 = 100\ \Omega$, is the resistor to be scaled up and $Z_2 = R_2 = 100\ \Omega$ and I_B can be varied such that the denominator is not zero. The frequency response shown in Fig. 10 confirms the functionality of the design.

3.2 Experimental Results

To verify the functionality of the proposed design experimentally, the proposed active inductor is used in the design of a tunable high pass filter with $R = 1\,\text{k}\Omega$ and the active impedance parameters $R_1 = 10\,\text{k}\Omega$ and $C_2 = 1$ nF(measured 1.2 nF). Plots of the transient response for different bias currents using 15 mV signal at the − 3 dB frequency are shown in Fig. 11.

It is clear from the plots that the active inductor is working properly.

The high pass filter circuit using AI was simulated for THD using different bias current and ($I_B = 0.2$ mA, 1 mA, and 2 mA). The THD is, respectively, 0.484%, 0.019%, and 0.005%) which is within the acceptable range.

The frequency response is also carried out for the bias current of 0.2mA. Plots of the frequency response are shown in Fig. 12. It is cleSar that the experimental results are in a good agreement with theory with small deviation as expected due to parasitic.

Comparison of the proposed AIS design with previous art is summarize in Table 1. It is clear from the table that the proposed design is better in terms of tunability, the number of functions, the number of passive components and the frequency range.

4 Conclusion

A new compact and tunable positive and negative active inductor simulator and impedance multiplier circuits are developed. The design is novel as it implement positive and negative inductor and simulate positive and negative capacitance and resistance multiplier. The functionality of the

Table 1 Summary of Performance Comparison

Ref#	Active building block	Power supply	Technology μm	# of passive elements		Frequency range	± AIS, ± R & ± C multiplier
				# of R G(F)	# of C G(F)		
[1]	1VCII	±0.9	0.18	(2)	1	1 kHz–10 MHz	+ AIS only
[2]	3 CFOA	NA	NA	2(1)	1(0)	1μHz–1 MHz	+ AIS only
[3]	1 CFOA	±15	NA	1(1)	0(1)	NA	+ AIS only
[17]	2CFOA	±5	NA				
[18]	1 E-VCII	±0.3	0.18	0	(1)	80 Hz–40 kHz	± C multiplier only
[19]	1 INIC, 1 VNIC	±0.75	0.13	0(2)	1(0)	100 Hz–50 MHz	+ AIS
[20]	1 MD VCC	±0.75	0.13	0(2)	1(0)		+ AIS
This work	1 VCII and 1 OTA	±5	NA	1(1)	1	100 Hz–10 MHz	All

F Floating, *G* Grounded

designs were confirmed using and simulation and experimental test using the commercially available ICs. The developed designs can be used as core bock in many analog signal-processing applications.

Acknowledgements The authors acknowledge the support of King Fahd university of Petroleum & minerals.

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