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RESEARCH ARTICLE-ELECTRICAL ENGINEERING

High Performance Three-Phase, Three-Port, Five-Level, DC/AC Inverter Based Switched Capacitor Circuit for Renewable Energy Application

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Abstract

Integration of multilevel inverters with renewable energy sources have been the subject of many research projects. Numerous topologies of multilevel inverters have been investigated for stand-alone and grid-connected PV systems. The high number of switching devices, complexity, large size, voltage imbalance, and high cost are main drawbacks of the conventional topologies. This paper presents a new three-phase, three-port, five-level inverter based on a switched-capacitor circuit for PV applications. Compared to the conventional topologies, the proposed inverter has voltage boosting capability and multilevel operation without using clamping diodes or flying capacitors, simplifying the control algorithms and improving the reliability, efficiency, and lifetime. The presented multilevel inverter offers 25% reduction in power devices counts and 50% reduction in flying capacitors. The proposed inverter solves the capacitor voltage balancing issue of the conventional topologies and achieves the lowest voltage stress, making it suitable for high voltage applications. Additionally, the new topology harnesses the superior features of silicon-carbide devices; hence, a fast-switching speed can be employed to reduce size of the storage elements and output filter requirements. Furthermore, the soft-switching operation is realized to regulate the charging current of the capacitor. The operating principle of the proposed topology is investigated, and its properties are compared to the traditional multilevel inverters. A laboratory prototype was built to validate the effectiveness of the proposed circuit, simulation and experimental results for the proposed inverter are provided.

Keywords Renewable energy · Three-phase DC–AC inverter · Silicon carbide devices · Switched-capacitor circuit · Soft-switching operation

1 Introduction

Currently, interest in renewable energy sources, such as photovoltaics (PVs) and wind turbines, is increasing, and they are considered to have significant potential. According to the International Energy Agency report in 2020, the global PV installed capacity has crossed 620 GW [1]. Residential PV applications can be classified into two main groups: grid-connected or stand-alone. In the grid-connected mode, the house is connected to a low-voltage utility grid, and the surplus power is diverted into the power grid. The stand-alone PV system is more suitable for houses that cannot be reached by the electrical grid. However, in this case, the system is more complex since battery packs are needed to store the energy to be used when additional energy is needed.

Power electronics are vital in PV systems. The generated outputs of the PV panels need to go through multiple conversion stages to achieve high-quality AC power. For high efficiency, more compact and lightweight power converters are required [2, 3]. Over the years, multilevel inverters have received interest, owing to their attractive features in power quality regulations [4]. Among different types of DC–AC inverters, multilevel inverters usually have lower harmonic contents, devices with lower rated power, lower filtering requirements, and higher voltage capabilities [5]. Additionally, some multilevel inverters enable transformerless operation and can increase the generated staircase output voltage without increasing the device rating.

Traditional topologies of multilevel inverters include neutral-point diode clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) inverters [6]. These topologies are currently implemented in a wide range of applications,

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such as blowers, grinding mills, and flexible AC transmission lines (FACTs) applications [7, 8]. However, various disadvantages limit each topology. In the NPC topologies proposed in [9–12], the main drawback is the unbalanced voltage of the input series-connected capacitors. Also, several clamping diodes are required to generate a higher level of output voltage [13]. Furthermore, with the recently proposed active NPC topology, such as T-type [14] or E-type [15], the replacement of clamping diodes with active switching devices makes the system more complex and results in additional conduction losses. Hence, the main drawback is still not effectively solved. The traditional FC inverter topologies proposed in [16–18] are composed of a series connection of units. Each unit consists of one FC and two power-switching devices. However, FC inverters are also limited to three-level applications because of the unbalanced voltage over the flying capacitors as the number of voltage levels increases. Another drawback is that an FC inverter with more than three levels requires many flying capacitors, which may require a large converter. The CHB multilevel inverter topologies proposed in [19] and [20] are composed of several units of H-bridge inverters connected in series with an isolated input DC source for each unit. This topology is commonly used in the industry for its high efficiency and modularity. However, the main disadvantage is the need for an isolated input DC source for each H-bridge inverter, which in turn increases the inverter size. Additionally, as the number of voltage levels increases, the numbers of DC sources and H-bridge inverters significantly increase.

The recently proposed multilevel inverters overcome the aforementioned drawbacks of the conventional multilevel inverter with the main objectives to reduce switches count, reduce number of DC sources, and reduce the voltage stress on power switches. In [21], fifteen level multilevel inverter is proposed to overcome the problem of the high number of DC sources, however, the topology requires ten power switches and three dc source to generate fifteen level. The high number of switches is the main drawbacks. A modular multilevel topology with symmetric configuration is introduces in [22]. The topology uses ten bidirectional switches and seven isolated DC source to generate fifteen level. The limitation of this topology is the high number of DC sources. In practical applications, this configuration requires additional capacitors which further increase the systems size. The drawback with this multilevel inverter can be overcome with the proposed packed U-cell multilevel inverter in [23] where less number of switches can be employed to generate fifteen voltage levels. However, using diodes prevent the bidirectional power flow in thus topology. To reduce the voltage stress of the power devices, the multilevel inverter presented in [24] combine the T-yple multivalve inverter with the three-level H-bridge inverter. This topology requires at least twelve power switches with four diodes. However, the high number of power switches making the topology less efficient and unaffordable. The switched capacitor circuit can be alternative solution to reduce the number of power switches and reduce the voltage stress. In [25], a new K-type is presented to generate thirteen voltage level. The topology requires one DC source, four capacitors and ten power switches. The main advantage is the auto-balance of the capacitor's voltages. However, the high number switching devices is a massive drawback of this topology. A new seven-level-PUC Multi-Cells Modular Multilevel Converter for AC-AC and AC-DC Applications is proposed in [26]. The required arm inductors is a big disadvantages of PUC topology. Complex control is another disadvantage where the control and balance of cell capacitors voltages is required. Moreover, circulating current has to be minimized and this requires another layer of control. Packed E-Cell (PEC) multilevel topology to achieve nine-level is proposed in [27]. The problem with this topology is difficult control to balance the voltage of dc-link capacitors. Also, some power devices need bidirectional voltage blocking, and this require extra gate drive circuit and additional layer of control.

In this paper, a switched capacitor–based multilevel inverter is proposed to overcome the drawbacks of traditional multilevel inverters. The proposed topology employs fewer components as compared to the conventional topologies. The capacitor voltage balancing problem in conventional NPC and FC inverters is addressed by the frequent charging of the capacitors in series to a constant voltage. Moreover, a switched-capacitor circuit avoids the drawback of multiple DC sources in a CHB inverter by using a single voltage source to generate higher voltage levels. Unlike traditional inverters, the proposed topology can boost the input voltage by charging the capacitors in parallel with the input voltage and discharging to the load by connecting the capacitors in series with the input voltage source. Furthermore, the maximum voltage stresses of the switches are limited to the input DC voltage, making the proposed inverter an excellent candidate for high-voltage PV power applications. In addition, the proposed inverter benefits from the superior features of silicon carbide (SiC) devices in high switching frequencies to reduce the size of passive components, such as capacitors and output filters [28]. The high-temperature capability of silicon carbide devices will further reduce the requirement of a cooling system. In the proposed topology, the stray inductance in the printed circuit board (PCB) traces is utilized to regulate the charging current and realize soft-switching. Finally, using a switching capacitor circuit allows for desirable inverter features, including small size, lightweight, large power density, and low harmonic components.

The rest of the paper is organized as follows. The proposed multilevel switched-capacitor inverter and its operation principle are presented in Sect. 2. The soft-switching analysis is described in Sect. 3, and the power losses analysis is pre-

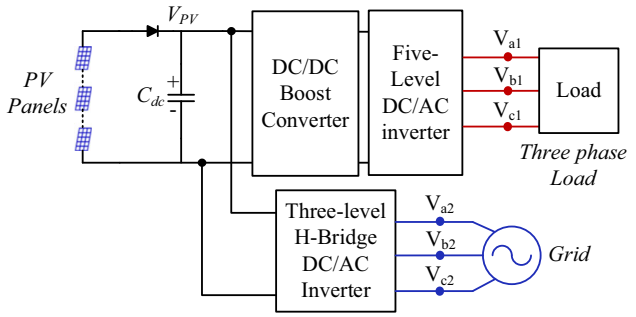


Fig. 1 System diagram of the conventional five-level three-port DC/AC converter

sented in Sect. 4 and the control algorithm is described in Sect. 5. The simulation and experimental results are illustrated in Sect. 6, and the conclusion is given in Sect. 7.

2 Proposed Three-phase Three-Port Five-Level Inverter

2.1 System Overview

In contrast to the traditional multiport, multilevel inverter topologies that involve several stages as depicted in Fig. 1, the proposed topology involves only a single-stage power conversion with three-port structure, as seen in Fig. 2. A single-stage DC-AC converter with boosting capability offers an interesting alternative compared to two-stage approaches. The proposed topology omits the intermediate stages since the system resources are shred. Multi-port, multi-level converters based switched capacitors can obtain higher DC voltage utilizations and become a research hotspot today. This paper presents a novel switched-capacitor-based three-phase, three-port, five-level inverter with reduced number of components. The proposed inverter is designed in a way that just one DC source is required to generate different voltage levels. Compared to conventional multilevel topologies, the proposed topology features many advantages (1) single stage conversion with boosting functionality (2) deployment of switched-capacitor circuit with no need for large inductors and transformers (3) low number of semiconductor devices, (4) soft switching operation that reduce the electromagnetic interference and switching losses (5) self-balancing of capacitor and (6) reduced voltage stress on the switches. Moreover, using the silicon carbide devices enable the converter to operate at higher switching frequencies, enabling a dramatic shrink in the size and cost of capacitors and inductors, which then reduces the overall system cost.

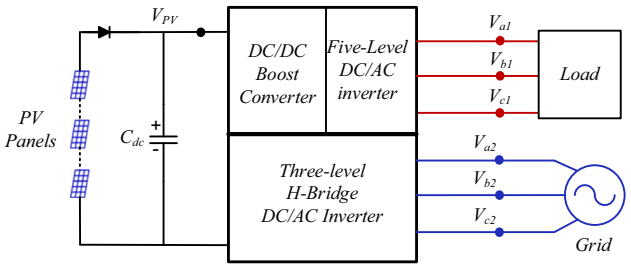


Fig. 2 System diagram of the proposed five-level three-port DC/AC converter

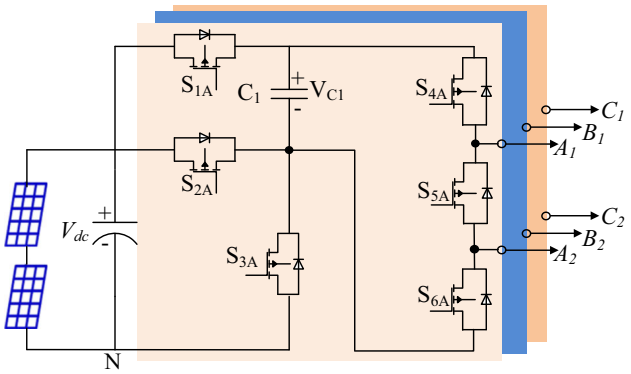


Fig. 3 The schematic of the proposed three-phase three-port five-level inverter

2.2 Circuit Configuration

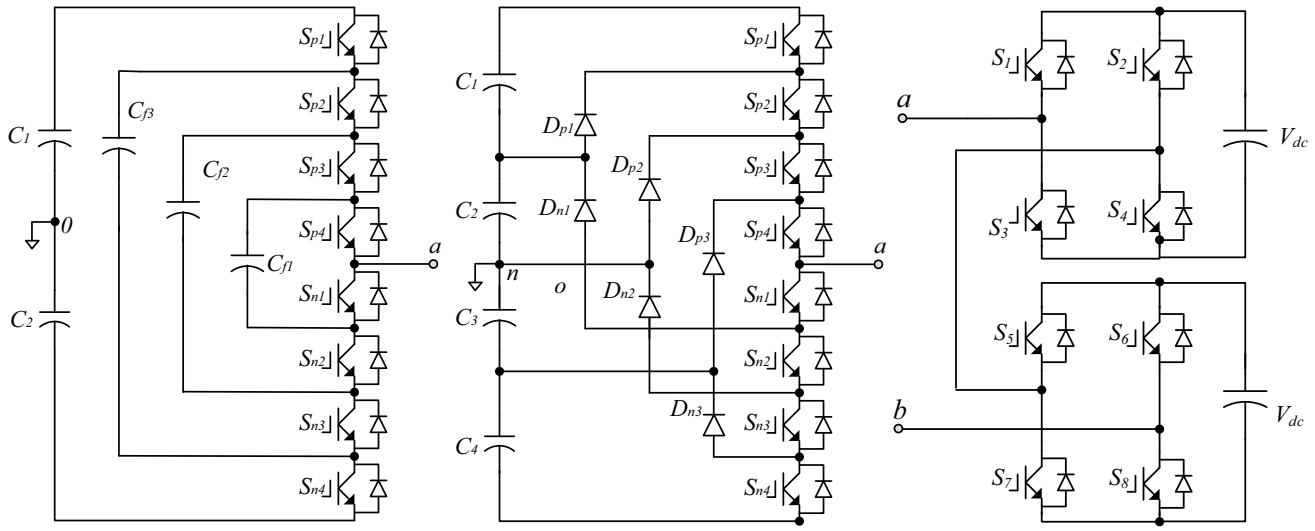
The schematic of the proposed three-port five-level inverter is shown in Fig. 3. The three-phase legs share the same DC source, reducing the number of DC-link capacitors. Each phase leg combines a switched-capacitor unit with a half-bridge inverter. The switched-capacitor unit in phase A contains one intermediate capacitor C_1 and three power switches S_{1A} and S_{3A} working in complementary with switch S_{2A}. Also, a two-port inverter can be formed; the first has the pole voltage V_{A1N}, resulting from switches S_{4A} and S_{5A}. The second has the pole voltage V_{A2N} from switches S_{5A} and S_{6A}. By switching the capacitor C_1 and the input DC source between series and parallel, node A_1 acts as a five-level inverter with a maximum pole voltage $V_{A1N,\max} = 2V_{\mathrm{dc}}$, while node A_2 serves as a three-level inverter with a maximum pole voltage $V_{A2N,\max} = V_{\mathrm{dc}}$.

2.3 Comparative Study with the Conventional Topologies

The proposed inverter is compared with recently published conventional multilevel inverter topologies. A summary of the comparative study is provided in Table 1, clarifying the prominent advantages of the proposed topology. The counterpart topologies are the NPC, FC, and CHB multilevel

Table 1 Comparison of the conventional five-level inverters and the proposed inverter

	5L-NPC	5L-FC	5L-CHB	[29]	[30]	[31]	[32]	Proposed 5L-inverter
No. of active switches	24	24	24	24	24	21	24	18
No. of diodes	18	0	0	2	0	4	0	0
No. of flying capacitors	0	9	0	6	3	6	3	3
No. of DC-bus capacitors	4	2	2	1	2	1	1	1
Front-end boost stage	No	No	No	Yes	No	Yes	No	Yes
Maximum voltage stress	V_{dc}	V_{dc}	V_{dc}	$2V_{dc}$	V_{dc}	$2V_{dc}$	$2V_{dc}$	V_{dc}
Capacitor self-balance control	No	No	–	Yes	No	Yes	Yes	Yes
No. of DC power supply	1	1	2	1	1	1	1	1
Soft-switching operation	No	No	No	No	No	No	No	Yes



(a) Five-lev FC inverter **(b)** Five-level NPC inverter **(c)** Five-level CHB inverter

Fig. 4 The conventional five-level DC/AC inverter

inverters as shown in Fig. 4. The topologies are quantitively compared in terms of the number of switching devices, diodes, capacitors, and input DC sources, as well as maximum voltage stress. Table 1 shows that the conventional topologies require a high number of semiconductor devices to realize a five-level operation. The FC inverter, NPC inverter and CHB inverter require at least twenty-four switching devices while the proposed inverter only has eighteen switching devices to generate a five-level output voltage. Hence, the employed number of switches in the proposed topology is less by 25%. Additionally, the FC inverter requires more six flying capacitors, and the NPC inverter requires eighteen clamping diodes while the proposed inverter only require three flying capacitors to achieve the same functionality. The flying capacitors in FC converter is 50% higher when compared to proposed topology. Moreover, the flying capacitor voltage as well as the DC-link voltage are difficult to balance in FC inverter and NPC inverter, respectfully, while the voltage balancing over the capacitors in proposed inverter can be achieved automatically. Hence, the system complexity and reliability are improved. The proposed topology offers a single-stage DC-AC converter with inherent boosting capability while other topologies require an extra DC-DC stage to achieve a voltage up to two times of the output voltage. However, the new stage requires additional semiconductor devices and passive components which eventually lead to a large system size and less efficiency. Furthermore, among the compared topologies, the proposed inverter shows the lowest voltage stresses. For the five-level FC and five-level CHP, the voltage stresses are $V_{dc}/2$. However, for the five-level CHB inverter, the voltage stresses are V_{dc}. The topologies proposed in [29–32] are based on switched capacitors circuit. However, these topologies still require high number of switching devices and flying capacitors. Topologies in [29, 30, 32] require twenty-four switching devices to generate three-phase, five-level inverter. However, topologies in [29, 31] require more clamping diodes and flying capacitors compared to other since it consists of front-end boosting stage.

Table 2 Five-level Output voltage and switching states of the circuit in Phase A only

Switching state	V_{A1N}	V_{A2N}	S_{1A}	S_{2A}	S_{3A}	S_{4A}	S_{5A}	S_{6A}
1	0	0	1	0	1	0	1	1
2	V_{dc}	0	1	0	1	1	0	1
3	V_{dc}	V_{dc}	1	0	1	1	1	0
4	$2V_{\mathrm{dc}}$	V_{dc}	0	1	0	1	0	1

The topology in [30] shows less voltage stress compared to other, however, this topology require additional layer of control since dc-bus capacitor voltages cannot be self-balanced. The table shows that the proposed topology is superior to other topologies with a fewer number of switching devices, fewer number of flying capacitors, and less voltage stresses. Furthermore, the proposed inverter is capable to run with soft switching for some devices which is not applicable for other topologies, the switching losses and electromagnetic interference noise can be further mitigated. In general, the proposed five-level inverter achieves high performance compared to other topologies, especially, in term of components count, system complexity and DC voltage utilizations.

2.4 Circuit Operating Principle

The operating principles of both five-level and three-level inverters are addressed in this section. The inverter switches are controlled to generate three unipolar voltage levels of 0, V_{dc}, and $2V_{\mathrm{dc}}$ in the pole voltages V_{A1N}, V_{B1N}, and V_{C1N} and two unipolar voltage levels of zero and $\mathrm{V_{DC}}$ in the pole voltages V_{A2N}, V_{B2N}, and V_{C2N}, respectively. Five-level bipolar voltages can be produced in the line voltages by subtracting the corresponding pole voltage in each phase leg. For example, the line-to-line voltage V_{A1B1} can be synthesized by subtracting the pole voltage V_{A1N} from V_{B1N}, generating five-level voltages of $-2V_{\mathrm{dc}}$, $-V_{\mathrm{dc}}$, 0, V_{dc}, $2V_{\mathrm{dc}}$. However, the line-to-line voltage V_{A2B2} can be synthesized by subtracting the pole voltage V_{A2N} from V_{B2N}, generating the three-level voltages $-V_{\mathrm{dc}}$, 0, and V_{dc}. The switching states for generating the five-level voltage V_{A1B1} and three-level voltage V_{A2B2} are illustrated in Table 2. The states are defined such that "0" refers to the OFF state, and "1" refers to the ON state of the related switches. The current paths in each operating switching state are shown in Fig. 5a–d. The following switching states analysis applies to the circuit in phase A; the circuits in phases B and C experience the same analysis, but the output voltage is shifted by $-120°$ and 120°, respectively.

2.4.1 Switching State 1 ($V_{A1N} = 0, V_{A2N} = 0$)

Figure 5a depicts the equivalent circuit for *switching state* 1. The front-end circuit switches S_{1A} and S_{3A} are ON while S_{2A} is OFF. During this state, capacitor C_1 is connected in parallel with the input DC source and charged to V_{dc}. In the half-bridge inverter, S_{4A} is OFF while switches S_{5A} and S_{6A} are ON. The pole voltages across both nodes A_1 and A_2 are zero.

2.4.2 Switching State 2 ($V_{A1N} = V_{\mathrm{dc}}, V_{A2N} = 0$)

The equivalent circuit is shown in Fig. 5b and labeled as *switching state 2*. The switches in the front-end circuit maintain the same switching pattern as in *state 0*. However, in the half-bridge inverter, the switches S_{4A} and S_{6A} are ON while S_{5A} is OFF. The pole voltage at node A_1 becomes $V_{A1N} = V_{\mathrm{dc}}$, and node A_2 has a pole voltage of zero, $V_{A2N} = 0$.

2.4.3 Switching State 3 ($V_{A1N} = V_{\mathrm{dc}}, V_{A2N} = V_{\mathrm{dc}}$)

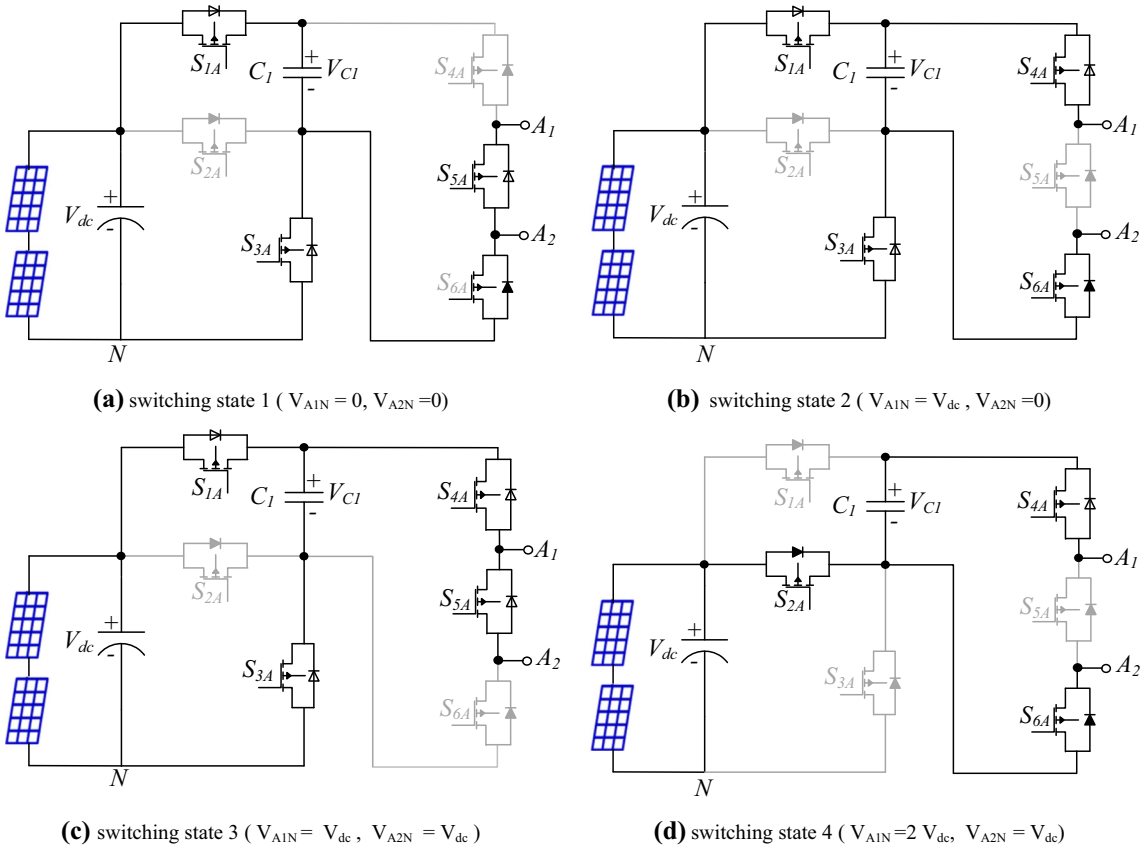
Figure 5c illustrates the equivalent circuit of *switching states 3*. In Fig. 3c, the switches in the front-end stage S_{1A} and S_{3A} are ON while S_{2A} is OFF, and capacitor C_A is still in charging mode. In the half-bridge stage, the switches S_{4A} and S_{5A} are ON while S_{6A} is OFF. The pole voltage at node A_1 becomes $V_{A1N} = V_{\mathrm{dc}}$, and node A_2 has the pole voltage $V_{A2N} = V_{\mathrm{dc}}$. Another redundant *switching state 3* can be realized by turning ON switches S_{2A}, S_{6A}, and S_{5A} and turning OFF switches S_{1A}, S_{3A}, and S_{4A}, connecting the DC source to nodes A_1 and A_2.

2.4.4 Switching State 4 ($V_{A1N} = 2V_{\mathrm{dc}}, V_{A2N} = V_{\mathrm{dc}}$)

The equivalent circuit is shown in Fig. 5d, labeled as *switching state 4*. In the front-end stage, switch S_{2A} is ON and switches S_{1A} and S_{3A} are OFF, thereby connecting capacitor C_1 in series with the input DC source. In the half-bridge stage, switch S_{4A} and S_{6A} are ON while switch S_{5A} is OFF, and C_1 is discharging in series with the DC source, resulting in $2V_{\mathrm{dc}}$ at node A_1 through S_{4A} and V_{dc} from node A_2 through S_{6A}.

2.5 Modulation Strategy

Since the proposed topology features fewer switching devices, some switching constraints are imposed in the modulating design. To solve these constraints, a sinusoidal pulse width modulation (SPWM) technique is applied. Figure 6 illustrates the modulation scheme for the inverter operation, where V_{ref_A1} and V_{ref_A2} are the modulating reference waveform for the pole voltage V_{A1N} and V_{A2N}. The modulation



(a) switching state 1 ($V_{A1N} = 0$, $V_{A2N} = 0$) **(b)** switching state 2 ($V_{A1N} = V_{dc}$, $V_{A2N} = 0$)

(c) switching state 3 ($V_{A1N} = V_{dc}$, $V_{A2N} = V_{dc}$) **(d)** switching state 4 ($V_{A1N} = 2V_{dc}$, $V_{A2N} = V_{dc}$)

Fig. 5 Four switching states for the three-port five-level inverter

reference waveforms for the circuit in phase A can be defined as

$$V_{ref\_A1}(t) = 2m_{A1}\sin(\omega t)$$
$$V_{ref\_A2}(t) = m_{A2}\sin(\omega t) + 1 \quad (1)$$

where m_{A1} and m_{A2} are modulation indices for pole voltages V_{A1N} and V_{A2N}, respectively.

To prevent the two modulating waves from intersecting, the voltage reference $V_{ref\_A2}(t)$ is lifted to the top by adding proper DC offsets. In this way, the inverter operation constraints are satisfied. Figure 7a illustrates the modulation scheme in a single switching period for the proposed inverter when the modulating reference waveforms are in the first half-cycle, compared with a common triangular carrier. In this case, the pulse width modulation (PWM) signals for switches S_{1A}–S_{6A} are generated such that the instantaneous time T_{A2} of the reference $V_{ref\_A2}(t)$ must be no less than the instantaneous time T_{A1} of reference $V_{ref\_A1}(t)$. However, when the reference $V_{ref\_A1}(t)$ passes to the negative half cycle, in this case, as illustrated in Fig. 7b, the two modulating reference waveforms are compared to different triangular carriers and arranged such that the instantaneous time T_{A1} of $V_{ref\_A1}(t)$ is not less than T_{A2} of $V_{ref\_A2}(t)$ at any instant of time. Therefore, PWM signals for switches S_{1A}–S_{6A} in the second half-cycle are generated such that the instantaneous time T_{A1} is longer than the instantaneous value T_{A2}.

3 Soft-Switching Operation

The main obstacle of the switched-capacitor circuit is that the charging current of the capacitor is not regulated. Hence, the switches in the path of charging current experience high pulses. In the proposed topology, the stray inductance in the PCB traces is utilized to regulate the charging current; hence, power devices realize soft-switching. The proposed soft-switching scheme is only applied to the switches located in the charging path of the capacitors. The main purpose is to minimize the associated power losses and reduce the electromagnetic interference (EMI) due to an unregulated charging current. Figure 8a shows the equivalent circuit of the capacitor charging loop in the circuit of phase A. By neglecting the equivalent resistance in the charging loop, the charging path can be represented only by the LC circuit. Under this assumption, the charging current that flows through switches S_{1A} and S_{3A} is sinusoidal. The current profile of capacitor C_1

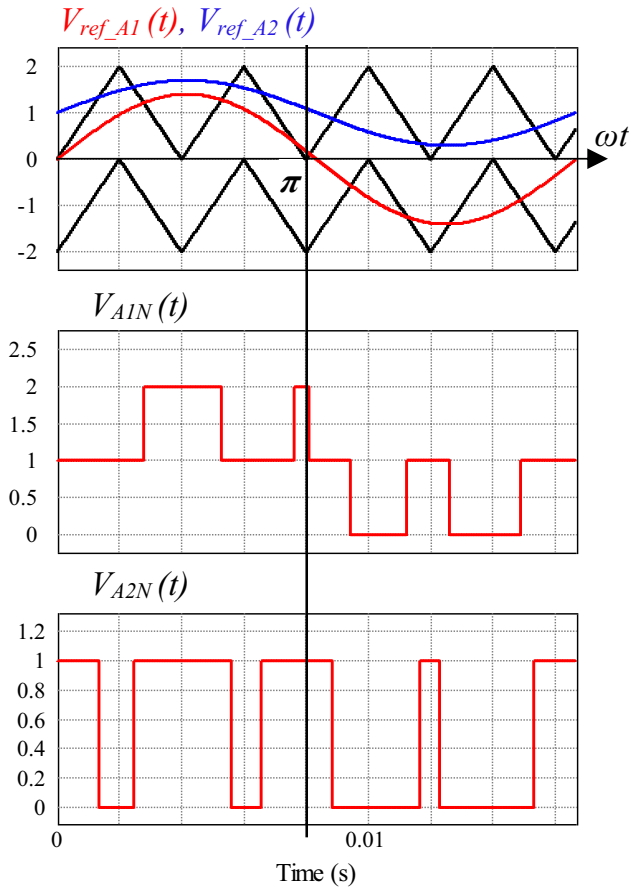


Fig. 6 Schematic diagram of the PWM technique

is shown in Fig. 8b. Capacitors C_2 and C_3 in phase B and phase C have the same current profiles.

To implement the soft-switching method in the proposed inverter, a variable switching-frequency algorithm is adopted. The main goal is to keep the charging time of the capacitor constant. The following equation describes the relationship between the charging time of the capacitor and the instantaneous duty ratio:

$$T_{ch}(t) = (1 - D(t))\frac{1}{f_s(t)} \tag{2}$$

The instantaneous duty ratio $D(t)$ during the charging/discharging process of capacitor C_1 can be defined as

$$D(t) = \begin{cases} 2m_{A1}\sin(\omega t) & 0 \le t \le DT_s \\ 2 - 2m_{A1}\sin(\omega t) & DT_s \le t \le T_s \end{cases} \tag{3}$$

From (5) and (6), the variable switching frequency $f_s(t)$ can be calculated as

$$f_s(t) = \frac{2(1 - D(t))}{T_{\text{osc}}} \tag{4}$$

where $T_{osc} = \pi\sqrt{L_s C_1}$ is the resonance time of the charging current.

Equation (4) illustrates the relation between the instantaneous duty ratio $D(t)$ and the switching frequency $f_s(t)$. Since the switching frequency varies from cycle to cycle, the voltage variation should be minimized to prevent the capacitor from being over-discharged. Therefore, the capacitor voltage ripple in one switching cycle is calculated from the following equation:

$$\begin{aligned} \Delta V_{C1} &= \frac{1}{C_1} D(t) i_{A1}(t) \frac{1}{f_s(t)} \\ &= \frac{1}{2}\frac{1}{C_1} i_{A1}(t) T_{\text{osc}} \left(\frac{1}{1 - D(t)} - 1\right) \end{aligned} \tag{5}$$

Equation (5) clearly states that the voltage variation increases with the inverter current $i_{IA}(t)$ and the instantaneous duty ratio $D(t)$. The maximum voltage variation occurs at a unity power factor when the inverter current $i_{IA}(t)$ and the duty ratio $D(t)$ reach their maximum value simultaneously. Hence, Eq. (4) becomes

$$\Delta V_{C1\_max} = \frac{1}{2}\frac{1}{C_1} I_{A1\_peak} T_{\text{osc}} \left(\frac{m_{A1}}{1 - m_{A1}}\right) \tag{6}$$

By using the current-second balance, the maximum charging current of the capacitor can be calculated from the following:

$$\frac{1 - D(t)}{\pi} \int_0^{\pi} I_{C1\_peak} \sin(\theta) d\theta = D(t) i_{A1} \tag{7}$$

Solving Eq. (7), the peak charging current in phase A can be obtained from

$$I_{S3A\_peak} = I_{C1\_peak} = \frac{\pi}{2}\left(\frac{1}{2 - 2m_{A1}}\right) I_{A1\_peak} \tag{8}$$

Equation (8) estimates the maximum capacitor charging current. Both the modulation index and the phase current directly impact the maximum charging current. Switch S_{1A} in phase A (see Fig. 5c), carries both the charging current $i_{C1}(t)$ and the inverter current $i_{A1}(t)$. Switch S_{1A} experiences the highest current stress. Therefore, the peak current value of switch S_{1A} is

$$I_{S1A\_peak} = \left(\frac{\pi}{4 - 4m_{A1}} + 1\right) I_{A1\_peak} \tag{9}$$

4 Power Losses Analysis

In this section, power losses are analyzed to study the effect of load value and switching frequency on system efficiency. The inverter mainly uses the capacitor and semiconductor devices

to perform the energy transfer tasks; therefore, a major part of the losses is dissipated in the semiconductor devices. Two types of losses are considered—conduction and switching losses.

4.1 Conduction Losses

The conduction losses of the inverter are caused by the on-state resistance R_{on} in the semiconductor devices when the current flows through them. Therefore, estimating the conduction losses mainly depends on the device parameters, load current, and the average value of the duty cycle. During the positive half cycle when the reference waveform $V_{refA1}(\theta) > 0, \theta \in [0, \pi]$, the duty ratios $d_{A1}(\theta)$ and $d_{A2}(\theta)$ are given by

$$\begin{cases} d_{A1}(\theta) = \frac{2m_{A1}\sin\theta}{2} & 0 \le \theta \le \pi \\ d_{A2}(\theta) = \frac{m_{A2}\sin\theta+1}{2} & \pi \le \theta \le 2\pi \end{cases} \tag{10}$$

However, when the reference $V_{refA1}(\theta)$ is in the negative half cycle, $\theta \in [\pi, 2\pi]$, the duty ratio is given by

$$\begin{cases} d_{A1}(\theta) = \frac{2m_{A1}\sin\theta+2}{2} & 0 \le \theta \le \pi 0 \le \theta \le \pi \\ d_{A2}(\theta) = \frac{m_{A1}\sin\theta+1}{2} & \pi \le \theta \le 2\pi \end{cases} \tag{11}$$

The total power conduction losses for the circuit in phase A equals the sum of the conduction losses of the switches S_{1A}–S_{6A}:

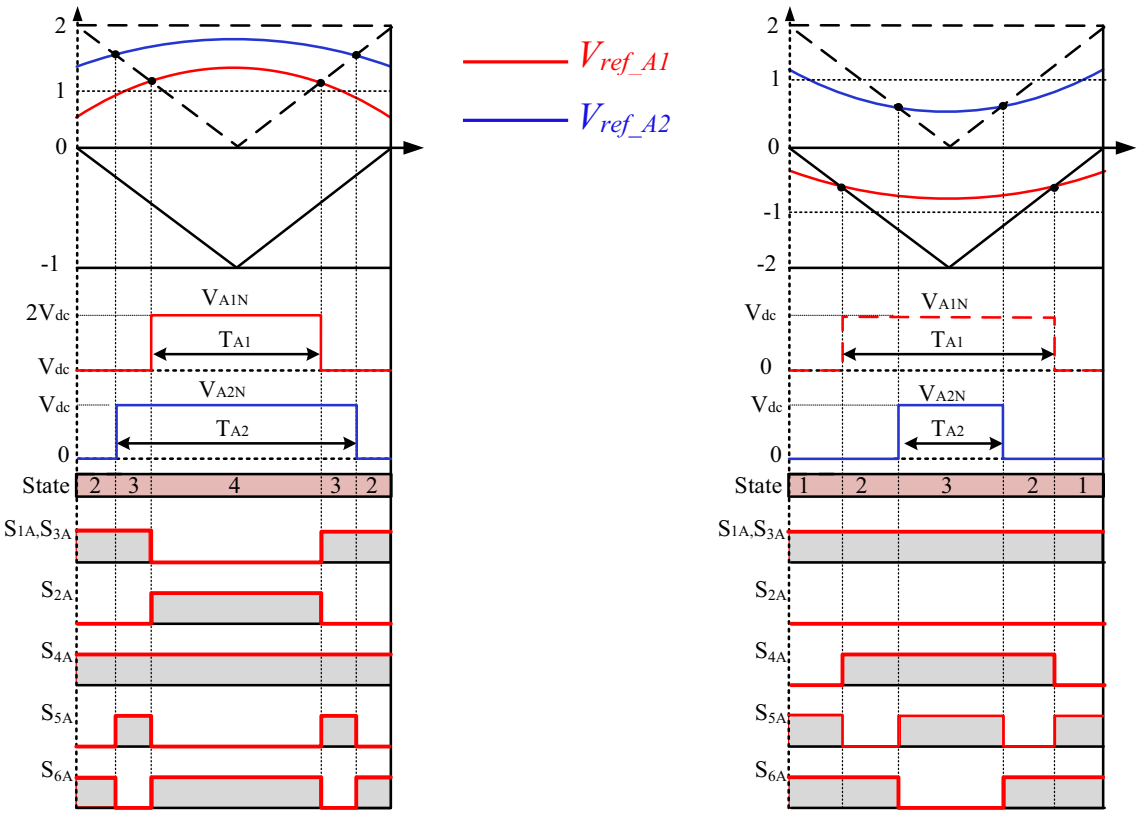
$$P_{con\_\phi A} = P_{S1A} + P_{S2A} + P_{S3A} + P_{S4A} + P_{S5A} + P_{S6A} \tag{12}$$

Since the circuit structures in the three phases are identical, the total conduction losses of the inverter are the sum of three phases:

$$P_{con\_3\phi} = 3P_{con\_\phi A} \tag{13}$$

4.1.1 Conduction Loss of Switch S_{1A}

Two currents are supported by switch S_{IA}. During the first half of the cycle, S_{IA} conducts the capacitor's charging current $i_{C1}(t)$, and both phase currents $i_{A1},(t)$ and $i_{A2}(t)$ flow through switches S_{4A} and S_{5A}, respectively. Since no charging/discharging operation occurs in the second half of the cycle, no current flows through S_{IA}. The conduction loss P_{Cond_S1A} can be written as



(a) Switching states when $V_{ref\_A1} > 0$ **(b)** Switching states when $V_{ref\_A1} < 0$

Fig. 7 Switching states of the proposed converter

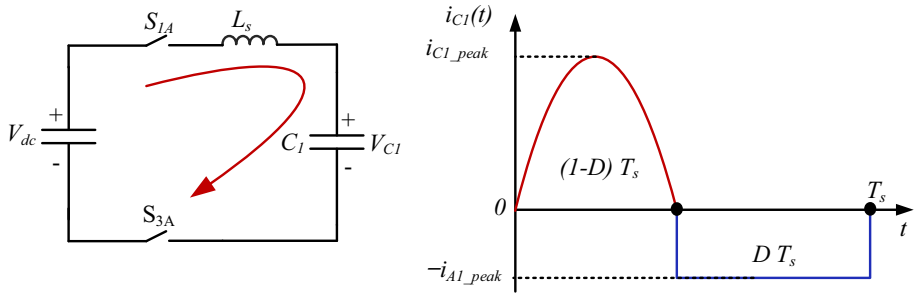


Fig. 8 Equivalent circuit during capacitor charging and current profile

(a) Circuit during capacitor charging **(b)** Charging/discharging current profile

$$P_{Cond\_S1A} = \left[\frac{1}{2\pi}\left(\int_0^{\pi}((1-d_{A1}(\theta))(i_{A1}(\theta)+i_{C1}(\theta)) +(d_{A2}(\theta)-d_{A1}(\theta))i_{A2}(\theta))^2 d\theta + \int_{\pi}^{2\pi}(d_{A1}(\theta)i_{A1}(\theta)+d_{A2}(\theta)i_{A2}(\theta))^2 d\theta\right)\right] r_S \quad (14)$$

4.1.2 Conduction Loss of Switch S_{2A}

Switch S_{2A} is only active in the first half of the cycle, conducting phase current i_{A1} (t) and i_{A2} (t). The conduction loss through switch S_{2A} P_{Cond_S2A} is given by

$$P_{Cond\_S2A} = \left[\frac{1}{2\pi}\left(\int_0^{\pi}(d_{A1}(\theta)(i_{A2}(\theta)+i_{A2}(\theta)))^2 d\theta\right)\right] r_S \quad (15)$$

4.1.3 Conduction Loss of Switch S_{3A}

Switch S_{3A} carries capacitor current i_{C1} during the first half-cycle and phase currents i_{A1} (t) and i_{A2}(t) during the second cycle. The conduction loss P_{Cond_S3A} can be obtained as

$$P_{Cond\_S3A} = \left[\frac{1}{2\pi}\begin{pmatrix}\int_0^{\pi}((1-d_{A1}(\theta))i_{C1}(\theta) \\ -(1-d_{A2}(\theta))i_{A2}(\theta))^2 d\theta \\ +\int_{\pi}^{2\pi}((1-d_{A2}(\theta))i_{A2}(\theta) \\ +(1-d_{A1}(\theta))i_{A1}(\theta))^2 d\theta\end{pmatrix}\right] r_S \quad (16)$$

4.1.4 Conduction Loss of Switch S_{4A}

Switch S_{4A} conducts the phase currents i_{A1} (t) and i_{A2}(t). The conduction loss P_{Cond_S4A} is given as:

$$P_{Cond\_S4A} = \left[\frac{1}{2\pi}\begin{pmatrix}\int_0^{\pi}(i_{A1}(\theta)+(d_{A2}(\theta) \\ -d_{A1}(\theta))i_{A1}(\theta))^2 d\theta \\ +\int_{\pi}^{2\pi}(d_{A1}(\theta)i_{A1}(\theta) \\ +d_{A2}(\theta)i_{A2}(\theta))^2 d\theta\end{pmatrix}\right] r_S \quad (17)$$

4.1.5 Conduction Loss of Switch S_{5A}

Switch S_{5A} conducts the phase current i_{A1} (t) and i_{A2}(t) in the first half of the cycle. During the negative half-cycle, the switch carries the phase current i_{A1} (t) only. The conduction loss P_{Cond_S5A} switch S_{5A} is:

$$P_{Cond\_S5A} = \left[\frac{1}{2\pi}\begin{pmatrix}\int_0^{\pi}((d_{A2}(\theta)-d_{A1}(\theta))i_{A2}(\theta))^2 d\theta + \\ \int_{\pi}^{2\pi}(d_{A2}(\theta)i_{A2}(\theta)+(1-d_{A1}(\theta))(i_{A2}(\theta)+i_{A2}(\theta)))^2 d\theta\end{pmatrix}\right] r_S \quad (18)$$

4.1.6 Conduction Loss of Switch S_{6A}

Switch S_{6A} carries both phase currents i_{A1} (t) and i_{A2}(t) in one fundamental cycle, and the power loss of switch S_{6A} P_{Cond_S6A} can be estimated as

$$P_{Cond\_S6A} = \left[\frac{1}{2\pi}\begin{pmatrix}\int_0^{\pi}(d_{A1}(\theta)i_{A1}(\theta)+(1-d_{A2}(\theta))i_{A2}(\theta))^2 d\theta + \\ \int_{\pi}^{2\pi}((1-d_{A2}(\theta))i_{A2}(\theta)+(1-d_{A1}(\theta))i_{A1}(\theta))^2 d\theta\end{pmatrix}\right] r_S \quad (19)$$

4.2 Switching Losses of Power Devices

The switching losses of the presented topology are calculated based on the charging and discharging of the parasitic capacitor C_s of the semiconductor devices. For all switches, the capacitor C_s is charged to the maximum voltage V_{dc} when the switch is turned off and discharged to zero when the switch is turned on. Therefore, the switching losses can be calculated as follows:

$$P_{sw} = C_s {V_{dc}}^2 f_{sw} \quad (20)$$

where f_{sw} is the switching frequency of the switches and can be calculated from

$$f_{sw} = N_{sw} f_o \tag{21}$$

where N_{sw} is the number of switching transitions in one period. Therefore, the N_{sw} of a single switch can be obtained as

$$N_{sw} = \frac{t_s f_c}{T_s f_o} \tag{22}$$

where t_s is the operating time of the switches, which can be determined from Fig. 7. T_s is the switching time of one cycle. Therefore, the total switching losses P_{sw} can be calculated from the following:

$$P_{sw} = 18 \sum_{i=1}^{18} C_{si} {V_{dc}}^2 t_{si} f_{sw} \tag{23}$$

The efficiency of the proposed inverter can be obtained from

$$\eta = \frac{P_{o1} + P_{o2}}{P_{o1} + P_{o2} + P_{con} + P_{sw}} \tag{24}$$

where P_{o1} and P_{o2} are the output power of AC port 1 and AC port 2, respectively. The losses of the inverter can be calculated numerically at different levels of output power. The values of r_s, f_s, f_o, and C_s are estimated to be 25 mΩ, 150 kHz, 60 Hz, and 500 pF, respectively. The calculated efficiency of the proposed three-phase inverter is shown in Fig. 9a. The losses are obtained under the condition that output powers of the two ports are equal, i.e., $P_{o1} = P_{o2} = 1$kW, and the conduction and switching losses can be determined as $P_{con} = 0.12$ W and $P_{sw} = 0.3$ W. The breakdown of the losses is illustrated in Fig. 9b.

5 Control Algorithm

The Control block diagram of the proposed multiport multilevel inverter is illustrated in Fig. 10. The DQ reference frame technique is used at the grid port. This technique employs two control loops, outer loop, and inner loop. The outer loop is the voltage control, and the objective is to keep a stable dc-link voltage. The output of the maximum power point tracking (MPPT) controller, V_{PV}, is employed as input voltage reference to the outer loop. The PI controller is implemented to minimize the error between the input voltage reference and the feedback signal from the dc-link voltage. The output of PI is fed into the inner loop. The inner loop is the current control loop, where the feedback signal is the grid current. The objective of this loop is to track any sudden change in the input power and also to maintain a unity power factor at grid side. Therefore, in case of any sudden increase or decrease in the input power, the outer loop will clamp the dc-link voltage and the inner loop will track the grid current. Usually, the inner loop response very fast when compared to the outer voltage control. The phase looked loop (PLL) is employed for grid current synchronization. At the load port, a high-quality ac voltage must be guaranteed. And the control objective is to keep a stable ac voltage all the time. Figure 10 illustrates that the output voltage of the load is fed into the load voltage controller. The PI controller is employed to maintain a constant voltage by continuously adjusting the related modulated signal.

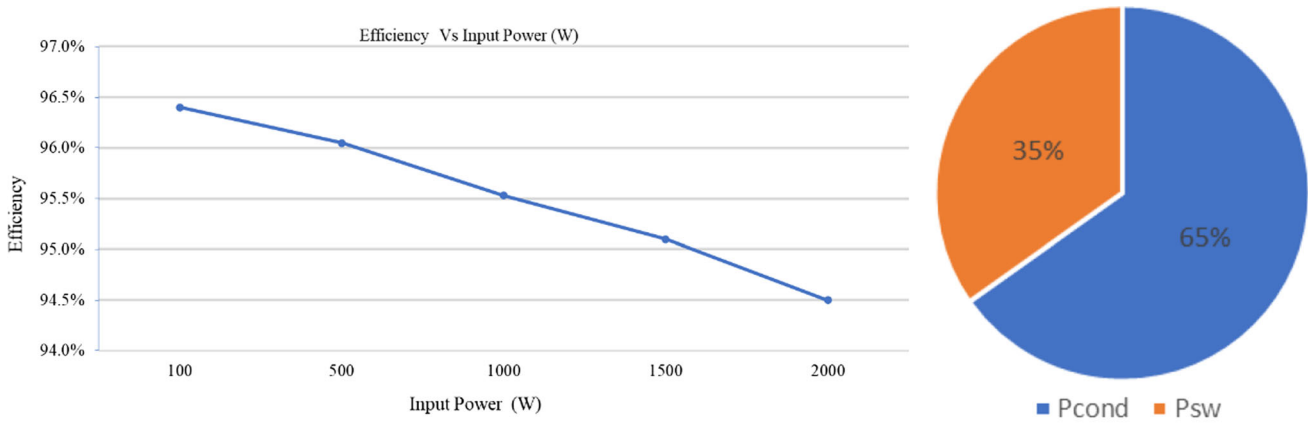
6 Simulation and Experimental Validation

6.1 Simulations Verification

To verify the effectiveness of the proposed three-phase topology, a simulation model was conducted using MATLAB. The topology was designed to operate in 240 V/120 V VAC. The DC bus was set to 200 VDC to coincide with the interface of a large PV array, with a line inductance of 2 mH and a switching frequency of 150 kHz. The modulation indices were equal for each port, $m_{A1} = m_{A2} = 0.8$. To achieve soft-switching, the stray inductance and capacitance in the charging loop were determined based on Eqs. (4) and (5) to be 140 nH and 50 μF, respectively.

Figure 11 shows the simulated waveforms of phase A unit. The five-level, line-to-line output voltage V_{A1B1} at load side, the three-level, line-to-line output voltage at grid side V_{A2B2}, the phase grid voltage V_g, and the phase current I_{A2} flows into grid port. It is very clear that the grid side voltage works in unity power factor since the phase voltage and phase current are in-phase, hence, the proposed control method is working effectively. Also, the figure shows that the five-level operation for the load port with step voltage 200 V making the line-to-line voltage approximately 240 Vrms. The grid port works with three-level and the line-to-line voltage is 120 Vrms. The phase current flows into the grid is approximately 4.8 Arms.

Figure 12 shows the simulation result for the three flying capacitor voltages V_{C1}, V_{C2}, and V_{C2}, the five-level load voltage (V_{A1B1}), and the load current (I_{A1}). The flying capacitor voltages are self-balanced with an average value of 200 Vdc, hence, the system does not require any additional layer of control. This is important advantage of the proposed inverter since the complexity of the system is reduced. Furthermore, the flying capacitors show a very small peak-to-peak ripple of about 3%, hence a small multilayer ceramic capacitor of about 5 μF is used. The load is inductive with 0.7 lag pf and the rms phase current is 4.2 A.



(a) Calculated efficiency at different power **(b)** Breakdown of losses

Fig. 9 Theoretical efficiency and losses analysis

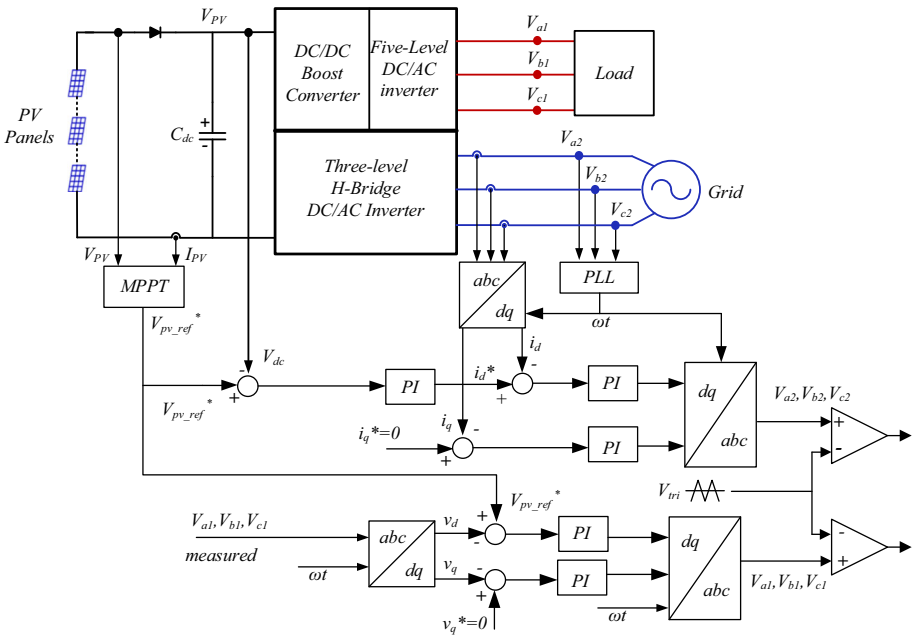


Fig. 10 Control block diagram of the proposed five-level three-port inverter

Figure 13 illustrates the dynamic performance of the proposed inverter. When a sudden change in load occurs, the proposed control algorithm must perform to maintain a stable system. The figure shows a step change occurs in the load current from half-load to full-load between the time 0.6–0.14 s. The average dc bus voltage is maintained constant at 200 V, however, the variation in the flying capacitors are increased due to the increase in the load current, hence a stable system is achieved.

Due to the unexpected variations in weather conditions, the solar irradiance is varied and simulated for analysis of the system. A PV-grid system model is built using MATLABSimulink with 9 solar modules connected in series and a total of 2 Kw power. Figure 14 shows the PV array output voltage Vs. current and power for different solar irradiance. The figure shows that the PV output current is directly proportional to the amount of the irradiance. The solar irradiance also has a direct impact on the output power, it can be seen that as the mount of solar irradiance increase the output power increases. In order to improve the system energy conversion efficiency, the maximum power point tracking (MPPT) is implemented to extract maximum power from PV panels. In this simulation, the perturb-and-observe (P&O) technique is applied for its simplicity and popularity.

The simulation result is shown in Fig. 15, initially, the simulation starts at t = 0, the irradiance is set at 1000 W/m^2 and the maximum output power of 2 kW is extracted from the PV modules. From $t = 0.14$ s, the irradiance is reduced from 1000 to 700 W/m^2, hence, the output power reduced from 2 to 1.4 kW. From $t = 0.27$ s, the solar irradiance is further

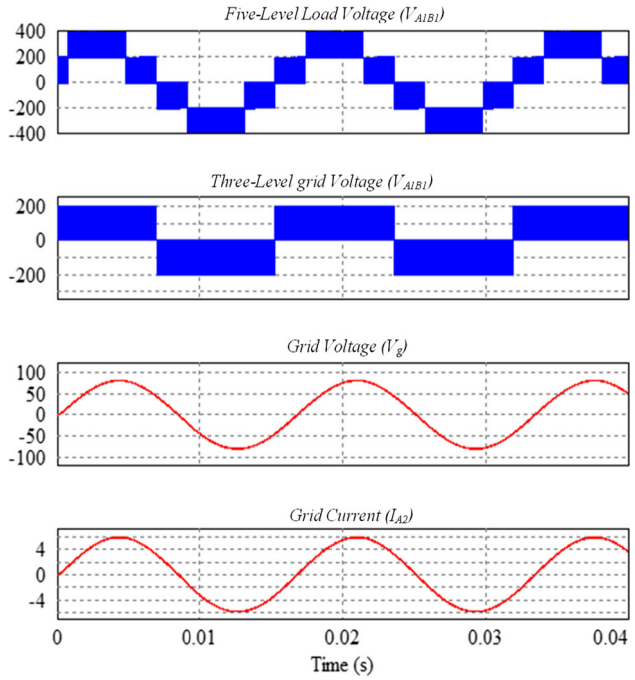


Fig. 11 Simulation result of the proposed inverter under unity power factor

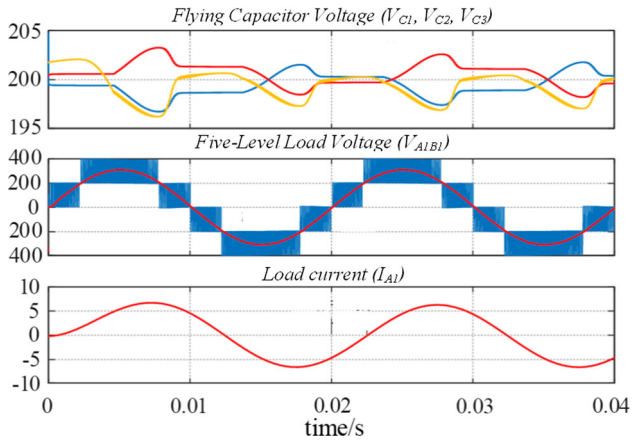


Fig. 12 Simulation result of the proposed inverter under 0.707 inductive load

reduced to 300 W/m^2 and the output power is reduced to 600 W. The figure clearly shows that the decrease in solar irradiance decreases the performance of the PV modules. Thus, varying solar irradiance has a significant effect on the output power generated, however, the effect on the output voltage is very small and can be ignored.

6.2 Experimental Validation

To verify the feasibility of the proposed topology experimentally, a prototype was built to test the steady-state performance and the parameters are listed in Table 3. The

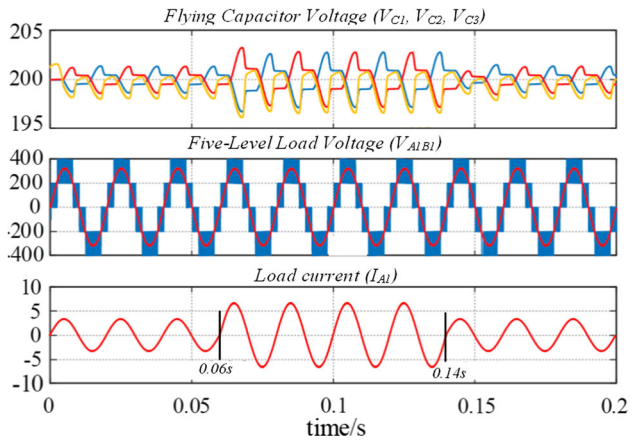


Fig. 13 Simulation result of the dynamic response under different load

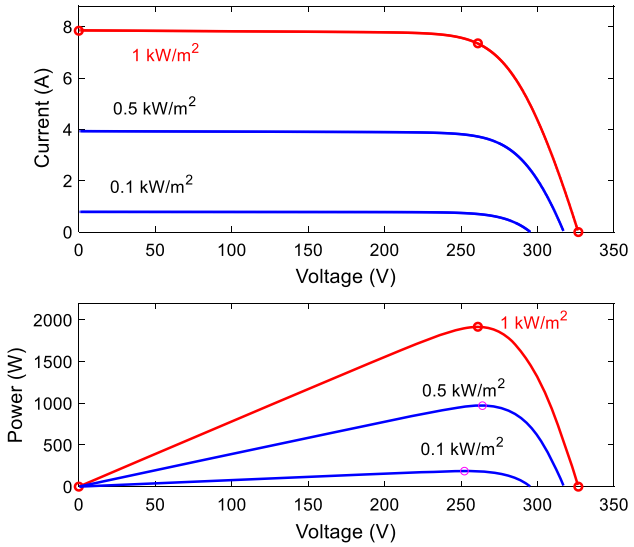


Fig. 14 PV module characteristic for varying irradiances

2-kW prototype was created using a single phase silicon carbide devices (TPH3006PD) from Cree as shown in Fig. 16. The test set up is shown in Fig. 17 where the units are connected together to form a three phase inverter. The parameters, devices, and PCB layout of the three circuits were identical. The flying capacitors C_1, in Fig. 3 are 5 μF multilayer ceramic capacitors. The input voltage was set at 200 VDC. The grid inductance L_g was 200 μH, the filter capacitance was 2 μF, the load was selected as $L_L = 200$ μH and $R = 57$ Ω, respectfully. The modulation index was $m_{A1} = m_{A2} = 0.8$, and the switching frequency was 150 kHz. A TMS320F2812 digital signal processor provided the stimulus to the gate drivers, and the voltage/current waveforms were measured using an oscilloscope Tektronix TPS2012.

The prototype was tested at rated power using the SPWM with the condition that the output power was equal for the two output ports. Figure 18 shows the measured line-to-line five-level output voltage (V_{A1B1}) in channel 1 (blue), the dc-link

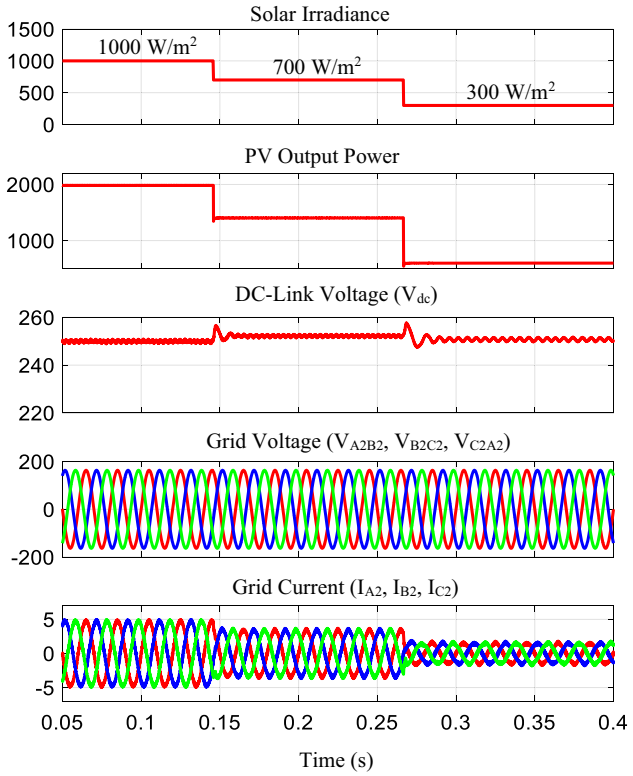


Fig. 15 Simulation results under variable irradiance condition

Table 3 Parameters of the prototype

Parameters	Symbols	Value
Power rating	P	2 kVA
Input voltage	V_{dc}	200 V
DC-link capacitor	C_{dc}	940 µF, 450 V
Flying capacitor	C_1	5 µF
Load	L_L, R_L	200 µH, 57 Ω
Filter inductor	L_g	200 µH
Filter capacitor	C_F	2 µF
Switching frequency	f_s	150 kHz
Switches	$S_{1A} - S_{6A}$	TPH3006PD

voltage (V_{dc}) in channel 2, the grid voltage (V_g) in channel 3 (purple), and the grid current (i_{A2}) in channel 4. It can be noticed that the five-level output voltage is generated, and the grid voltage is synchronized with the phase current, hence unity power factor is achieved. It can be seen that that V_{dc} is 200 V, the magnitude value of grid voltage is 120 Vrms, and the magnitude of the grid rms current is 4.8 A, and the delivered power to the utility is about 1 kW. As the voltage of the input dc source was 200 V, a boost gain multiplier of two was achieved. Compared to the five-level conventional topologies, the proposed inverter can generate five-level inverter voltage step of 200 V and a maximum output voltage of *400 V* with fewer number of switching devices, and better DC voltage utilization.

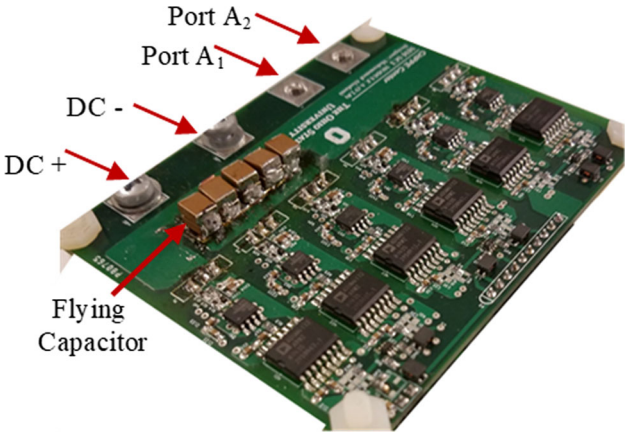


Fig. 16 single phase unit

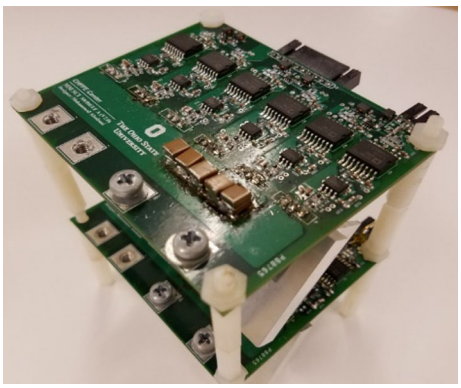


Fig. 17 Test setup: three-phase, three-port, five-level inverter

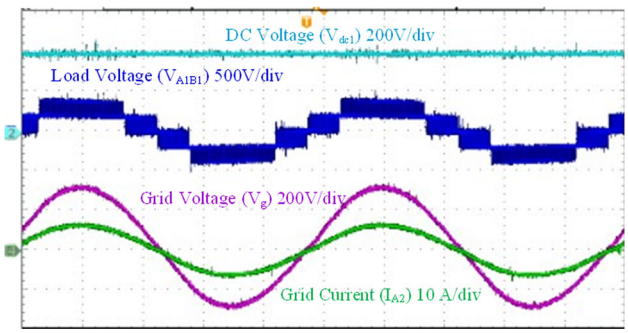
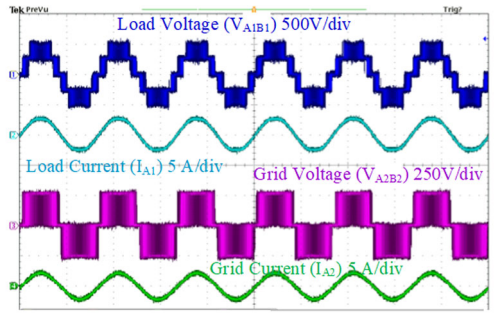
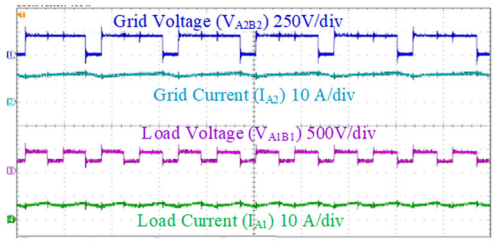


Fig. 18 Experimental results when grid-port under unity power factor

Figure 19a shows the measured three-level line-to-line output voltage at grid side (V_{A2B2}), the phase current at grid side (I_{B1}), five-level line-to-line output voltage at load side (V_{A1B1}), and the phase current at load side (I_{A1}). It can be seen that the five-level voltage of the load V_{A1B1} and the

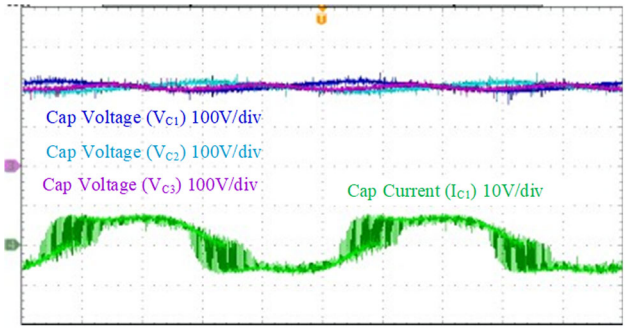


(a) Experimental results for five-level and three-level output waveforms

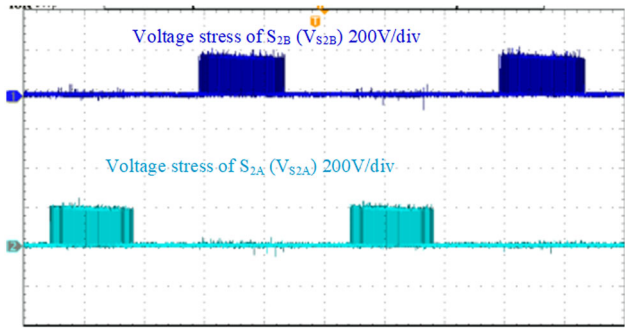


(b) Experimental results, zoomed-in picture for five-level and three-level output waveforms

Fig. 19 **a** Experimental results for five-level and three-level output waveforms. **b** Experimental results, zoomed-in picture for five-level and three-level output waveforms



(a) Experimental results for dc-link voltage, FC voltages and current flowing into capacitor C_1.



(b) Experimental results for voltage stresses of switches S_{2A} and S_{2B}

Fig. 20 **a** Experimental results for dc-link voltage, FC voltages and current flowing into capacitor C_1. **b** Experimental results for voltage stresses of switches S_{2A} and S_{2B}

three-level voltage of the grid V_{A2B2}. The measured RMS voltage were *120 Vrms* and *240 Vrms*, respectfully, and RMS phase currents were 4.8 A and 2.4 A, respectively. In this testing condition, the modulation index was fixed at *0.8* and the peak switching frequency was 150 kHZ. Figure 19b shows the zoomed-in view of Fig. 19a. It can be seen clearly that the time/div is 10 us, therefore, the system is operating at very high switching frequency about *150 kHz*. Hence, the significant reduction in flying capacitors size and the output filter requirements is a major achievement of the proposed five-level inverter compared to the conventional five-level topologies. The flying capacitors was chosen 5 μF whereas the output inductance filter was 200 μF. The employment of the silicon carbide devices made an important contribution in the overall converter size reduction.

Figure 20a illustrates the measured flying capacitors voltages in the three phases, V_{C1}, V_{C1}, and V_{C3} and the current flowing into capacitor C_1, i_{C1}. The average voltages for all flying capacitors equal 200 V. It is the same as the input dc voltages, hence, $V_{C1} = V_{C2} = V_{C3} = V_{\mathrm{dc}}$. It can be seen that the peak-to-peak voltage ripples over the flying capacitors is 12 V, about 6% of the average value. As a result, A multilayer ceramic capacitors of about 5 μF was used in the proposed inverter to replace a large size of electrolytic capacitor. Furthermore, the self-balancing of the flying capacitors voltages is another advantage of the proposed inverter when compared to the conventional NPC and FC multilevel inverter. The current flowing into capacitor C_1 is also measured and has an rms value of about 4.16 A. Figure 20b illustrates the voltage stress of switches. The experimental results show the voltage stress for switches S_{2A} and S_{2B} is 200 V. The proposed topology has an even distribution of the voltage stress, and the voltage blocking for all switches are the same and equal to the input dc voltage.

The converter transient response to the change in the load current is tested and the resulted waveforms are depicted in Fig. 21. The load current has step change from half to full load at time t_1 and another step change back to the original value at time t_2. As the current increase, the voltage ripple across the capacitors C_1 and C_2 is increased, but the average voltage is maintained at 200 V. The grid current i_{A1}*is* smoothly follow the change in the power, hence, the applied control technique has an excellent transient response performance.

The solar PV emulator from NHR (9200) is used to study the performance of the proposed inverter under different solar irradiance conditions. It is mainly used to evaluate the performance of the MPPT algorithm with built-in control panel to adjust the parameters of PV simulator for different scenarios. The experimental result under variable irradiance condition is shown in Fig. 22. Initially, the solar irradiance is set at 1000 W/m^2, the grid voltage is 120 Vrms, the output load current is 2.4 A and the output grid current is 4.6 A. As shown in channel 4 with green color, a step change of the solar irradiance from 1000 to 0 W/m^2 is emulated. The current for both grid current and load current decreased to zero

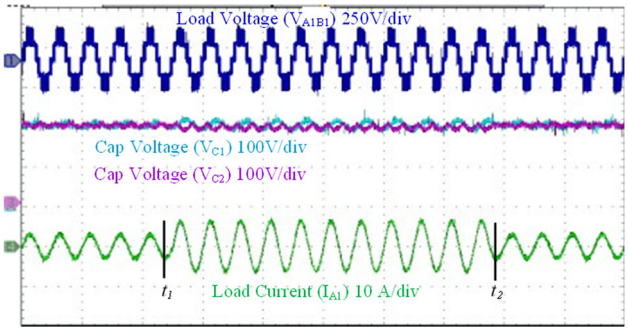


Fig. 21 Experimental results under transient response with step change in the load

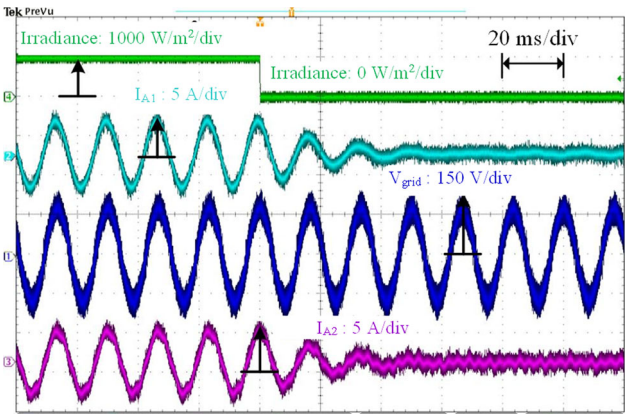


Fig. 22 Experimental results under variable irradiance condition

at the same time, hence, the load current and the grid current tracked the control reference from the MPPT control algorithm. The experimental result verifies the functionality of the system under different solar irradiance conditions.

The measured efficiency is plotted in Fig. 23. The efficiency test was carried out with the condition that the output power was equal for the two ports. The measured output power ranges from 100 to 2000 W. It is divided equally between the two-output port, for example, when measuring 200 W, the load port is 100 W and the grid port is 100 W. For this condition, a peak efficiency of 96.3% was achieved at 100 W. The efficiency curve in Fig. 23 takes this shape because the switching losses are dominant when low power is derived. This is because the rms value of the output current is very small, hence a small current flow through the power devices resulting in small conduction losses. However, when high power is derived, the conduction losses become dominant. The switching losses kept the same, and with high current flow through power devices, the conduction losses become dominant, hence, the efficiency curve starts decreases. Moreover, using the fast speed of silicon carbide devices, the circuit benefited from the created stray inductance to achieve soft switching and further improvement in the efficiency performance is achieved. The efficiency is about 3% higher than the efficiency of the conventional topology in [12] which was obtained at 93.3%. The main reason is that six extra power switching devices are involved in the conventional topology, which generate higher conduction losses.

7 Conclusion

Topology based on a three-phase, three-port, five-level switched capacitor is presented in this paper. The converter operation principles and control strategy under unity power factor were analyzed and presented. The circuit employs silicon carbide devices to increase the efficiency and improve the performance of the system. The prototype was fabricated to operate in 240 V/120 V VAC, and the DC bus was set to 200 VDC. The experimental results show that a peak conversion efficiency of 96.3% was achieved. Contrary to the conventional five-level inverter, the proposed topology has single stage power converter with boosting functionality and employs 25% less switching devices. Furthermore, the employed flying capacitors in the proposed topology are 50% less with self-balancing capability. The topology utilized the switched capacitor unit in the front-end stage to replace the traditional DC–DC converter; therefore, the large inductor

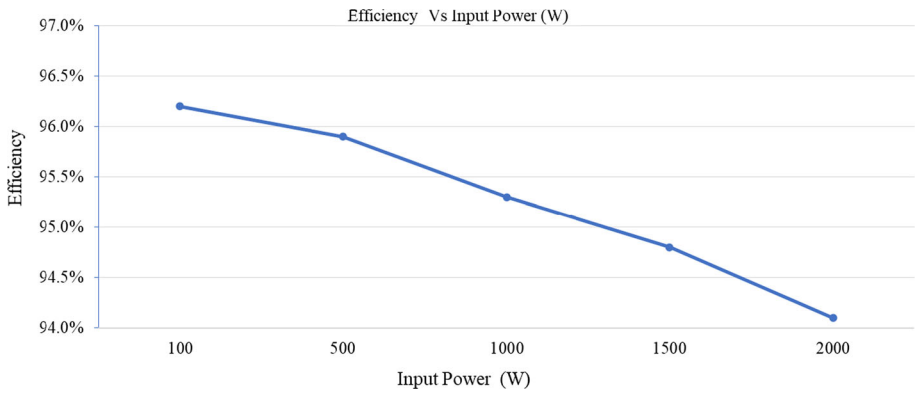


Fig. 23 Measured efficiency curve of the proposed inverter

could be removed, replacing with small capacitors. The backend H-bridge inverter generates five voltage levels without clamping diodes or flying capacitors. Moreover, using silicon carbide devices enabled the converter to run at high switching frequency (150 kHz). Hence, a very small multilayer ceramic capacitors of about 5 μF were used, and very small size output filter with values 200 μH and 1.2 μF can be realized. As a result, a very small voltage ripples of about 6% is obtained. Such a reduction in converter size cannot be achieved without using the silicon-carbide devices. The proposed inverter can be used on the grid-connected PV system, and the application also can be extended to the off-line PV system such as houses, traction and pumps.

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