An Efficient Inverter Logic in Quantum-Dot Cellular Automata for Emerging Nanocircuits

Mrinal Goswami[1,2] · Mayukh Roychoudhury[1] · Joydeb Sarkar[1] · Bibhash Sen[1] · Biplab K. Sikdar[3]

Abstract

Quantum-dot cellular automata (QCA) has been advocated as one of the most propitious nanoelectronic technologies. The fault rates in QCA are very high due to its susceptibility to cell deposition defects. Also, the power requirements of QCA are getting more critical to avoid either over-design for power rails or unreliability under high-performance stress. Among the different primitive logic structure of QCA, the inverter is keyed out to enable more reliable as well as low-power design. This work proposes a novel approach to generate stimulus for low-power dissipation in QCA logic primitives (inverter) in order to obtain worst-case power scenarios. Hybridizing rotated and non-rotated QCA cell together with a new low-power inverter tile structure in QCA is proposed. Further, the functional characterization of the proposed inverter tile is investigated. Kink energy estimation, as well as simulation results, is considered for verifying the circuit layout and functionality. Moreover, a composable logic block is synthesized that realizes triple fanout (with two inverted output). The reliability of these logic primitives is also extended by implementing full adder and XOR circuit.

Keywords Nanoelectronics · Quantum-dot cellular automata (QCA) · Inverter · QCA defects · Fault tolerance · Power dissipation

1 Introduction

Downscaling of current CMOS devices beyond a certain limit is not feasible as it introduces an anomalous quantum behavior in nanoscale level. Several emerging technologies such as carbon nanotubes, silicon nanowires, quantum-dot cellular automata, single-electron transistors emerge as a possible replacement of current CMOS. Quantum-dot cellular automata (QCA) is one of them, and it promises higher circuit densities, faster speeds, low power consumption over the traditional CMOS technology [1]. The design capability of QCA circuit for general-purpose computing is reported in [2–7]. The 3-input majority voter is the basic unit of QCA circuits. However, the 3-input majority voter is functionally incomplete without an inverter logic to synthesize all types of Boolean logic. Fanout is another important part of implementing logically significant QCA arrays providing signal splitting [8].

On the other hand, circuit reliability is another important design issue that needs to be considered for advanced logic circuits [9]. According to [10], the huge complexity of nanoarchitectures ensures the requirement of high fault tolerance. Fabrication defect, room temperature realization and how to fix the input state as well as the output state is measured are the three most demanding issues that need to be addressed to exploit the full potential of QCA circuits [11]. Increasing the fault tolerance capability of a QCA logic

✉ Mrinal Goswami
  mgoswami@ddn.upes.ac.in

  Mayukh Roychoudhury
  mayukhr@ymail.com

  Joydeb Sarkar
  jksarkar007@gmail.com

  Bibhash Sen
  bibhash.sen@cse.nitdgp.ac.in

  Biplab K. Sikdar
  biplab@cs.iiestcs.ac.in

1   Department of Computer Science and Engineering, National Institute of Technology, Durgapur, West Bengal 713209, India

2   Department of Systemics, School of Computer Science, University of Petroleum and Energy Studies, Dehradun 248007, India

3   Department of Computer Science and Technology, Indian Institute of Engineering Science and Technology, Shibpur, West Bengal 711103, India

circuit has become the utmost necessity besides solving the critical manufacturing issues.

Majority voter and inverter are the two basic primitives found in QCA. Various attempts have been done to realize fault-tolerant majority logic [12–18], NNI (Nand-Nor-Inverter) [19,20], fanout and wires [21], I/O Interface [22]. Coplanar and multilayer wire crossings are also investigated in QCA. However, low robustness and fabrication issues leave them challenging [23]. Each existing method to tackle the wire crossing problem has its own problems. The 3×3 grid-based method has been recognized in [12] to construct versatile logic and interconnection functions. However, very little research reports are presented on the fault-tolerant design of inverter [24,25], which motivates us to focus on it. The main contributions of this paper are as follows:

- The most compact inverter structure based on 2×2 QCA tile is realized.
- Kink energy estimation of the proposed inverter has investigated to showcase its robustness.
- Functional characteristics highlighting the robustness of the inverter is examined.
- Analysis of power dissipation of the proposed inverter indicates its low-power feature.
- A new composable block realizing fanout and inverter simultaneously is synthesized.
- Finally, a complex logic circuit using proposed inverter is also synthesized.

Note that fault tolerance issue has been so far analyzed as an implementation technology point of view. However, in this paper, we investigate the issue of fault tolerance from an architectural point of view. Our approach is based on the following conjecture. Assuming that there is a certain amount of irregularity present in the assembly of the QCA cells as well as missing cells, it is possible to design QCA circuits that still perform the desired operations despite their faults. Considering these facts, we have been pursuing this direction as a technique for enabling fault-tolerant QCA logic gates and circuits. In this paper, we present the design of novel QCA logic gates that offer remarkable robustness with respect to input and output misalignment, irregularity in cells assembly, and missing cells. The fault-tolerant properties of inverter tiles, subject to these defects, are evaluated through kink energy estimation as well as simulation with QCADesigner [26].

The rest of the paper is distributed as follows. In Sect. 4, the proposed design of inverter is explored, including characterization of inverters. A proper characterization of composable block implementing fanout and inverter is reported in Sect. 5. Section 6 investigates the power dissipation of the proposed inverter. Section 7 explores the design of fault-tolerant adder and XOR. Section 9 concludes the paper.
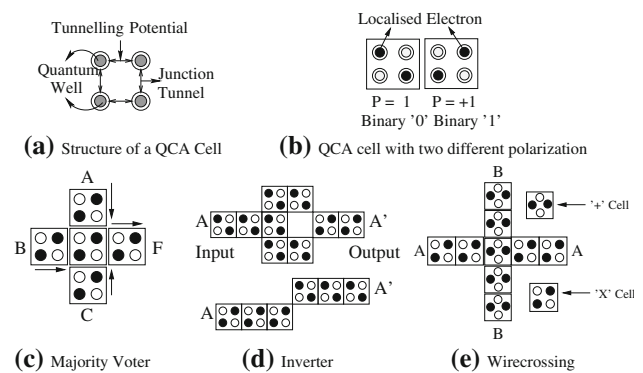
Fig. 1 QCA logic primitives

(a) Structure of a QCA Cell (b) QCA cell with two different polarization (c) Majority Voter (d) Inverter (e) Wirecrossing

2 QCA Basics

A basic QCA cell (Fig. 1a) is square-shaped and has four quantum dots placed at four corners. There are two free electrons that can move between these dots via tunneling [27]. Due to the coulombic repulsive force, both electrons will always occupy the opposite corners as it creates the largest possible distance between the electrons. Based on the position of the electrons, a bi-state device with a logic 0 ($P = -1$) and logic 1 ($P = +1$) can be formed (Fig. 1b).

The 3-input majority voter (Fig. 1c) is the basic building block for all QCA circuits. Its output follows the majority of the polarization of the input cells. The logic generated by a 3-input majority voter can be represented as M(A,B,C) = AB + BC + CA. By applying fixed polarization at one of the input cells as $P = +1$ or $P = -1$, the majority voter can function as an AND or OR gate, respectively. There are two different ways to implement NOT gate in QCA (Fig. 1d).

In QCA, information propagates through the wire. QCA consists of two types of wire, namely 90° (X-cell) wire and 45° ($+ -$ cell) wire (Fig. 1e). In a 90° wire, the coulombic repulsive force between electrons ensures adjacent cells to have the same polarization. Input polarization is fixed at one end and is carried throughout the whole length of the wire. On the other hand, a 45° wire consists of cells that are rotated at an angle of 45°. The polarized state of a cell in a 45° wire is always the opposite state of the adjacent cell. QCA accommodates two types of wire crossing, coplanar and multilayer. Coplanar wire crossing can be done in a single layer with the help of both 90° and 45° QCA wire, as shown in Fig. 1e. Coplanar wire crossing is based on the observation that when these two types of wire cross each other, they do not have any interaction between them [27,28]. On the other hand, the multilayer wire crossing uses more than two different layers.
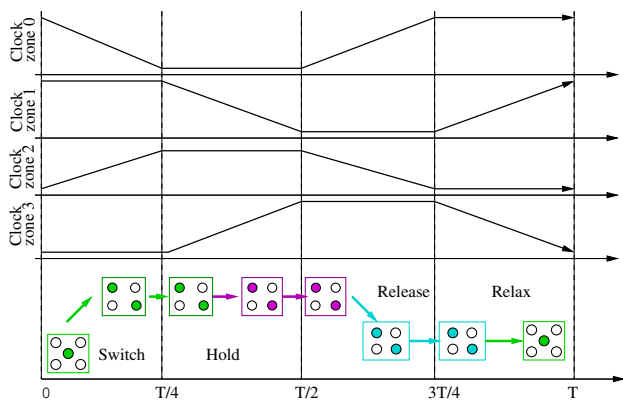
Fig. 2 QCA clocking

2.1 QCA Clocking

In QCA, timing is decided by clocks. QCA clocking has four periodic phases with a $\Pi/2$ phase difference between contiguous phases [27,29]. Clocking divides a QCA circuit into zones where each zone has a specific clock phase. All the cells inside a specific zone are in the same phase. Clock ensures that cells within a particular clock zone are frozen into a specific polarized state when cells in adjacent zones are changing. QCA clock can be used to synchronize the circuit, making sure all the input signals reaches a particular logic gate at the same time.

There are four different phases in a QCA clock (Fig. 2): switch, hold, release, relax. In the beginning, QCA cells are unpolarized, and their inter-dot potential barrier is low. The barrier is raised during the switch phase, and the cells get the polarization according to the input value. In the hold phase, barriers are kept high so that the polarization can be used as input for the next cell. The barriers are lowered in the release phase, and cells become unpolarized again. At last, in the relax phase, cells remain in the relaxed unpolarized state. To pass information, the sender must be in hold state, whereas the receiver must be in switch state.

If the input of a QCA circuit is switched suddenly, then the QCA wire could go into some combination of opposite polarization. This incident creates a significant delay in the system when it is trying to reach its ground state, thus making the overall system slower. To prevent this incident, adiabatic switching is applied in QCA circuits. However, in adiabatic switching, changes in operating temperature, as well as the longest length of a QCA wire within the same clock zone, can have an adverse effect [27].

2.2 QCA Defects

The main reason behind high fault rates in QCA is due to various types of deposition defects found in the literature

[30]. Defects in QCA may occur during the synthesis as well as while positioning of QCA cells [31]. Referable to smaller geometries of QCA cells and the very high accuracy required in the arrangement of these cells, defects could be more probable to take place during the deposition phase [31]. The various cell deposition defects (missing cell defects, cell displacement defect, cell misalignment defect, extra cell defect, and cell rotation defect) found in the fabrication process are shown in Fig. 3.

Here, the deposition defects are discussed one by one with the help of a 3-input majority gate. The Boolean representation of a 3-input majority gate is $MV(P, Q, R) = PQ + QR + RP$. A 3-input majority voter can also suffer from faulty fabrication process and produce erroneous output. Different types of defects that can occur to a 3-input majority voter are discussed below.

(1) *Missing cell defect* A missing cell defect can take place at any of the three inputs, at the middle cell and also at the output cell (Fig. 3b). If one of the inputs is omitted, the output gets heavily influenced by one of its remaining input. The incorrect behavior is similar to "stuck-at-fault" found in CMOS design where the output value is indistinguishable from one of its input values. If cell omission happens at the middle cell, then the output also becomes inaccurate.

(2) *Cell displacement defect* Due to the minuscule size of the QCA cells, chances of cell displacement errors are quite high (Fig. 3c, d). Any of the 3 inputs may be wrongly displaced from its original position. Depending on the amount of displacement, the obtained output can be erroneous.

(3) *Extra cell deposition defect* One or more extra cells are wrongly deposited along the boundary of the majority voter producing faulty output (Fig. 3e).

(4) *Cell rotation defect* A QCA cell is wrongly rotated and has a different orientation than its neighbors (Fig. 3f). For example, if the middle cell is wrongly rotated 45°, the majority voter acts as if the middle cell is missing, resulting in erroneous output.

3 Related Work

Single-electron fault for QCA inverter to handle space radiation effect has been investigated in [34]. Testa et al. investigated inverter propagation for majority-based synthesis to synthesize inversion-free networks [35]. In [36], a ternary QCA inverter gate is investigated. Primitively, inverter logic (Inverter 1) is realized by splitting and joining two parallel wire from input to output (Fig. 4a). Inverter chain (Inverter 2) is also a dominant representation of the inverter using the inverter chain by placing cells diagonally to each
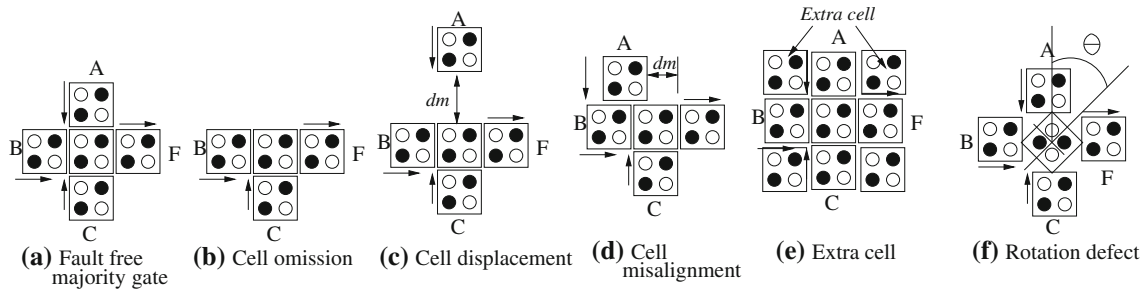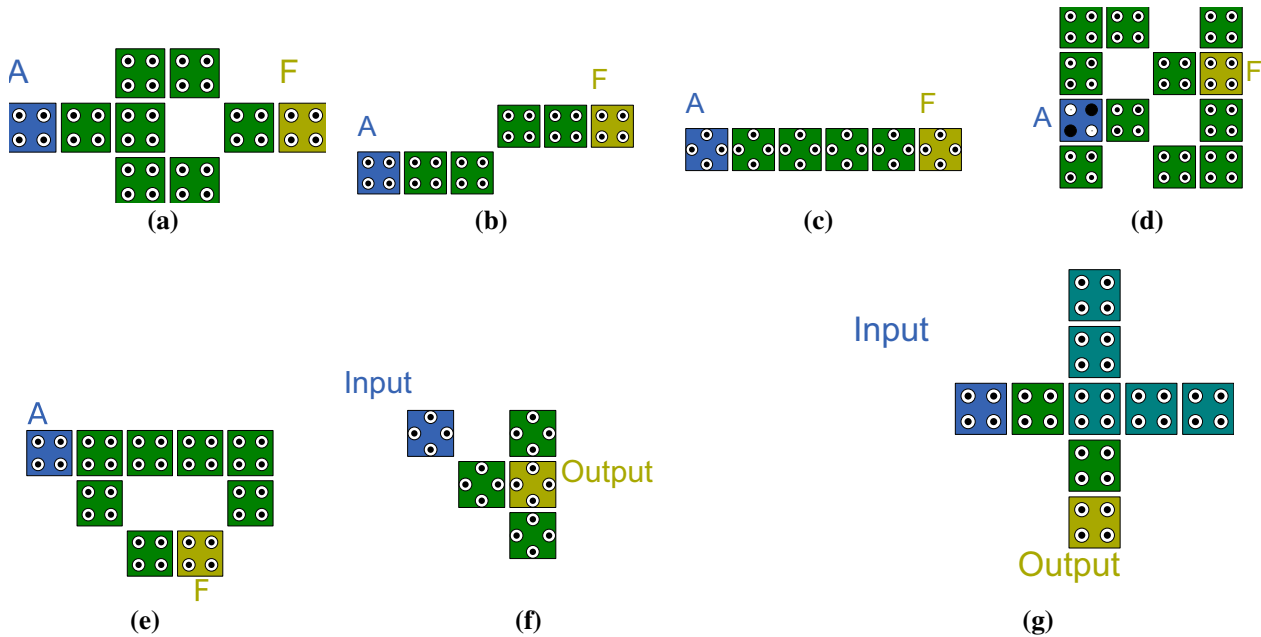
Fig. 3 QCA defects

Fig. 4 Existing QCA **a** Inverter 1 [28], **b** Inverter 2 [28], **c** Inverter 3 [28], **d** Inverter 4 [24], **e** Inverter 5 [25], **f** Inverter 7 [32], **g** Inverter 8 [33]

other. Standard cells in a diagonal orientation (Inverter 3) tend to align in opposite directions of polarization as in the inverter chain (Fig. 4c). In [24], Beard established a fault-tolerant not gate (Inverter 4) with non-fully populated 4 × 4 tiles (Fig. 4d) which requires 8104.36 nm². Kumar et al. proposed a new design of fault-tolerant inverter design (Inverter 5) as shown in Fig. 4e [25]. In [32], a highly polarized inverter design is investigated as shown in Fig. 4f. Even though the proposed design is highly polarized, it is not possible to connect the QCA circuit with a normal cell. Recently, Kalogeiton et al. [33] proposed a novel design of inverter utilizing different clock zone, as shown in Fig. 4g. However, it possesses limited fault tolerance.

4 Proposed Fault-Tolerant Inverter Design

In this section, a new alternative 2 × 2 tile structure is proposed to optimize the structural complexity of the inverter

logic (Fig. 5a). It uses only 4 rotated cells with standard (non-rotated) input and output cell covering 4384.38 nm². Fabrication complexity of the rotated cell is same as normal cell [37,38]. In coplanar wire crossing, the rotated and normal cells are placed together without interfering the inputs to each other [23,28].

The kink energy of output cell (F1) is calculated to verify the functional correctness of the proposed inverter. Initially, the position of electrons is identified in the output cell by considering the electrostatic energies at a different position of the driver cells and the input cells. For every input combination, electron's position, which possesses the least energy, is included for the target position.

The state energy is calculated using electrostatic energy between each cell and their adjacent cell. The electrostatic energy between the quantum dots in cell i and j is calculated as shown in Eq. 1 [39].

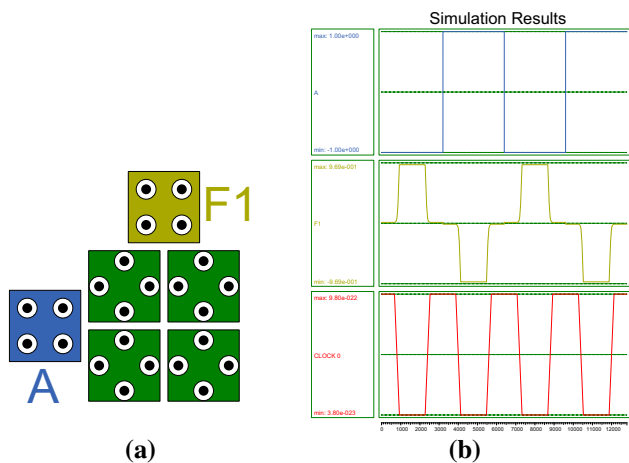$$E_{i,j} = \frac{q_i q_j}{4\pi \varepsilon_o \varepsilon_r |r_{i,j}|} \tag{1}$$

Fig. 5 **a** Proposed fault-tolerant inverter 6 and its **b** simulation result
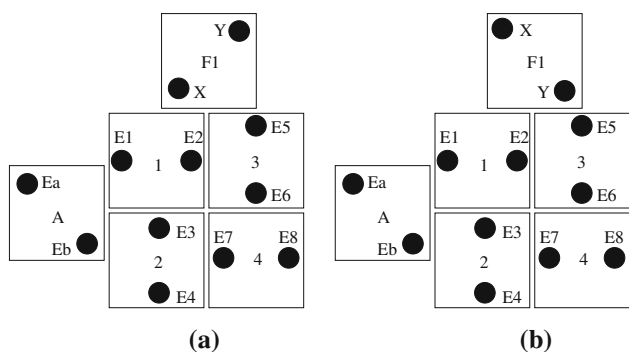
Fig. 6 Cell position of inverter for **a** case A, **b** case B

Table 1 Estimation of kink energy at F1 under different polarization

Electron x	Electron y
Case A	
$U_A = 0.713 \times 10^{-20}$	$U_A = 0.475 \times 10^{-20}$
$U_B = 0.713 \times 10^{-20}$	$U_B = 0.475 \times 10^{-20}$
$U_1 = 1.55 \times 10^{-20}$	$U_1 = 0.571 \times 10^{-20}$
$U_2 = 1.69 \times 10^{-20}$	$U_2 = 0.751 \times 10^{-20}$
$U_3 = 1.04 \times 10^{-20}$	$U_3 = 0.525 \times 10^{-20}$
$U_4 = 0.575 \times 10^{-20}$	$U_4 = 0.379 \times 10^{-20}$
$U_5 = 1.27 \times 10^{-20}$	$U_5 = 1.15 \times 10^{-20}$
$U_6 = 0.856 \times 10^{-20}$	$U_6 = 0.606 \times 10^{-20}$
$U_7 = 0.707 \times 10^{-20}$	$U_7 = 0.464 \times 10^{-20}$
$U_8 = 0.515 \times 10^{-20}$	$U_8 = 0.460 \times 10^{-20}$
$U_T = 15.485 \times 10^{-20}(J)$	
Case B	
$U_A = 0.543 \times 10^{-20}$	$U_A = 0.465 \times 10^{-20}$
$U_B = 0.465 \times 10^{-20}$	$U_B = 0.543 \times 10^{-20}$
$U_1 = 0.751 \times 10^{-20}$	$U_1 = 0.765 \times 10^{-20}$
$U_2 = 0.765 \times 10^{-20}$	$U_2 = 1.55 \times 10^{-20}$
$U_3 = 0.575 \times 10^{-20}$	$U_3 = 0.810 \times 10^{-20}$
$U_4 = 0.397 \times 10^{-20}$	$U_4 = 0.525 \times 10^{-20}$
$U_5 = 0.835 \times 10^{-20}$	$U_5 = 10.331 \times 10^{-20}$
$U_6 = 0.542 \times 10^{-20}$	$U_6 = 1.15 \times 10^{-20}$
$U_7 = 0.460 \times 10^{-20}$	$U_7 = 0.719 \times 10^{-20}$
$U_8 = 0.408 \times 10^{-20}$	$U_8 = 0.707 \times 10^{-20}$
$U_T = 23.306 \times 10^{-20}(J)$	

where ε_0 is the permittivity of free space and ε_r is the relative permittivity of the material of the quantum cell. q_i and q_j are the electron dots charges at i and j, respectively. The distance between the two dots is calculated as $r_{i,j} = |r_i - r_j|$. The above equation calculates electrostatic energy of the electrons inside device cells that are faulty for different inputs.

The quantum dots on the input cell are marked with E_a to E_b and the driver calls are marked from E_1 to E_8. Figure 6 shows the quantum dots of the output cell that are marked as x and y. Electrostatic energy at position $\times$ due to electron at position E_A in cell 'A' is k_{eq}/r_a, where r_{ax} is the distance between E_a and x. Similarly electrostatic energy is calculated at position $\times$ due to electron position at E_b and E_1 to E_8. Total electrostatic energy at the position $\times$ (denoted as U_x) is shown below:

For test case A,

$$U_A = \frac{k_{eq}}{r_{ax}} + \frac{k_{eq}}{r_{bx}} = 0.713 \times 10^{-20} j \qquad (2)$$

where $k_{eq} = q^2/4\pi\varepsilon_o\varepsilon_r = 23.04 \times 10^{-20}$

Likewise, electrostatic energy at position y is calculated as indicated in Table 1.

Two cases are considered here: case A: Assume the polarization of the output cell F1 as +1 as shown in Fig. 6a and compute the kink energy of the x and y electrons of the output cell F1. Case B: The output cell F1 to be in -1 polarization as shown in Fig. 6b is considered. Table 1 presents the kink energy of both the cases. It can be concluded from the above observation that case (A) has lower kink energy thus providing more stability. Hence, the complementary nature of the proposed tile is proved.

4.1 Fault Tolerance of Inverter

The fault tolerance of the inverter tile has been evaluated by performing an exhaustive simulation with up to 2 cells that are not deposited having a yield level greater than 50%. When the missing cell defect occurs in the inverter tile, then the result must be found among three functions that are a wire (output=input), an inverter (output=$\overline{input}$) and an undefined state. The analysis of the missing cell (undeposited cell) defect of all 8 types of inverter tiles is reported in Table 2.

Table 2 Characterization of inverter tiles with multiple undeposited cell

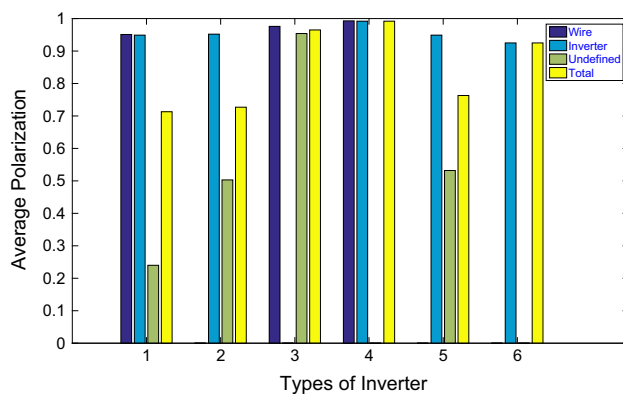| Type of inverter	INV 1 [28]		INV 2 [28]		INV 3 [28]		INV 4 [24]		INV 5 [25]		INV 6 [Proposed]		INV 7 [32]		INV 8 [33]	
Undeposited cell	1	2	1	2	1	2	1	2	1	2	1	2	1	2	1	2
Defective patterns	7	21	4	6	4	6	10	45	7	21	4	6	3	3	7	21
Occurrences of wire func.	1	9	0	2	3	0	1	7	0	7	0	1	1	1	0	0
Wire func. percentages (%)	14.2	42.8	0	33.3	75	0	10	16	0	33.3	0	16.6	33.3	33.3	0	0
Occurrence of INV func.	5	6	3	1	0	3	9	38	6	11	4	4	2	2	6	15
INV func. percentages (%)	71.4	28.6	75	16	0	50	90	84	85.71	52.3	100	66.6	66.6	66.6	86	71
Occurrence of undefined	1	6	1	3	1	3	0	0	1	3	0	1	0	0	1	6
Undefined state percentage (%)	14.2	28.6	25	50	25	50	0	0	14.2	14.2	0	16.6	0	0	14	28.5

Fig. 7 Average magnitude of max. polarization level of inverter under single missing cell deposition

Table 3 Performance of QCA inverters

| Design	Cell	Area (nm^2)	FT (%)
Inverter 1	9	6844	71.43
Inverter 2	6	6711	75
Inverter 3	6	4351	0
Inverter 4	12	8104	90
Inverter 5	9	5684	88.88
Inverter 7	5	3364	66.67
Inverter 8	9	9604	86
Inverter 6*	4	4384	100

FT Fault tolerance
*Proposed here

Here, only single and double missing cell defect is considered during the evaluation of those functions. For multiple undeposited cells, a wire function or an inverting function (complement of the input) is produced by the tile.

In the case of a single missing cell defect, the average magnitude of the maximum polarization level of the proposed inverter tile is shown in Fig. 7. The proposed inverter (inverter 6) has a fault tolerance of 100% under single-cell deposition, whereas inverter 4 and 7 produces no undefined function. In almost 90% of the cases, the inverter 4 and 6 tiles can still perform as a wire as well as an inverter due to the spatial redundancy, which provides an exceptional level of functionality. The following additional properties can be observed: (i) For an output signal, the probability of being in an undefined state is proportional to the number of cells that are undeposited. However, such a probability is very less in case of inverter 4 and 6. (ii) The probability of having a wire or inverting function is more than undefined function. (iii) Inverter 4 and 6 provides a better inverting function that traditional inverter logic under missing cell deposition. A comparative analysis of the inverters is reported in Table 3 considering the fault tolerance capability under single-cell deposition only. It is evident that the proposed inverter (INV
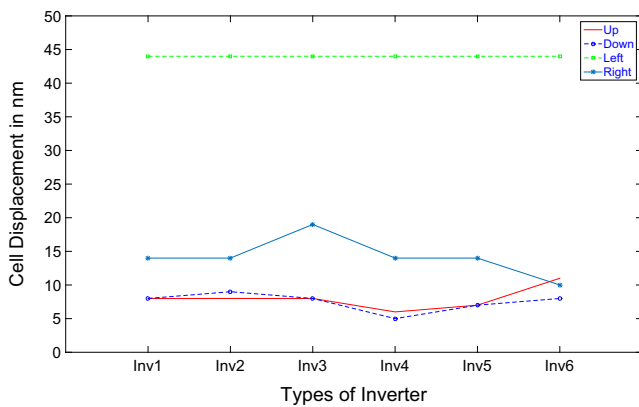
(a) Input cell
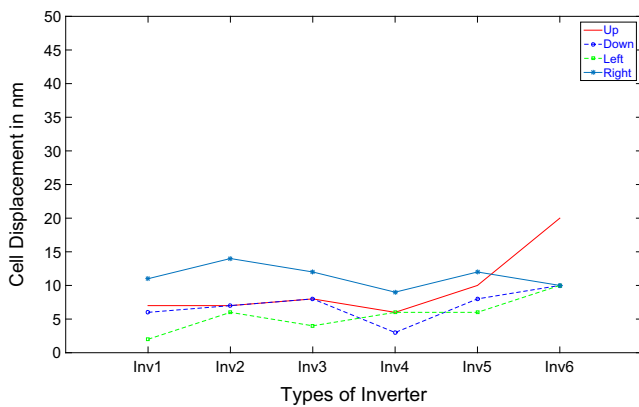
(b) Output cell

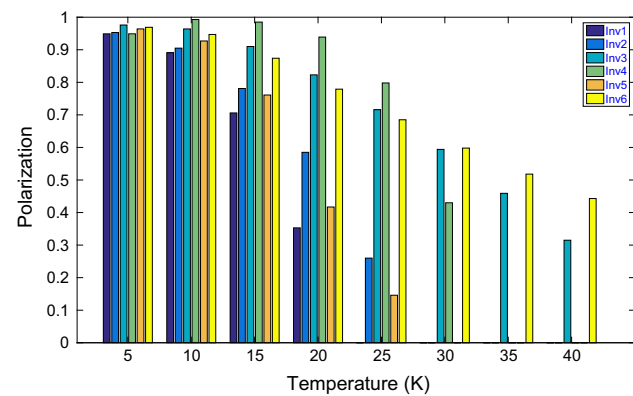**Fig. 8** Maximum displacement tolerance of I/O cell of inverters

**Fig. 9** Average magnitude of maximum polarization level of inverter in different temperatures

Table 4 Fault tolerance (in %) capability of single missing and additional cell defect

Design↓	Single missing cell defect			Single additional cell defect		
	2-bit	3-bit	4-bit	2-bit	3-bit	4-bit
Inverter 1	50	72.22	50	73	76.92	76
Inverter 2	16.66	33.33	41.67	83.33	83.33	83.33
Inverter 3	33.33	54.54	27.27	84.61	75	96.67
Inverter 4	66.66	66	75	56.25	62.50	86.36
Inverter 5	50	67	75	66.66	58	74
Inverter 6*	100	100	100	100	100	100

*Proposed
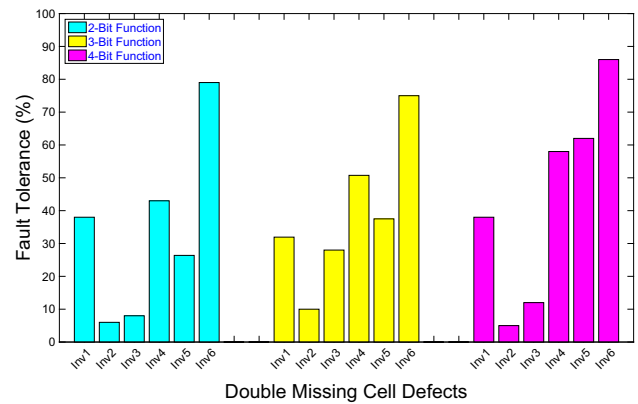
(a) Double missing cell defects

(b) Double additional cell defects

Fig. 10 Double missing and additional cell defects

6) requires a minimum area while providing maximum fault tolerance under single-cell deposition.

The misplaced cells (input/output) may have an adverse effect on the output polarization. Misplacements toward horizontal ('left' and 'right') and vertical ('up' and 'down') directions are considered. The maximum amount of displacements (permissible) of the cells (in both vertical and horizont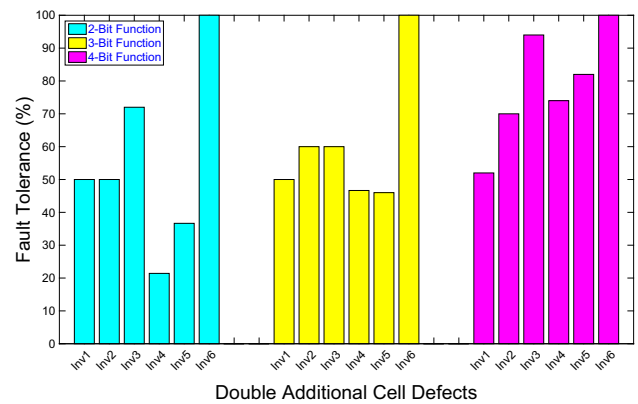al directions) that do not affect the function of the inverter is examined as shown in Fig. 8a and b. It is evident that inverter 6 possesses high fault tolerance to the displacement of the input and output cell comparing other inverters.

Since QCA devices perform their computation using the location of each electron, the question may arise whether they are more vulnerable toward fabrication imperfections and thermal effects. Hence, the performance of the inverters is analyzed under different temperatures, as shown in Fig. 9. It is evident that polarization value decreases with increase in temperature. However, at high temperature where other

inverter fails to produce marginal output polarization, the inverter 6 still provides an inverting function.

5 Fault Tolerance of Multi-bit Boolean Circuits Based on Different Inverters

In this section, attempts are made to investigate the fault-tolerant property of the proposed inverter when it is applied on separate Boolean circuits of varying bits. The results are tabulated, and relationship graphs are realized between the Boolean circuits of different bits. Functions implemented with the inverter gates are XOR ($A \oplus B = AB' + A'B$,) for 2-bit, full adder (sum= $A \oplus B \oplus C$) for 3-bit and controlled

universal function ($D(AB + A'C')$) for 4-bit are considered here for the analysis of the multi-bit circuits.

Table 4 tabulates the fault tolerance patterns of the various inverters used in 2, 3, 4-bit logic circuits. From Table 4 inferences to the efficacy of the proposed inverter can be made as it is 100% fault-tolerant with a comparison to lower fault tolerance values of the other inverters for single missing cell defects.

Likewise, Fig. 10 represents the fault tolerance values of different circuits (2, 3, 4-bit) based on the inverters under double missing and additional cell defect. Y-axis represents the fault tolerance(%), and the 2, 3, 4-bit functions are represented on the x-axis. The proposed inverter arguably has the highest fault tolerance when compared to fault tolerance of other inverter designs.

5.1 Design of New Composable Logic Block with Inverter/Fanout

Here, a new composable logic structure is synthesized, which has three outputs (F1, F2, F3), as shown in Fig. 11a. We will consider only two outputs (F1, F2) because of the function-
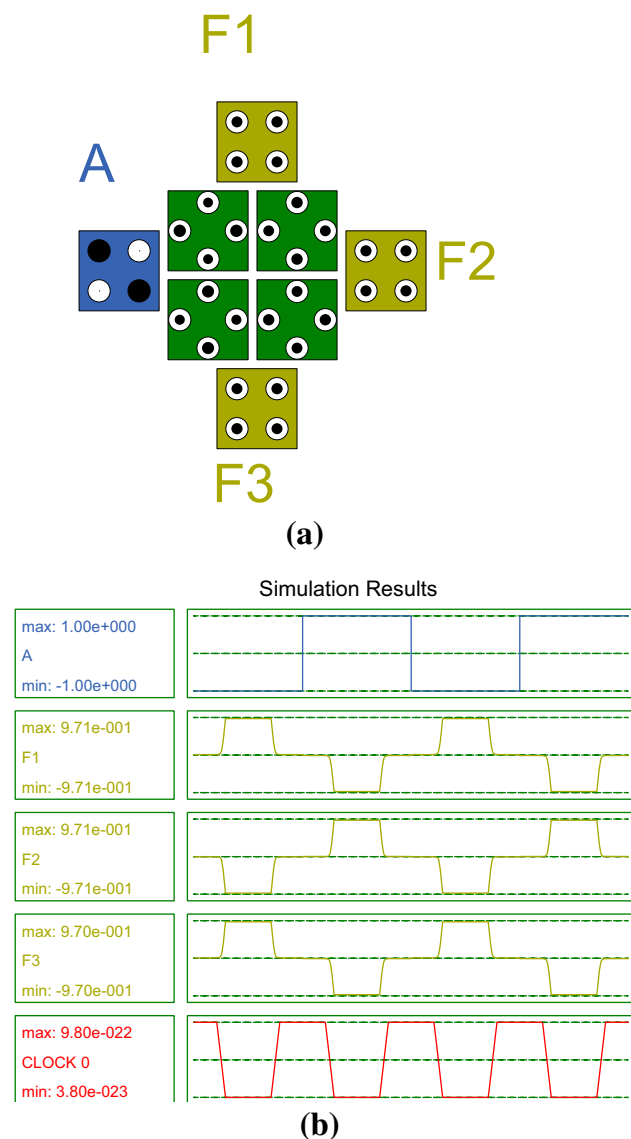

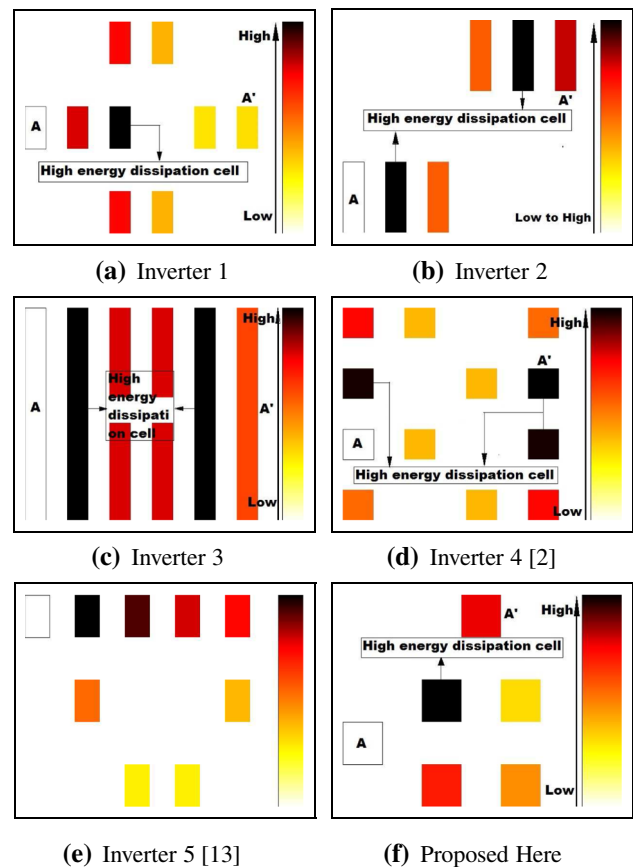**Fig. 11** Proposed **a** Composable block and its, **b** simulation result

Fig. 12 The power dissipation image for inverter gates at 2 K temperature with 0.5 E$_k$

ality. It is not purely fanout because one output is inverted. However, in-circuit level, this inverted output can be converted to non-inverted output by just placing a cell diagonally on it. The specialty of this structure is output is converted to inverter and wire simultaneously. In the proposed structure, two inverted (F1 = F3 = $\overline{A}$) and one wire function (F2 = A) are generated as shown in Fig. 11b.

This is a special kind of composable QCA block where the wire and two inverted fanout is driven out simultaneously. No such QCA logic is found in literature where multiple outputs (fanout + inverter) can be generated together with such robustness, as shown in Fig. 11. Using a single block of Fanout, the synthesis capability of the circuit can be extended further with less complexity, as explained in Sect. 7.

6 Power Dissipation of the Proposed Inverter

In [40,41], a probabilistic model (QCAPro) is proposed to estimate the power dissipation of QCA layouts. Under non-adiabatic switching, the QCAPro tool [40,41] can evaluate the minimum, maximum, and average power dissipation in a QCA structure. Also, it can be applied to verify circuit functionality according to the Bayesian network analysis.

All the inverters are examined for three distinct kink energy levels ($0.5\,E_k$, $1\,E_k$ and $1.5\,E_k$) at 2 K temperature. The total dissipated energy is divided into switching and leakage energies. The total power dissipation figures of presented inverter gates under $0.5\,E_k$ are shown in Fig. 12. The dark color indicates high power dissipation. Evidently, in Fig. 12, the logic/driver cells in existing designs dissipate more power compared to other cells. As a consequence, the most significant reason for increasing power dissipation in QCA circuits is the effect of surrounding cells as well as input cells on the driving cell. However, in the proposed design, the driver cells are in the 2×2 tile, which dissipates less power in con-
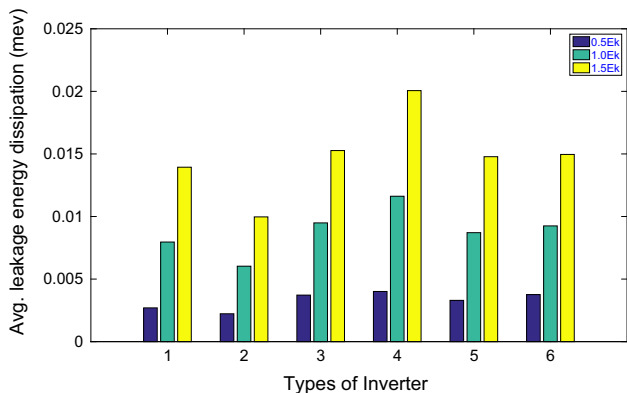
(a) Average leakage energy dissipation
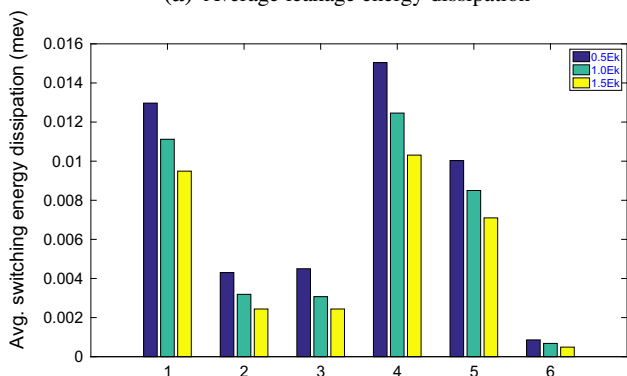
(b) Average switching energy dissipation
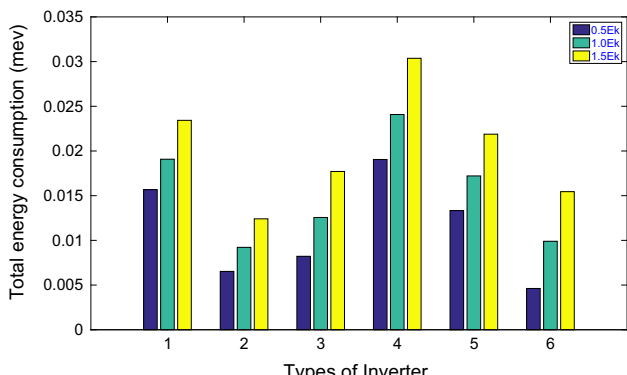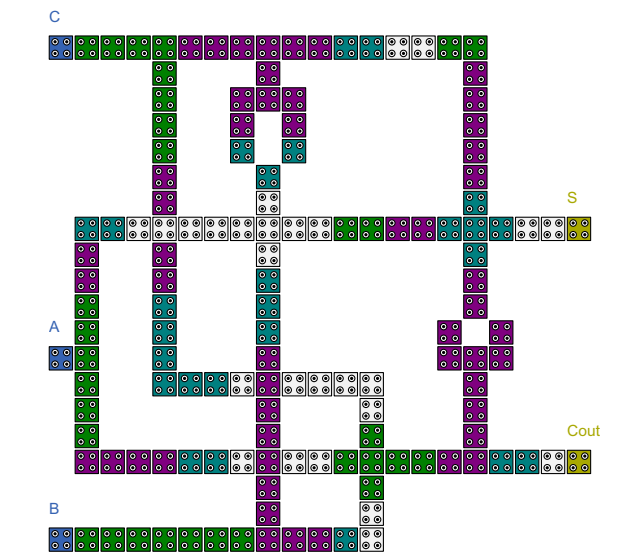
(c) Total energy consumption

Fig. 13 Energy dissipation analysis of different inverters under different kink energy ($T = 2.0\,$K)

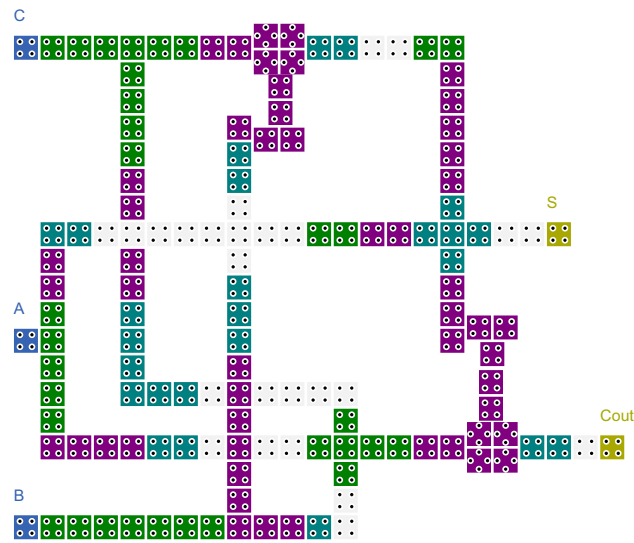**Table 5** Comparative analysis of power dissipation at different Inverters

Kink energy E_k	Type of inverter	Avg. leakage energy dissipation	Avg. switching energy dissipation	Total energy consumption (meV)
0.5	INV 1	0.00270	0.01297	0.01567
	INV 2	0.00223	0.00430	0.00653
	INV 3	0.00372	0.00450	0.00822
	INV 4	0.00401	0.01504	0.01905
	INV 5	0.00330	0.01003	0.01333
	INV 6	0.00376	0.00086	0.00462
1	INV 1	0.00796	0.01112	0.01908
	INV 2	0.00603	0.00319	0.00922
	INV 3	0.00949	0.00307	0.01256
	INV 4	0.01162	0.01246	0.02408
	INV 5	0.00871	0.00850	0.01721
	INV 6	0.00925	0.00068	0.00990
1.5	INV 1	0.01394	0.00949	0.02343
	INV 2	0.00997	0.00244	0.01241
	INV 3	0.01527	0.00244	0.01771
	INV 4	0.02006	0.01031	0.03037
	INV 5	0.01478	0.00710	0.02188
	INV 6	0.01496	0.00049	0.01545

trast to other cells. Hence, regarding the special configuration of input cells in Fig. 12f, we have achieved a consistently reduced power dissipation. Proposed configuration imposes less energy to the driver cell compared to the previous reports.

Based on this Fig. 13b, proposed inverter 6 has a superiority over the presented designs in the literature. Though inverter 2 has the least leakage energy overall input vector pairs in comparison with the other designs (Fig. 13a), fault tolerance is poor. The energy comparison of the six structures is presented in Fig. 13c by calculating the amount of the average leakage and switching energies for different kink energy levels. It is evident that the proposed design (Inverter
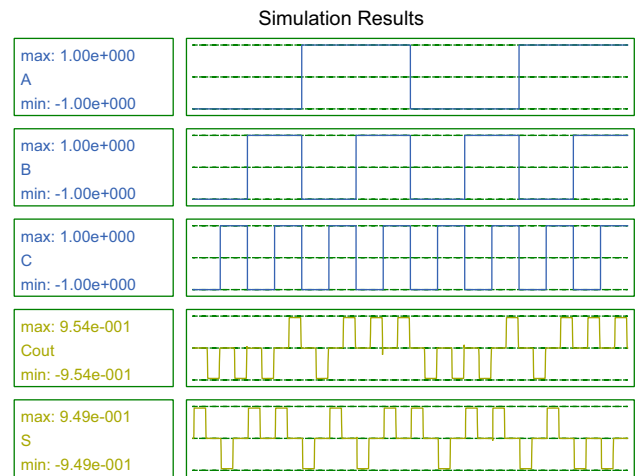

Fig. 15 Simulation result of full adder using inverter 6

6) shows a considerable energy-effective compared to others, as shown in Table 5. Considering these results, inverter 6 represents a low-power inverter which enables architects to implement low-power and large-scale QCA circuits with minimum consumed cells.

7 Design of Fault-Tolerant Combinational Circuit

The fault-tolerant capability of inverter logic is, further, extended to design full adder. The full adder is synthesized using traditional inverter logic, as shown in Fig. 14a. In a similar layout of the full adder, the conventional inverter is replaced with the fault-tolerant inverter 6, as shown in Fig. 14b. The simulation result is shown in Fig. 15. QCADesigner version 2.0.3 [26] simulator is used to confirm the functional correctness of all the proposed designs. We have used bistable approximation and also coherence vector simulation with all the default parameters.

An investigation on fault tolerance capability of the inverter implementing full adder and XOR circuit is reported in Table 6. Here, same full adder and XOR circuit are implemented with the different inverter and then their fault tolerance capability is estimated. It is evident from Table 6 that the introduction of such fault-tolerant inverter boosts the overall performance of the circuit.

8 Discussion

This section will highlight the merits and demerits of the proposed inverter (Inverter 6). Research suggests that the deposition defects are more common than any other faults found in QCA. There are various deposition defects found in

(a) Full adder using conventional inverter 1

(b) Full adder using proposed inverter 6

Fig. 14 Full adders

Table 6 Performance of fault-tolerant inverter implementing adder

Design using	Full adder				XOR			
	INV 1	INV 4	INV 5	INV 6	INV 1	INV 4	INV 5	INV 6
# Cell in inverter	18	24	18	12	9	12	9	6
FT %	72.22	66	67	100	50	66.66	50	100

FT Fault tolerance under single missing cell defect

QCA (discussed in Sect. 2.2). Among all the defects, single missing cell defect is the most discussed fault in QCA due to its high chance of occurrence than any the other deposition defects. The proposed inverter shows 100% fault tolerance (Table 2) in terms of single missing cell defect over all the existing inverters (Fig. 4). However, in terms of the missing double cell, the proposed inverter (inverter 6) shows less tolerance in comparison with inverter 4. Inverters 1, 2, 3, 7, and 8 are realized without considering the issue of fault tolerance, and hence, these designs show limited tolerance to any deposition defects. On the other hand, inverters 4 and 5 have established as a fault-tolerant design. However, both the designs possess low fault tolerance concerning inverter 6 in terms of single missing cell defect. Inverter 7 [32] is a highly polarized design compared to inverter 6, but the fault tolerance capability of the inverter 7 is much less than inverter 6. Moreover, the area overhead of all the existing design is much higher than the proposed inverter. All the inverter (1–7) discussed in this paper requires single clock zone except inverter 8, which requires two clock zones. Power dissipation results established the low-power feature of the proposed inverter. Further, the proposed inverter can serve as a fanout unit, too, which is not found in any of the previous designs.

9 Conclusion

In this paper, a robust inverter logic with the proper characterization of various deposition fault is presented. In the presence of one undeposited cell, the proposed inverter produces correct output. Even in most cases, the proposed inverter can produce a correct output if the tile contains multiple undeposited cells (up to two cells). The proposed 2×2 inverter tile shows 100% fault tolerance in case of single missing cell defect. A new composable logic structure is also synthesized based on the inverter, which reduces the requirement of disparate hardware in the complex logic circuit providing inverted fanout and wire function simultaneously. The power issues (average leakage and switching power dissipation) of the proposed inverter are investigated using QCAPro tool. The proposed inverter logic is compared with the existing designs, and results show the superiority of our designs over all the previous designs in terms of delay in the circuit, occupation in terms of area, the power consumed

and count of QCA cells. The effectiveness of the proposed logic is, further, established by the implementation of fault-tolerant 'adder' and 'XOR' logic.

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