



Implementation of Closed-Loop Control of NSC-Drive with Reactive Power Compensation

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Abstract

This paper presents a closed-loop control scheme of the AC–DC–AC nine switch converter (NSC) with induction motor operated under dynamic loading conditions. In industries, induction motors are widely used which are operated at lagging power factor and different loading conditions. The electrical distribution company demands high power factor operation, and it gives benefits to the consumer on operating a system closer to unity. The scope of this paper is to control active and reactive power flow between NSC-drive and utility within NSC converter operating constraints. The control scheme is developed such that the active power required for the induction motor is directly transferred from the utility without affecting DC-link voltage. Also, the NSC with induction motor is used to operate at unity power factor and even at leading power factor. On operating NSC at desired leading power factor, the required reactive power at the point of common coupling can be compensated. The proposed control algorithm is implemented in MATLAB software as well as in the hardware. The 5 KVA prototype of NSC is developed in the laboratory. Software and hardware results confirmed the practicability of the proposed control technique.

Keywords Digital signal controller · Nine switch converter · Twelve switch converter · Induction motor · Reactive power

1 Introduction

Evolution of powerful semiconductor devices and high-speed digital signal controller (DSC) offered the opportunity for innovative circuit techniques. There has been an increased interest in reduced switch topology of power converter among the researchers [1,2]. Reduction in power switches leads to compact circuit design, lowering cost and increase in efficiency. Practical implementation of high switching power devices with modified pulse width modulation (PWM) techniques is possible with high-speed DSC processor [3,4]. Many DSC manufacture companies developed application dedicate DSCs which are cheap in cost and consume less

power. These DSCs have built-in high-speed PWM modules to operate power electronics switches, analog to digital converter (ADC) and digital to analog converter (DAC) to process signal inside the processor, input capture to measure the pulse frequency, timers, output compare to generate interrupt signal on match event, quadrature encoder interface (QEI) to measure speed. A single DSC can be optimally used to control power electronics converters [5,6].

The conversion of AC–DC–AC is required for many industrial applications. Various topologies are available in the literature for AC–AC conversions, e.g., conventional twelve switch converter (TSC) [7], matrix converter [8], sparse matrix converter, etc., [9]. These converters require more active switches and complex logic control [10]. The use of many power switches increases the cost, and at the same time, it reduces the reliability of the power conversion system. For the equal rating of converters, the reduction in the number of active switches reduces drive circuits and power losses of the circuit. Thus, the cost, size, and weight of the circuit reduce with the increase in reliability and efficiency [11]. The NSC requires only nine active switches for AC–DC–AC conversion in a single stage as shown in Fig. 1 [12]. The NSC has 2 three-phase independent terminals with common DC-link. The NSC can be operated as DC–AC, with DC as an input

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source and two independent three-phase AC output. It can be used as AC–DC–AC with DC and AC output. The hybrid input configuration is also possible with renewable DC and three-phase AC source as input and single three-phase output of the NSC. Depending upon the various connection configurations of AC–DC sources and load, various applications are found in the literature. Figure 2 shows various applications of the NSC. It is used as a three-phase single input and dual output matrix converter [13], dual input and dual output z-source inverter [14] and grid integration of hybrid AC/DC energy resources [15] as shown in Fig. 2a–c. Figure 2d, e shows the application of NSC for the electric vehicle based on the bidirectional z-source inverter with battery charging and motor drive [16,17]. The NSC with three-phase AC input and AC output is used in uninterrupted power supply [18], distributed generation station [19], and wind power system [20] which is shown in Fig. 2f–h.

The reduced in switch count imposes certain operating criteria of the NSC. When NSC is operated at different frequency modes, e.g., adjustable speed drives, the DC-link voltage requirement goes to twice of the rated voltage compared to the conventional TSC. However, when the NSC is operated at a constant frequency as in UPS, the rated voltage requirement is equal to TSC. The application criteria of the NSC confirm that the efficiency of NSC, when operated at constant frequency, is more as compared to TSC [19,21–

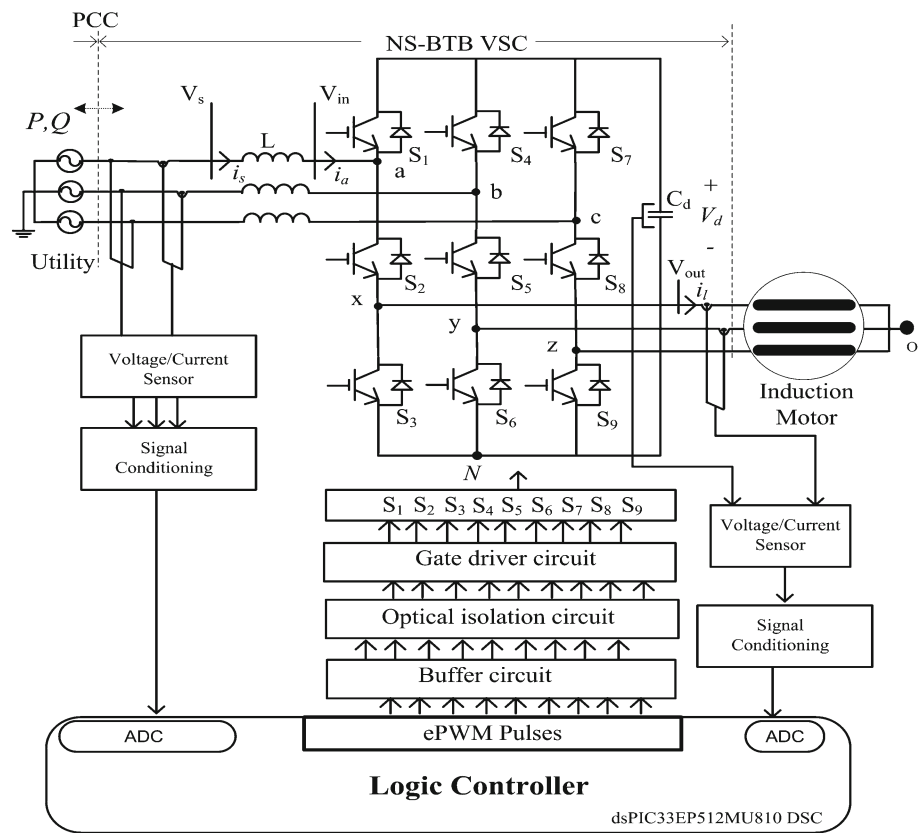
23]. Due to these merits, the NSC is operated under constant frequency mode.

In industries, for various applications, the number of induction motors is operated at constant speed and variable loading condition, e.g., water pump, cooling fan, and exhaust fan. These induction motors are operated on lagging power factor which absorbs reactive power from the utility. The electrical distribution company emphasis on the operating a system closer to unity power factor. It gives incentives to the consumer on operating system at good power factor closer to unity. In the proposed control scheme, the NSC with induction motor is not only operated at unity power factor but also at leading power factor delivering reactive power from NSC to the point of common coupling (PCC) to achieve utility unity power factor operation. The closed-loop control technique for NSC is developed such that it controls real and reactive power independently. With the change in loading on induction motor, NSC is operated at desired power factor.

In summary, this paper features:

- Operation of the utility-connected NSC with induction motor load at unity power factor.
- The NSC is operated as rectifier and inverter simultaneously. For rectifier operation, instantaneous utility angle is tracked using synchronous reference frame phase lock loop (SRF-PLL).

Fig. 1 Induction motor driven by NSC using DSC



- The algorithm for closed-loop control of NSC with induction motor is implemented in DSC dsPIC33EP512MU810.
- The algorithm is developed such that the real power required by the induction motor is transferred directly from the utility, without affecting DC-link voltage under dynamic loading on the induction motor.
- By operating NSC at leading power factor, reactive power is transferred from converter to the utility.
- The NSC is operated under constant frequency operation; thus, efficiency is more as compared to the convention TSC.

The paper is structured as follows. In Sect. 2, the operation of the NSC and generation of the gate signal are presented. Total loss comparison between NSC and TSC is presented in Sect. 2.1. The proposed closed-loop control scheme is

explained in Sect. 3. In Sect. 4, tracking of instantaneous angle of the utility is explained. The simulation and experimental results are presented in Sects. 5 and 6, respectively. Finally, the conclusion is drawn in Sect. 7.

2 Nine Switch Converter

2.1 Operation

Figure 1 shows the induction motor driven by NSC using DSC. The source inductor (L) is connected between three-phase source and NSC. The DC-link capacitor (C_d) is connected as an intermediate source. Points $a, b,$ and c are the input terminal, and $x, y,$ and z are the output terminal points. Three switches are connected in series in a single leg. These

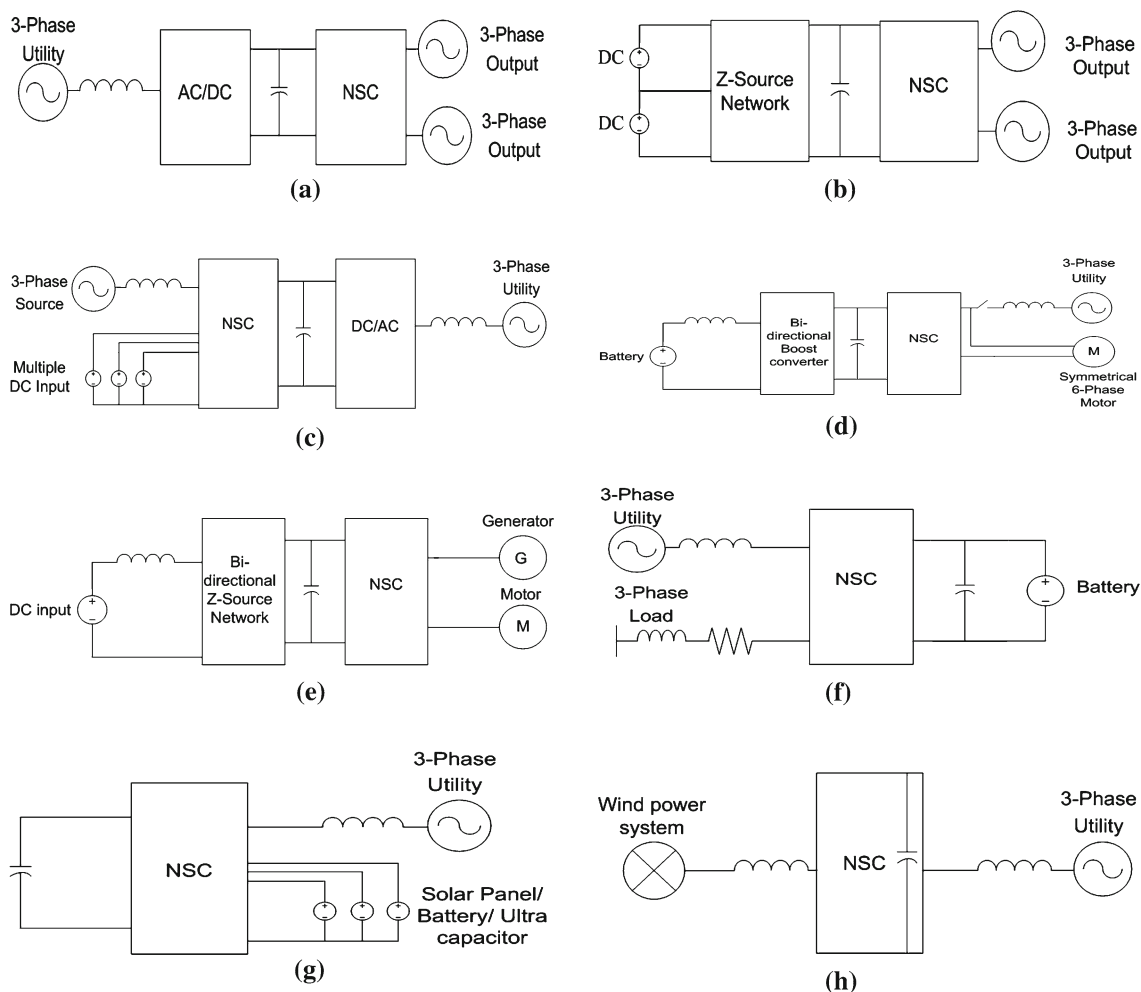
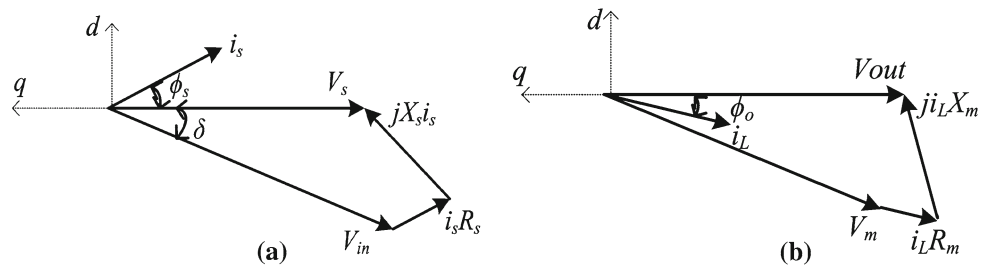


Fig. 2 Various applications of the NSC. **a** 3-Phase single input and dual output matrix converter. **b** Dual input and dual output z-source inverter. **c** Grid integration of hybrid AC/DC energy resources. **d** Bidirectional z-source inverter with battery charging and motor drive. **e** Integrated

motor drive and battery charging system for electric vehicle. **f** Uninterrupted power supply. **g** Distributed generation station. **h** Wind power system

Fig. 3 Phasor representation. **a** Supply side. **b** Load side



three legs are connected in parallel to form NSC. Point N is negative terminal of DC-link. The dsPIC33EP512MU810 DSC is used to control the operation of the NSC. The ADC module of DSC is used to measure system voltages and currents continuously. To measure voltage and current, LEM-LV 20P and LA 25A sensors are used. The signal conditioning circuitry is developed to interface sensor output to the DSC. The high-speed PWM of DSC is used to generate desired gate pulses. These PWM pulses of DSC are unable to drive the power devices due to its low electrical characteristics. Thus, these PWM pulses are processed through the buffer circuit, optical isolation circuit, and gate driver circuit. The buffer circuit amplifies the PWM pulses. The optical isolation circuit provides the isolation between the power circuit and low power DSC circuit. The gate driver circuitry drives the power devices by supplying appropriate PWM pulse current magnitude.

The NSC simultaneously operated as a rectifier and inverter in the single stage. For the operation of the rectification and the inversion, two modulating references (Ref_{rec} and Ref_{inv}) are required which are compared with single carrier reference to get desired gate pulses. As shown in Fig. 1, the V_s is the utility phase voltage. The V_{in} and V_{out} are the input and output phase voltages of the NSC. The voltage magnitude and frequency of the V_{in} and V_{out} depend on modulating references Ref_{rec} and Ref_{inv} , respectively. The common DC-link capacitor voltage V_d is shared for rectifier and inverter operation. The sinusoidal pulse width modulation technique is used. Thus, relation between V_{in} and V_{out} with common DC-link is given by

$$V_{in} = Ref_{rec} V_d / 2 \tag{1}$$

$$V_{out} = Ref_{inv} V_d / 2 \tag{2}$$

The active power flow from source to NSC is mainly dependent on the angle δ between V_s and V_{in} . Also, DC-link capacitor voltage depends on the charging of capacitor which indirectly is based on the angle δ . The reactive power exchange between source and NSC mainly depends on voltage magnitude of V_s and V_{in} [24,25]. Figure 3 shows the phasor representation of supply side and load side variables. As shown in Fig. 3a, magnitude of V_{in} is greater than magnitude of V_s ; thus, source phase current (i_s) leads V_s by an

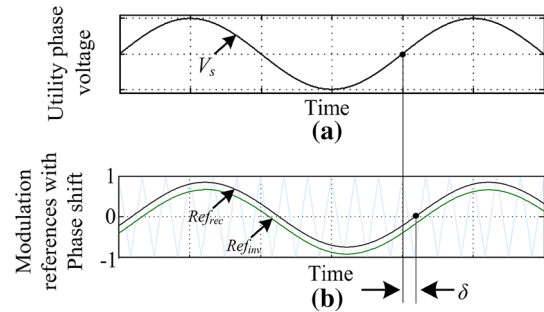


Fig. 4 Utility phase voltage and phase shifted modulation references

angle ϕ_s delivering reactive power from NSC to the utility. Figure 3b shows phasor representation of load side where load current (i_L) lags NSC output phase voltage (V_{out}) by load angle ϕ_L . The magnitude of V_{in} and V_{out} is dependent on DC-link voltage as per (1) and (2). Thus, real and reactive power is dependent on angle δ . In ideal conditions, i.e., neglecting the resistance (R_s) of source inductance, real and reactive power is given by

$$P_S = (V_s V_{in} \sin \delta) / X_L \tag{3}$$

$$Q_S = (V_s^2 - V_s V_{in} \cos \delta) / X_L \tag{4}$$

The angle δ is controlled by shifting Ref_{rec} with respect to V_s as shown in Fig. 4. Thus to control real and reactive power of the NSC, sinusoidal modulating references are modified. The three-phase modulation references are given by

$$\begin{aligned} Ref_{rec_a} &= m_r \sin(\theta + \delta) + dc_u \\ Ref_{rec_b} &= m_r \sin(\theta - 120^\circ + \delta) + dc_u \\ Ref_{rec_c} &= m_r \sin(\theta + 120^\circ + \delta) + dc_u \\ Ref_{inv_x} &= m_i \sin(\theta + \delta) - dc_L \\ Ref_{inv_y} &= m_i \sin(\theta - 120^\circ + \delta) - dc_L \\ Ref_{inv_z} &= m_i \sin(\theta + 120^\circ + \delta) - dc_L \end{aligned} \tag{5}$$

where m_r and m_i are the modulation indices of rectifier and inverter, respectively. The angle θ is the instantaneous angle of the utility, and δ is a phase shift angle. A small dc-offset dc_u and dc_L is added and subtracted from Ref_{rec} and Ref_{inv} , respectively, to satisfy the switching constraints of the NSC detailed in next subsection.

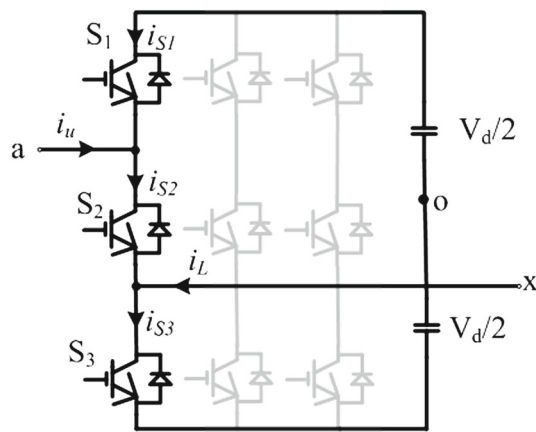


Fig. 5 Nine switch converter

Table 1 Switching states

Switching states (SS)	S_1	S_2	S_3	V_{ao}	V_{xo}
<i>Valid states</i>					
1	1	1	0	$V_d/2$	$V_d/2$
2	1	0	1	$V_d/2$	$-V_d/2$
3	0	1	1	$-V_d/2$	$-V_d/2$
<i>Forbidden states</i>					
4	1	1	1	0	0
5	0	0	0	0	0
6	1	0	0	$V_d/2$	0
7	0	1	0	0	0
8	0	0	1	0	$-V_d/2$

2.2 Generation of Gate Signals and Switching Constrains

To understand the generation of gate signals, one leg of an NSC is considered as shown in Fig. 5. The terminal o is the midpoint of the DC-link capacitor. There are three switches connected in series in each leg. They made eight possible switching states (2^3) as shown in Table 1. Among these, only three (1–3) switching states are valid. The rest of the switching states (4–8) should not be consider to avoid short circuit of the DC-link and open circuit of the inductive load. The terminal voltages V_{ao} and V_{xo} are measured for the valid switching states. It is observed that upper terminal voltage (V_{ao}) is always greater than or equal to the lower terminal voltage (V_{xo}).

$$V_{ao} \geq V_{xo} \tag{6}$$

V_{ao} and V_{xo} are the function of DC-link capacitor voltage and corresponding duty cycle D_1 and D_2 . Thus, it can be related as follows:

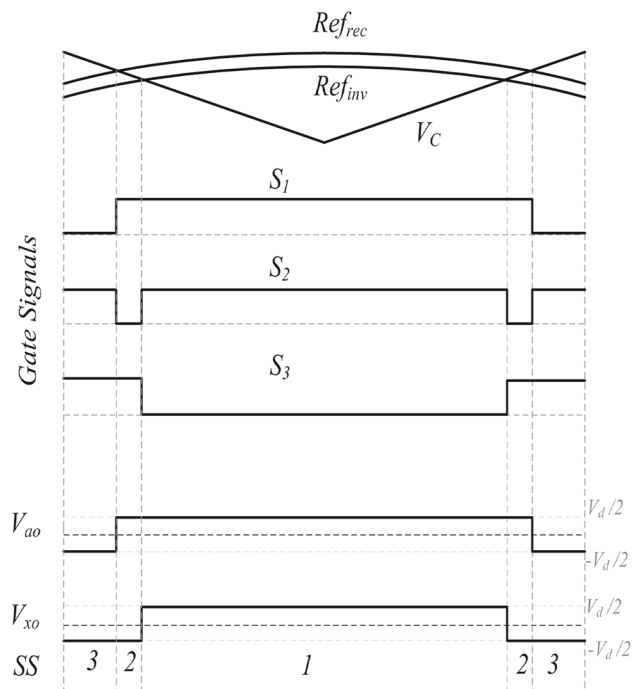


Fig. 6 Gate signal generation

$$V_d/2(2D_1 - 1) \geq V_d/2(2D_2 - 1) \tag{7}$$

$$D_1 \geq D_2 \tag{8}$$

which represents a constraint to avoid switching states 4 to 8 operation. To ensure this condition, a small dc-offset is added and subtracted with rectifier and inverter references, respectively, as given in Eq. 5. Figure 6 shows gate pulse generation. Two modulating references Ref_{rec} and Ref_{inv} are compared with single carrier waveform. Analyzing the terminal voltages V_{ao} and V_{xo} , when S_1 (upper switch) is high, V_{ao} is positive and when S_3 (lower switch) is high, V_{xo} is negative. The complimentary of S_3 , i.e., \bar{S}_3 gives positive V_{xo} . Thus, complementary logic is applied to the lower switch signal. Gating signal for the middle switch is then generated by performing logical operation $S_2 = S_1 \oplus \bar{S}_3$, where \oplus is the XOR operator.

3 Closed-Loop Control of NSC-Drive

3.1 Proposed Control Scheme

Figure 7 shows the proposed closed-loop control scheme of the NSC. The NSC operates in rectifier as well as in inverter mode simultaneously. For desired rectification operation, instantaneous utility angle θ must be known. To track the instantaneous angle of the utility, SRF-PLL is developed. This angle θ is used to generate modulating references as given in (5). The real and reactive power flow is controlled

Fig. 7 Proposed control scheme

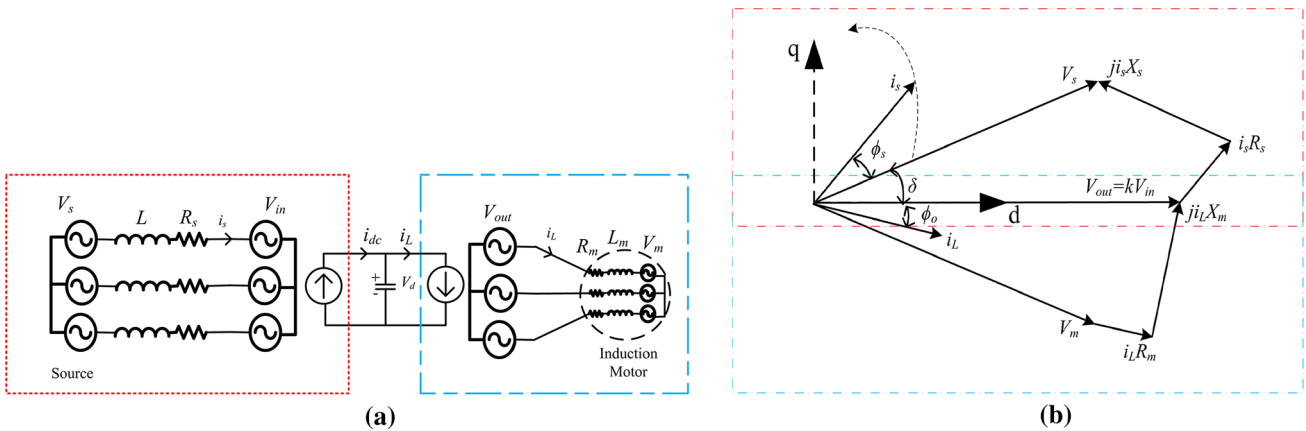
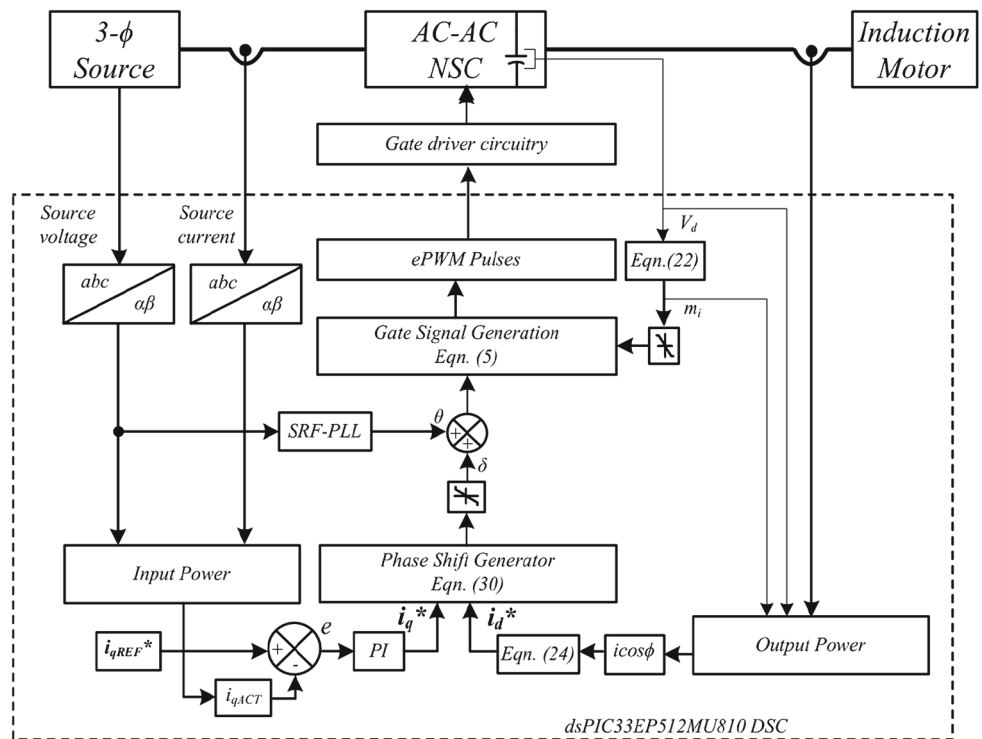


Fig. 8 Representation of NSC with induction motor system. **a** Equivalent circuit diagram. **b** Equivalent phasor diagram

independently such that with the change in motor load, real power is directly transferred from the input source keeping the DC-link voltage constant. The control scheme is developed in such a way that, with a varying load, NSC operates at desired reactive power reference. To achieve independent control of real and reactive power flow, two current references i_d^* and i_q^* are used, respectively. To find i_d^* , input and output real power of NSC is equated. Reactive power mainly depends on magnitude difference between V_s and V_{in} . Thus, the expression for V_{in} is derived to achieve desired reactive power exchange between NSC and utility. As shown in Fig. 7, both input and output instantaneous powers of the NSC are measured to generate reference real and reactive current signals. For simplicity, equivalent circuit and phasor diagram of

the NSC with induction motor are drawn as shown in Fig. 8. Figure 8a shows DC-link capacitor is shared by both the rectifier and inverter operation. The rectifier and inverter voltages are the function of common DC-link voltage V_d . Thus, combining phasor diagrams shown in Fig. 3a, b, equivalent phasor diagram of complete NSC with V_d as a reference is redrawn in Fig. 8b. A dq-reference representation of a three-phase system is used for control and analysis for the NSC. For a three-phase system, real and reactive power is given by

$$P(t) = \frac{3}{2} [V_d(t)i_d(t) + V_q(t)i_q(t)] \tag{9}$$

$$Q(t) = \frac{3}{2} [-V_d(t)i_q(t) + V_q(t)i_d(t)] \tag{10}$$

Aligning the d -axis of the V_{in} and V_{out} with the d -axis of the synchronous reference frame: For rectifier operation

$$V_d = V_{ind} \tag{11}$$

$$V_q = 0 \tag{12}$$

For inverter operation

$$V_d = V_{outd} \tag{13}$$

$$V_q = 0 \tag{14}$$

By using (11), (13), and (14), real power at the rectifier input side is given by

$$P_{in} = \frac{3}{2}[V_{ind} i_{sd}] \tag{15}$$

Bu using (11), (15), and (16), real power at the inverter output side is given by

$$P_{out} = \frac{3}{2}[V_{outd} i_{ld}] \tag{16}$$

where i_{ld} is d -axis component of load current. Assuming the NSC to be loss less and applying power balance criteria,

$$P_{in} = P_{out} \tag{17}$$

$$\frac{3}{2}[V_{ind} i_{sd}] = \frac{3}{2}[V_{outd} i_{ld}] \tag{18}$$

As the same dc-link is shared by the rectifier and inverter, V_{ind} and V_{outd} is given by

$$V_{ind} = \text{Ref}_{rec} V_d/2 \tag{19}$$

$$V_{outd} = \text{Ref}_{inv} V_d/2 \tag{20}$$

By using (17), (18), and (19)

$$i_{sd} = \left[\frac{m_i}{m_r} \right] i_{ld} \tag{21}$$

Equation (23) gives relation between source current and load current in terms of modulation index of rectifier and inverter reference. From the phasor diagram i_{ld} is given by

$$i_{sd} = \left[\frac{m_i}{m_r} \right] i_l \cos\phi_o \tag{22}$$

where ϕ_o is load phase angle. Rectifier terminal voltage is given by

$$V_{in} = V_s - (R_s + jX_s)i_s \tag{23}$$

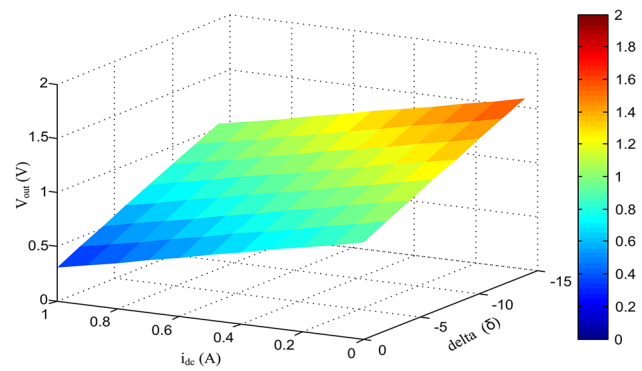


Fig. 9 Effect of δ and loading on inverter output voltage

where

$$i_s = i_{sd}^* + j i_{sq}^* \tag{24}$$

From (23) and (24)

$$V_{in} = (V_s - R_s i_{sd}^* + X_s i_{sq}^*) - j(R_s i_{sq}^* + X_s i_{sd}^*) \tag{25}$$

The rectifier input terminal voltage magnitude and phase angle is given by

$$V_{in} = |V_{in}| \angle \delta \tag{26}$$

where

$$|V_{in}| = \sqrt{(V_s - R_s i_{sd}^* + X_s i_{sq}^*)^2 + (R_s i_{sq}^* + X_s i_{sd}^*)^2} \tag{27}$$

$$\angle \delta = \tan^{-1} \frac{(R_s i_{sq}^* + X_s i_{sd}^*)}{(V_s - R_s i_{sd}^* + X_s i_{sq}^*)} \tag{28}$$

From (29) and (30), it is observed that the magnitude and phase angle can be controlled by generating reference currents i_{sd}^* and i_{sq}^* . The (24) is used for the generation of i_{sd}^* reference, and i_{sq}^* is calculated from required reactive power compensation.

3.2 Relation Between δ and DC-Link Capacitor

The reactive power transfer is dependent on the magnitude of V_{in} . V_{in} is a function of DC-link capacitor voltage.

$$V_{in} = K_1 V_d \tag{29}$$

For sinusoidal pulse width modulation technique,

$$K_1 = m_r/2\sqrt{2} \tag{30}$$

This DC-link voltage is a function of angle δ . The relation between DC-link voltage and angle δ is determined by power

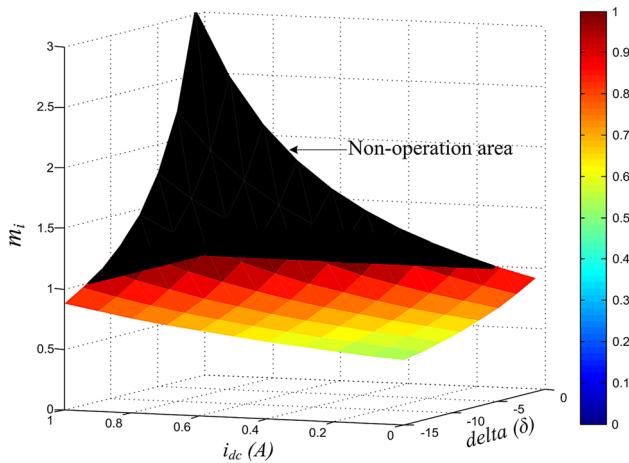


Fig. 10 Effect of δ and loading on m_i

balance condition between source side and intermediate DC-link capacitor. The source current i_s which is controlled by the magnitude and angle of V_{in} charges the DC-link capacitor. Thus, power balance equation can be expressed in d-q frame as follows:

$$V_d i_{dc} = V_{ind} i_{sd} + V_{inq} i_{sq} \tag{31}$$

Phasor representation shown in Fig. 3a gives relation between source voltage and V_{in} . The phasor diagram can be expressed in d-q frame as

$$V_{sd} = V_{ind} + R_s i_{sd} - X_s i_{sq} \tag{32}$$

$$V_{sq} = V_{inq} + R_s i_{sq} + X_s i_{sd} \tag{33}$$

From (34) and (35),

$$i_{sd} = \frac{-R_s V_{ind} + X_s V_{sq} - X_s V_{inq}}{R_s^2 + X_s^2} \tag{34}$$

$$i_{sq} = \frac{-R_s V_{inq} + R_s V_{sq} + X_s V_{ind}}{R_s^2 + X_s^2} \tag{35}$$

Aligning V_s to d-axis

$$V_{sq} = 0, V_{sd} = \sqrt{3} V_s \tag{36}$$

$$V_{ind} = \sqrt{3} |V_{in}| \cos \delta \tag{37}$$

$$V_{inq} = -\sqrt{3} |V_{in}| \sin \delta \tag{38}$$

By using (31)–(40),

$$V_d = \frac{V_s}{R_s K_1} (R_s \cos \delta - X_s \sin \delta) - \frac{i_{dc} (R_s^2) + X_s^2}{3 K_1^2 R_s} \tag{39}$$

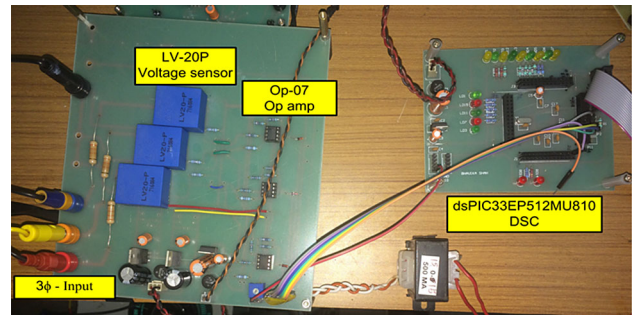


Fig. 11 Sensor circuit with DSC

As V_d is common for the inverter and rectifier operation, inverter output voltage is given by:

$$V_{out} = K_2 V_d \tag{40}$$

where,

$$K_2 = \frac{m_i}{2\sqrt{2}} \tag{41}$$

From (39) and (40), inverter output voltage is given by

$$V_{out} = \frac{K_2 V_s}{R_s K_1} (R_s \cos \delta - X_s \sin \delta) - \frac{i_{dc} K_2 (R_s^2) + X_s^2}{3 K_1^2 R_s} \tag{42}$$

To study effect of variation of δ and loading of NSC on inverter output voltage, (41) is used. If $m_r = m_i = 1$, then $K_1 = K_2 = 0.3535$. The analysis is carried out considering practical condition with source inductance of 10 mH and its internal resistance of 1.63Ω. Let; V_s be 1 pu. Figure 9 shows the relation of V_{out} with respect to change in δ and loading. As Ref_{REC} is phase shifted by an angle δ (negative) with respect to V_s , V_{out} (pu) increases. Also it is observe that as load increases, i.e., i_{dc} (pu) from 0 to 1 pu, V_{out} decreases. Thus, with the increase in load, δ should be increased to achieve constant V_{out} voltage. To drive induction motor, inverter output voltage must be constant irrespective of change in V_d and variable loading condition. Thus, to achieve constant V_{out} , m_i of NSC is changed. Figure 10 shows variation in m_i with respect to δ and loading. For reactive power compensation, DC-link voltage is increased by shifting Ref_{rec} with respect to V_s by an angle δ . Also with the change in loading m_i should be varied so as to achieve constant V_{out} voltage. It is observed that under loading condition, proper δ must be maintained for active power flow to avoid non-operation area of the converter. Otherwise, required m_i may be greater than 1, which results in over-modulation of the converter and this leads to increase in harmonics in V_{out} .

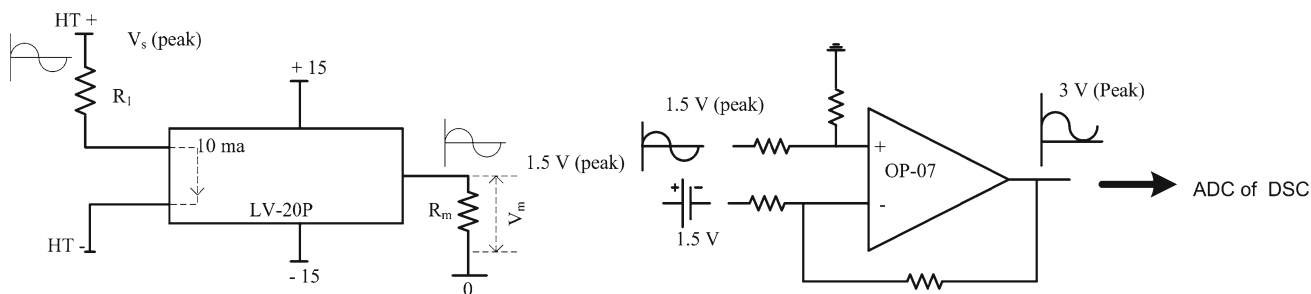


Fig. 12 Signal conditioning for DSC

Fig. 13 SRF-PLL for instantaneous θ extraction

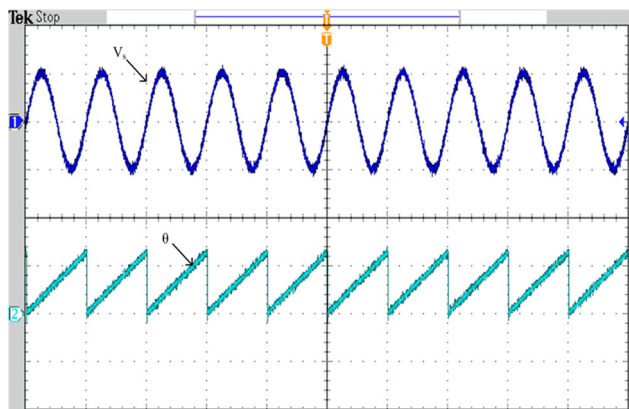
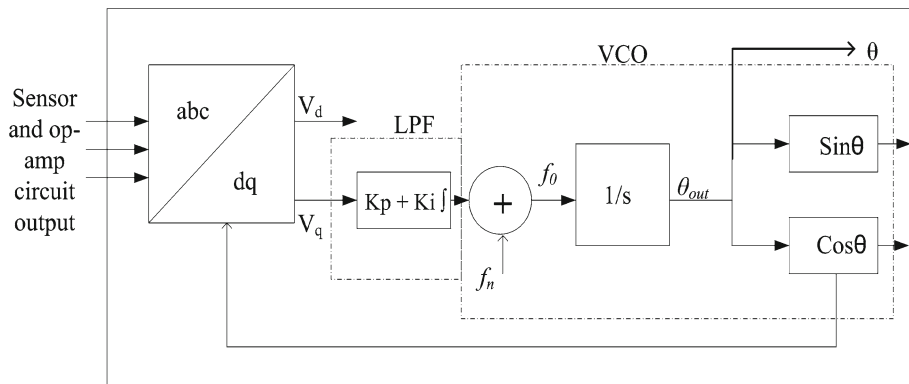


Fig. 14 Experimental result of tracking of instantaneous angle θ (5 radian/div) and V_s (1 pu/div)

4 Tracking of Instantaneous Angle of Utility

For the generation of modulation reference of rectifier Ref_{rec} of NSC, instantaneous angle θ is needed. The SRF-PLL technique is incorporated to track instantaneous angle θ . The algorithm is implemented in dsPIC33P512MU810 DSC. To implement SRF-PLL, three-phase voltage signals are required. The three-phase voltages are sense using Lem LV-20P voltage transducers. The electrical operating characteristic of DSC is 0–3.3 V. To convert sensor output within DSC operating range, signal conditioning is done using op-amp IC OP-07. Figure 11 shows the arrangement of sensor and op-amp circuit. The source phase voltage is sensed and converted into 0–3.3 V which is in DSC operating range. For single phase, signal conditioning using sensor and op-amp is shown in Fig. 12. The input source voltage is stepped

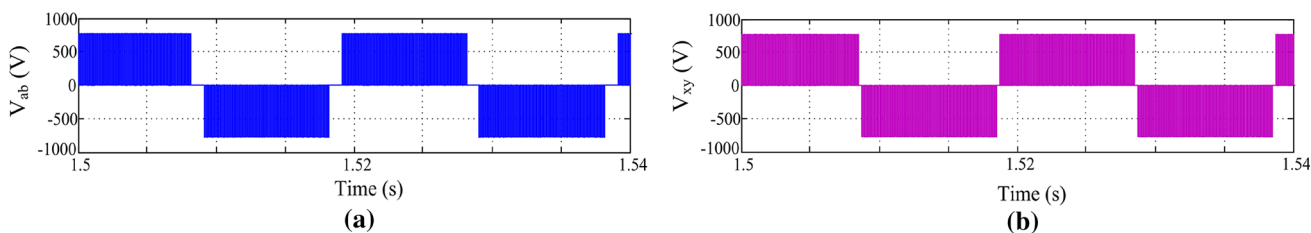


Fig. 15 NSC input and output line voltage. a NSC input line voltage. b NSC output line voltage

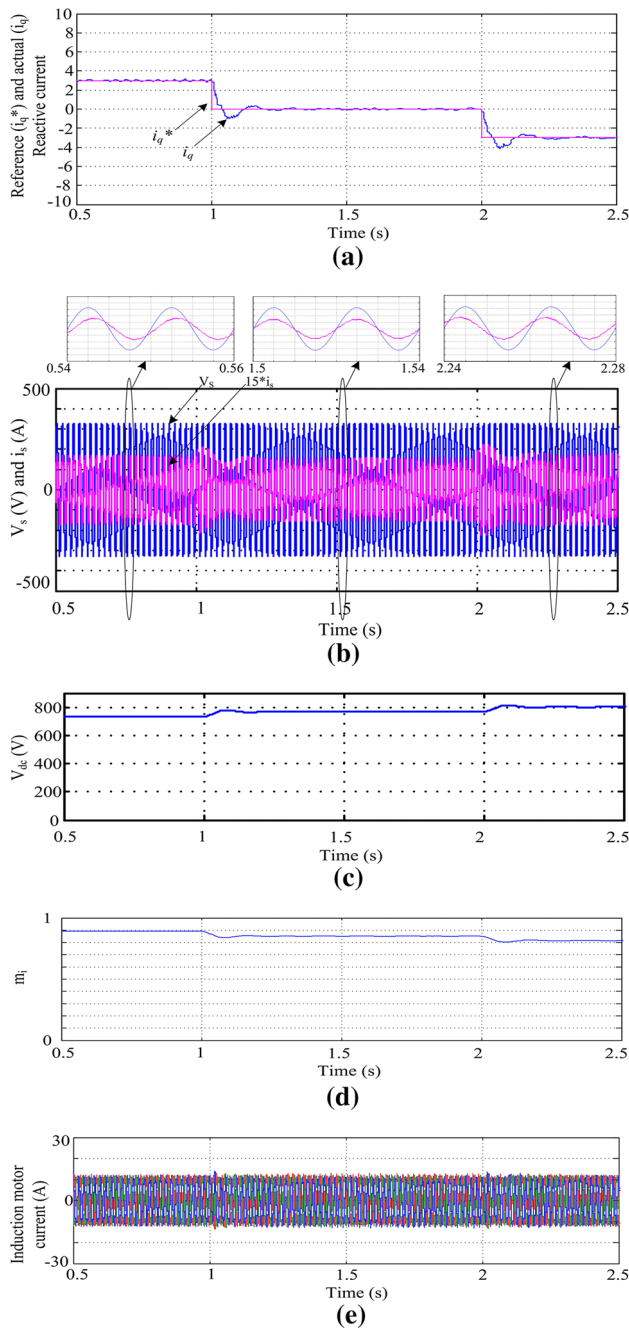


Fig. 16 Performance of NSC under varying i_q^* reference. **a** Effect of step change in reactive current reference. **b** Source phase voltage (V_s) and current (i_s). **c** DC-link capacitor voltage. **d** Change in inverter amplitude modulation index. **e** Constant load current

down to 1.5 V (peak). A dc offset of 1.5 V is added using OP07 IC such that negative half cycle is shifted up. The processed signals have a 3 V peak which is in the range of DSC. These three-phase analog signals are converted to digital for PLL operation inside the DSC. The phase angle of utility is extracted by implementing SRF-PLL in the software of the DSC. As shown in Fig. 13, the utility voltage is converted into stationary coordinates (α, β) by Clarke transformation. These

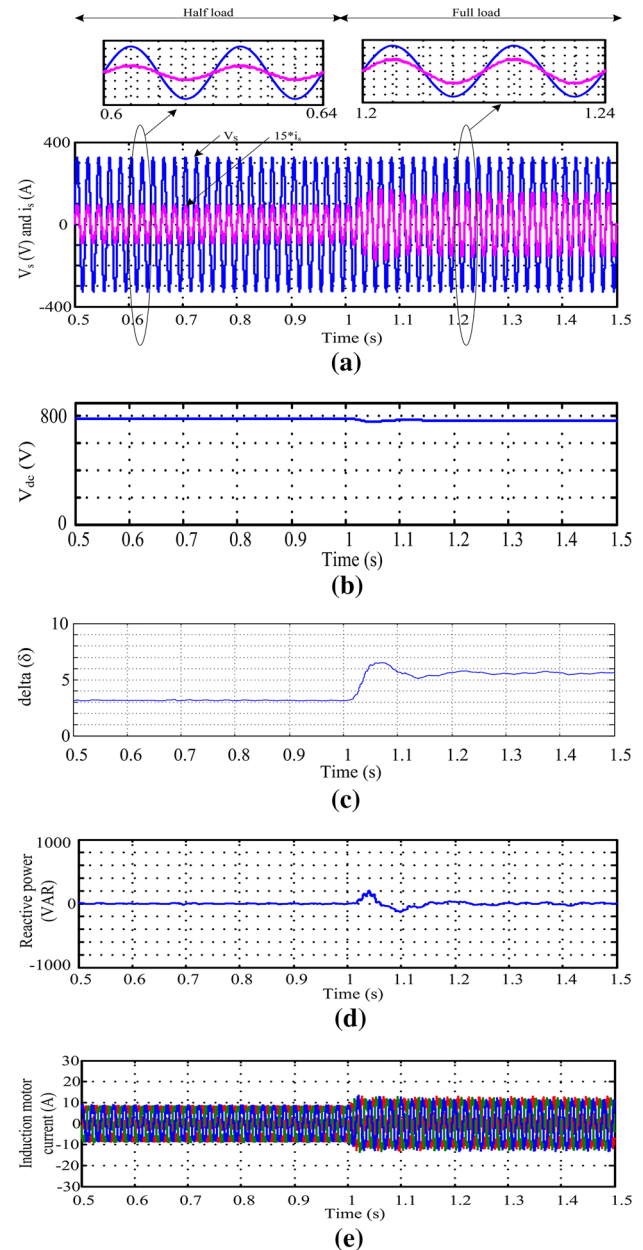


Fig. 17 Performance of NSC when $i_q^* = 0$ A under varying load condition. **a** Utility phase voltage (V_s) and current (i_s). **b** DC-link capacitor voltage. **c** Change in δ . **d** Per phase input reactive power. **e** Change in δ . **d** Per phase input reactive power. **e** Change in δ

coordinates are transformed to rotating reference (d, q) by Park transformation. The angular position of dq reference is regulated by a feedback control loop that forces V_q to zero. The loop filter is designed using proportional integrator [26,27]. To implement in DSC, the loop filter is developed in a discrete time domain by taking z-transform of the continuous equation. Thus, instantaneous angle θ of utility is extracted and used for generating references for rectifier operation. The experimental result of tracking of utility instantaneous angle θ is shown in Fig. 14.

Table 2 Simulation results

$[V_s = 230 \text{ V/phase}, m_r = 0.8]$

$i_q^* = 0\text{A}$	V_{ab1} (V) % THD	i_s (A) % THD	δ° (degree)	V_d (V)	m_i	V_{xy1} (V) % THD	i_L (A)	Input P.F	Input reactive power/phase (VAR)
Half load	388.2 89.6	3.98 4.6	3.16	782	0.837	401 85.53	5.3	0.99	0
Full load	381 89.79	6.98 3.2	5.6	770	0.85	402 86	7.6	0.99	0

5 Simulation Results

MATLAB simulation is performed with three-phase, 5.4 hp, 4 pole, 400 V, 50 Hz induction motor driven by NSC. The values of L , R_s , m_r are 10 mH, 1.63Ω, and 0.8, respectively. The switching frequency of the converter is 9kHz. To test the proposed control scheme, two cases are considered. In the first case, motor load is kept constant and i_q^* reference is varied. In the second case, reactive current reference (i_q^*) is kept constant and the motor load is changed from half load to full load. Figure 15a, b shows NSC input and output line voltage, which depends on the magnitude of DC-link capacitor voltage.

5.1 Case 1

As shown in control scheme (Fig. 7), to operate NSC at desired reactive power, i_q^* current reference is required. To test the performance of NSC for desired reactive power operation, the i_q^* reference current is changed in three steps 3 A, 0 A, and -3 A. Keeping constant loading the performance of NSC is studied. Figure 16a shows actual i_q follows reference i_q^* . The effect of the step change in i_q^* reference is observed in V_s and i_s shown in Fig. 16b. The Zoomed part shows that when $i_q^* = 3$ A, i_s lags V_s ; when $i_q^* = 0$ A, i_s is in phase with V_s ; and when $i_q^* = -3$ A, i_s leads V_s . Figure 16c shows as per change in reference i_q^* from 3 A to -3 A, DC-link capacitor voltage is increased. As the DC-link voltage is increased, inverter modulation index is decreased to maintain inverter output voltage constant. This is shown in Fig. 16d. Figure 16e shows constant load current although there is variation in i_q^* reference.

5.2 Case 2

Performance of NSC when $i_q^* = 0$ is studied under varying load conditions as shown in Fig. 17. Initially, induction motor is operated at half load and after 1 sec, it is operated at full load. Figure 17a shows V_s and i_s . As i_q^* reference is kept 0, the zoomed part of Fig. 17a shows that i_s is always in phase with V_s , only the magnitude of i_s is changed. Figure 17b shows a

stable DC-link voltage although there is the change in load condition. Of course there is a small drop in DC-link capacitor voltage. This is because of the internal resistance of source inductance. In practical systems, some internal resistance of source inductance is always present. Hence, a small internal resistance is included in simulation study also. Figure 17c shows variation in power angle δ with the change in load. As the load changes, δ is changed to supply required real power to get the faster response without dropping DC-link voltage level. Figure 17d shows that per phase input reactive power is zero although there is a change in load. This is because, i_q^* is set at 0. Figure 17e shows induction motor current at the half and full load. Table 2 summarizes all the system parameters keeping i_q^* reference constant and varying load condition.

The above simulation study reveals that the design of the proposed controller is perfect. The controller performance is verified under dynamic loading and different reference reactive power cases.

6 Experimental Setup and Results

To realize simulation results, the experimental setup is developed in the laboratory. Figure 18 shows prototype setup with the naming of various components. The results are taken in dynamic condition to ensure the feasibility of the closed-loop control of NSC-drive. Table 3 shows all the setup specifications. Figure 19 shows NSC input and output line voltages. Experimental verification is done for two cases. In the first case, i_q^* reference is varied and induction motor load is kept constant. In the second case, i_q^* reference is kept constant and induction motor load is varied.

In the first case, i_q^* reference is varied in three steps, i.e., $+0.4$ pu, 0 pu, and -0.2 pu with constant load on an induction motor. The effect of a change in i_q^* reference is observed on the power factor of the utility and amplitude of source current (i_a). When reference i_q^* is $+0.4$ pu, i_a lags to V_s by 40° , i.e., power factor is 0.76. After step change of i_q^* from $+0.4$ to 0 pu, i_a is in phase with V_s . With the step change of i_q^* from 0 pu to -0.2 pu, i_a leads to V_s by 20° , i.e., power factor is 0.93. The effect of a step change in i_q^* reference on

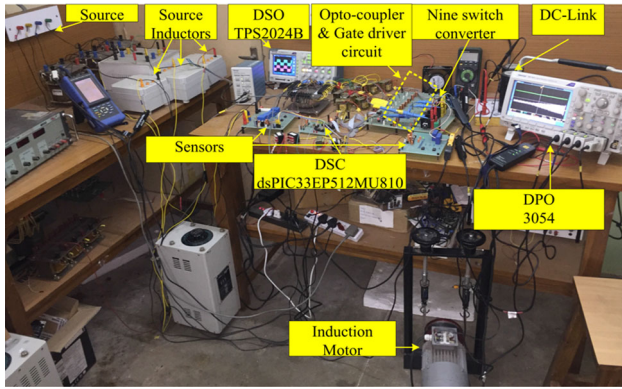


Fig. 18 Experimental setup

Table 3 Experimental Setup

Item	Specification
AC source	0–110 V
Source inductance	10 mH
IGBT	KGT25N120NDH
Gate driver IC	MIC4425
DSP	dsPIC33EP512MU810
Software	MPLAB X IDE v2.10
Sensors	LV-20P, LA-25P
Induction motor	1 hp, 4 Pole, 110 V, 50 Hz

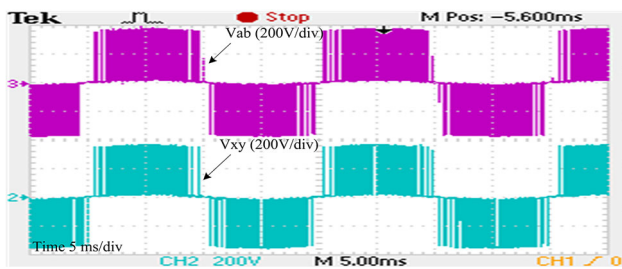


Fig. 19 NSC input (V_{ab}) and output (V_{xy}) line voltage

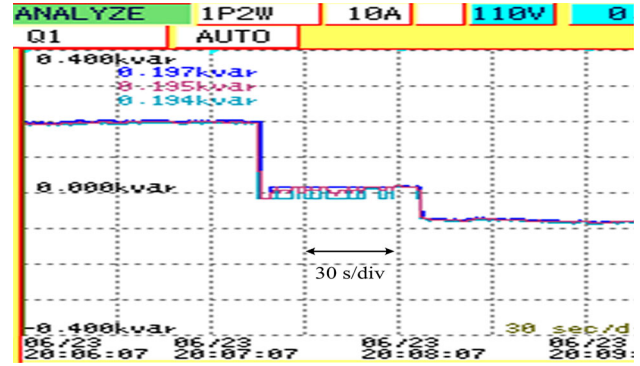


Fig. 21 Per phase reactive power for different i_q^* reference

utility phase voltage and current is shown in Fig. 20. With the step change in i_q^* reference DC-link capacitor voltages is also changed. Figure 20a shows lag to unity power factor operation of NSC. The DC-link voltage is increased from 360 to 400 V. Figure 20b shows unity to leading power factor operation of the NSC. The DC-link voltage is increased from 400 to 430 V. The experimental per phase reactive power is measured for all the i_q^* reference. It is observed that when i_q^* is + 0.4 pu, reactive power is absorbed from the utility. When i_q^* is 0pu, there is no reactive power transfer between NSC and utility. When the i_q^* is – 0.2 pu, reactive power is delivered to the utility from the NSC. Thus, operating at desired i_q^* reference, reactive power can be compensated. Figure 21 shows effect of a step change in i_q^* on the system VAR. Figure 22 shows three-phase induction motor current.

In the second case, the performance of NSC is tested keeping i_q^* reference constant, i.e., $i_q^* = 0$ pu. Figure 23 shows induction motor current and DC-link voltage. It shows that although the load is varying gradually from no load to full load, DC-link voltage remains constant. As DC-link voltage remains constant at 400 V, reactive power transfer between utility and NSC remains constant. Figure 24 shows V_s and i_s , at induction motor half load and full load condition keeping

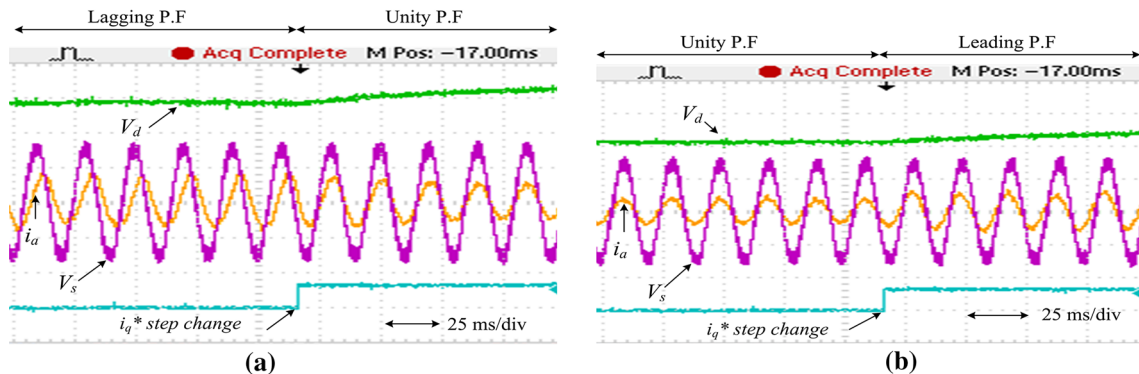


Fig. 20 Effect of step change in i_q^* reference on utility phase voltage and current. a Effect of step change in i_q^* from + 0.4 to 0 pu. b Effect of step change in i_q^* from 0 to – 0.2 pu

$i_q^* = 0$ pu. Figure 24a, b shows that V_s and i_s is in phase at half load as well as at full load.

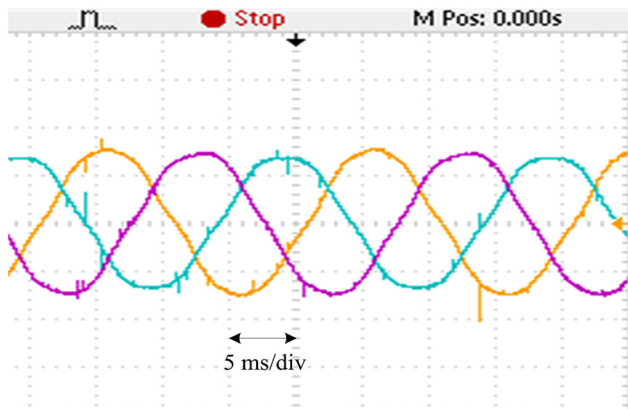


Fig. 22 Three-phase induction motor current

Fig. 23 Constant DC-link voltage with change in load on induction motor

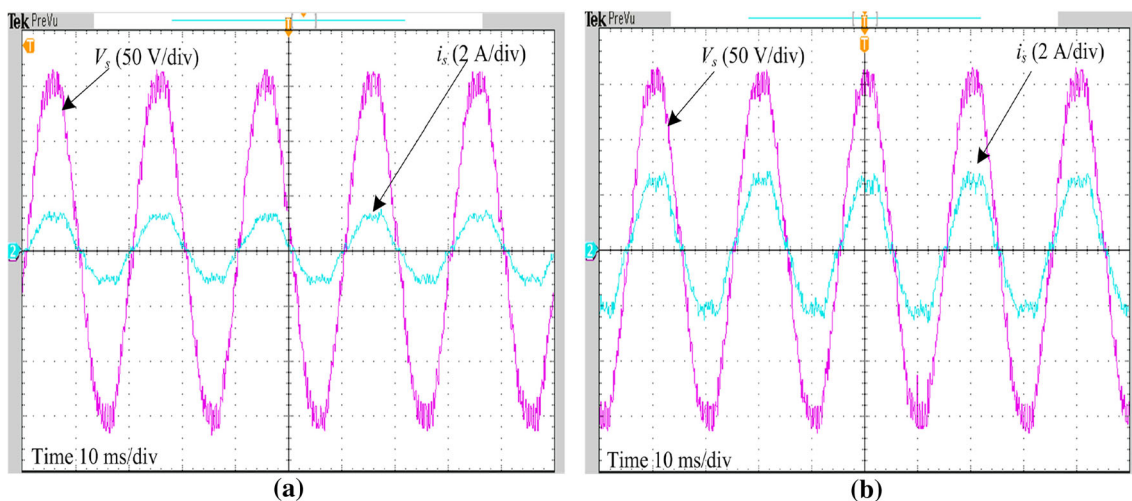
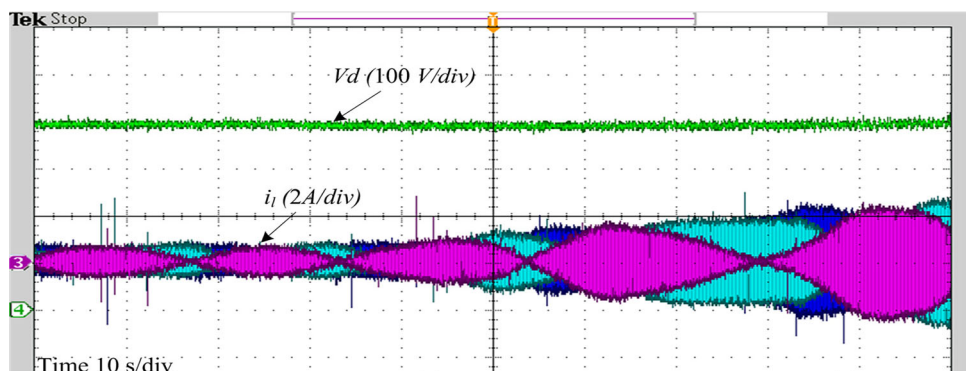


Fig. 24 Source phase voltage and current at $i_q^* = 0$ pu. a V_s and i_s at half load. b V_s and i_s is at full load

7 Conclusion

In this paper, a closed-loop control scheme is developed for NSC-drive with reactive power compensation. The NSC is not only operated at unity power factor but also operated at leading power factor delivering reactive power from NSC to the utility. The proposed control scheme is tested under dynamic loading condition on an induction motor. The mathematical and graphical analysis is presented to study the effect of loading on power angle δ and various parameters of the NSC. To track the instantaneous angle θ , SRF-PLL is implemented. The control logic is implemented in DSC dsPIC33EP512MU810. The software and experimental results validate the proposed closed-loop control technique for reactive power compensation at variable loading condition.

References

- Norambuena, M.; Kouro, S.; Dieckerhoff, S.; Rodriguez, J.: Reduced multilevel converter: a novel multilevel converter with a reduced number of active switches. *IEEE Trans. Ind. Electron.* **65**, 3636–3645 (2018)
- Baranwal, R.; Iyer, K.; Basu, K.; Castelino, G.; Ned, M.: A reduced switch count single stage three-phase bidirectional rectifier with high frequency isolation. *IEEE Trans. Power Electron.* **PP**(99), 1–1 (2017)
- Alias, A.; Rahim, N.A.; Hussain, M.A.: DSP-based modified SPWM switching technique with two-degrees-of-freedom voltage control for three-phase AC–DC buck converter. *Arab. J. Sci. Eng.* **39**(11), 8001–8013 (2014)
- Renge, M.; Suryawanshi, H.; Chaudhari, M.: Digitally implemented novel technique to approach natural sampling SPWM. *EPE J.* **20**, 13–20 (2010)
- Caruso, M.; Di Tommaso, A.O.; Genduso, F.; Miceli, R.; Galluzzo, G.R.: A DSP-based resolver-to-digital converter for high-performance electrical drive applications. *IEEE Trans. Ind. Electron.* **63**(7), 4042–4051 (2016)
- Harkare, C.; Harkare, H.: Design and development of a switched reluctance motor and dsPIC based drive. In: 2nd International Conference for Convergence in Technology (I2CT), pp. 960–964 (2017)
- Friedli, T.; Kolar, J.W.; Rodriguez, J.; Wheeler, P.W.: Comparative evaluation of three-phase AC–AC matrix converter and voltage DC-link back-to-back converter systems. *IEEE Trans. Ind. Electron.* **59**(12), 4487–4510 (2012)
- Metidji, T.N.; Rekioua, B.: A fixed switching frequency direct torque control strategy for induction motor drives using indirect matrix converter. *Arab. J. Sci. Eng.* **39**(3), 2001–2011 (2014)
- Kolar, J.W.; Schafmeister, F.; Round, S.D.; Ertl, H.: Novel three-phase AC–AC sparse matrix converters. *IEEE Trans. Power Electron.* **22**(5), 1649–1661 (2007)
- Kolar, J.W.; Friedli, T.; Rodriguez, J.; Wheeler, P.W.: Review of three-phase PWM AC–AC converter topologies. *IEEE Trans. Ind. Electron.* **58**(11), 4988–5006 (2011)
- Sandoval, J.; Krishnamoorthy, H.; Enjeti, P.; Choi, S.: Reduced active switch front-end multipulse rectifier with medium-frequency transformer isolation. *IEEE Trans. Power Electron. J.* **32**(10), 7458–7468 (2017)
- Liu, C.; Wu, B.; Zargari, N.R.; Xu, D.; Wang, J.: A novel three-phase three-leg AC/AC converter using nine IGBTs. *IEEE Trans. Power Electron.* **24**(5), 1151–1160 (2009)
- Liu, X.; Wang, P.; Loh, P.C.; Blaabjerg, F.: A compact three-phase single-input/dual-output matrix converter. *IEEE Trans. Ind. Electron.* **59**(1), 6–16 (2012)
- Dehghan, S.M.; Mohamadian, M.; Yazdian, A.; Ashrafzadeh, F.: A dual-input dual-output Z-source inverter. *IEEE Trans. Power Electron.* **25**(2), 360–368 (2010)
- Liu, X.; Loh, P.C.; Wang, P.; Blaabjerg, F.: A direct power conversion topology for grid integration of hybrid AC/DC energy resources. *IEEE Trans. Ind. Electron.* **60**(12), 5696–5707 (2013)
- Diab, M.S.; Elserougi, A.A.; Abdel-Khalik, A.S.; Massoud, A.M.; Ahmed, S.: A nine-switch-converter-based integrated motor drive and battery charger system for EVs using symmetrical six-phase machines. *IEEE Trans. Ind. Electron.* **63**(9), 5326–5335 (2016)
- Dehghan, S.M.; Mohamadian, M.; Yazdian, A.: Hybrid electric vehicle based on bidirectional Z-source nine-switch inverter. *IEEE Trans. Veh. Technol.* **59**(6), 2641–2653 (2010)
- Liu, Congwei; Wu, Bin; Zargari, N.; Xu, D.: A novel nine-switch PWM rectifier-inverter topology for three-phase UPS applications. In: European Conference on Power Electronics and Applications, pp. 1–10 (2007)
- Loh, P.C.; Zhang, L.; Gao, F.: Compact integrated energy systems for distributed generation. *IEEE Trans. Ind. Electron.* **60**(4), 1492–1502 (2013)
- Wen, G.; Chen, Y.; Zhong, Z.; Kang, Y.: Dynamic voltage and current assignment strategies of nine-switch-converter-based DFIG wind power system for low-voltage ride-through (LVRT) under symmetrical grid voltage dip. *IEEE Trans. Ind. Appl.* **52**(4), 3422–3434 (2016)
- Qin, Z.; Loh, P.C.; Blaabjerg, F.: Application criteria for nine-switch power conversion systems with improved thermal performance. *IEEE Trans. Power Electron.* **30**(8), 4608–4620 (2015)
- Ali, K.; Das, P.; Panda, S.K.: A special application criterion of nine-switch converter with reduced conduction loss. *IEEE Trans. Ind. Electron.* **99**, 31–36 (2017)
- Zhang, L.; Loh, P.C.; Gao, F.: An integrated nine-switch power conditioner for power quality enhancement and voltage sag mitigation. *IEEE Trans. Power Electron.* **27**(3), 1177–1190 (2012)
- Veas, D.R.; Dixon, J.W.; Ooi, B.-T.: A novel load current control method for a leading power factor voltage source PWM rectifier. *IEEE Trans. Power Electron.* **9**(2), 153–159 (1994)
- Dixon, J.; Moran, L.; Rodriguez, J.; Domke, R.: Reactive power compensation technologies: state-of-the-art review. *Proc. IEEE* **93**(12), 2144–2164 (2005)
- Shitole, A.B.; Suryawanshi, H.M.; Talapur, G.G.; Sathyan, S.; Balal, M.S.; Borghate, V.B.; Ramteke, M.R.; Chaudhari, M.A.: Grid interfaced distributed generation system with modified current control loop using adaptive synchronization technique. *IEEE Trans. Ind. Inform.* **13**(5), 2634–2644 (2017)
- da Silva, C.H.; Pereira, R.R.; da Silva, L.E.B.; Lambert-Torres, G.; Bose, B.K.; Ahn, S.U.: A digital PLL scheme for three-phase system using modified synchronous reference frame. *IEEE Trans. Ind. Electron.* **57**(11), 3814–3821 (2010)

