Arabian Journal for Science and Engineering (2019) 44:2453–2465
https://doi.org/10.1007/s13369-018-3586-3

RESEARCH ARTICLE - ELECTRICAL ENGINEERING

An Improved Space Vector Pulse Width Modulation for Nine-Level Asymmetric Cascaded H-Bridge Three-Phase Inverter

Busireddy Hemanth Kumar[1] · Makarand Mohankumar Lokhande[1] · Karasani Raghavendra Reddy[2] · Vijay Bhanuji Borghate[1]

Received: 11 August 2017 / Accepted: 3 October 2018 / Published online: 12 October 2018

Abstract
This paper presents an improved space vector pulse width modulation (SVPWM) for nine-level cascaded H-bridge inverter with unequal DC voltage sources. This technique is based on the use of 60° spaced *r*–*s* coordinate system to achieve SVPWM of multilevel three-phase inverter. In order to realize nine-level inverter, conventional SVPWM requires 1296 lookup tables, which is difficult to realize in the form of lookup tables, but the proposed technique does not require any lookup tables in the process of SVPWM realization, and it is generalized algorithm for any inverter levels. Hence, the system memory requirement is very less. The proposed modulation technique improves the nature of inverter output voltage and its total harmonic distortion value. Simulation results have been carried out using MATLAB/SIMULINK software tool. A comparative analysis is performed with classical pulse width modulation (PWM) techniques like sinusoidal PWM and third harmonic injection PWM at different modulation indices. To validate the simulation results and to confirm the practicality of the proposed control algorithm, experimental verification has been done.

Keywords Cascaded H-bridge (CHB) · Space vector pulse width modulation (SVPWM) · Asymmetric · Harmonic distortion · Nine-level inverter

1 Introduction

The augmented interest in multilevel inverter (MLI) is perhaps owing to the fact that the output waveforms of the converter are greatly enhanced compared to the two-level converter ideas. Various other advantages obtained from MLI are improved voltage rating of converter owing to the chain link of the power devices, lower harmonic content in the converter output waveforms with reduced dimension of the filters, reduction in common mode voltage of inverter and reduced switching frequency for the equal harmonic distortion value in the converter output. Especially for drive applications [1] in large and medium power range, multilevel converters give a superior power quality including an improved power factor, lesser dielectric stress on the motor insulation and small harmonic content with lower eddy current losses [2].

Multilevel inverter (MLI) can also be used for applications like industrial motor drives, FACTS and traction drive system. Mainly in the literature, three different multilevel converter topologies are neutral point clamped (diode clamped) [3], capacitor clamped (flying capacitor) [4] and cascaded H-bridge (CHB) MLI [5]. Among several MLI topologies, the CHB multilevel inverter is suitable for most of the applications. The advantages of the CHB converter over clamped converter are no extra diodes and capacitors used in CHB and modular in structure. Also, CHB has capability to control single-phase output individually, etc. The separate DC source modular structure topologies are recommended for renewable energy applications [6,7].

✉ Busireddy Hemanth Kumar
hemub09@gmail.com

Makarand Mohankumar Lokhande
makarand.lokhande@gmail.com

Karasani Raghavendra Reddy
raghu.vnitnagpur@gmail.com

Vijay Bhanuji Borghate
vijay_borghtae@rediffmail.com

[1] Electrical Engineering Department, Visvesvaraya National Institute of Technology, Nagpur 440010, India

[2] Electrical Engineering Department, Sreenidhi Institute of Science and Technology, Hyderabad, Telangana 501301, India

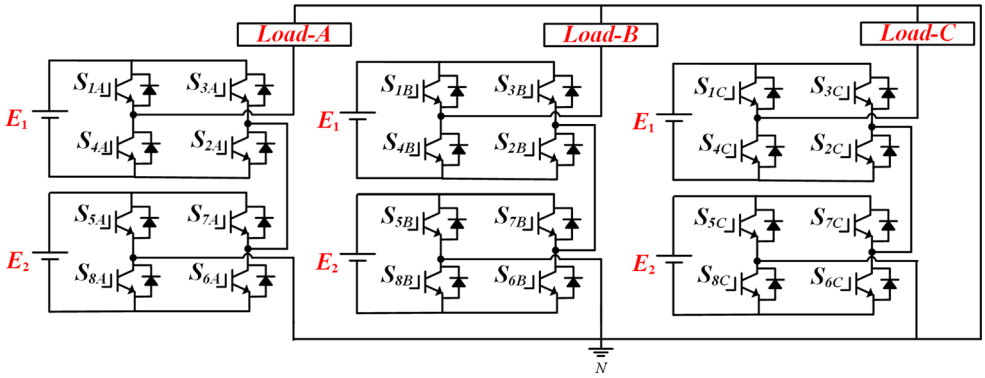

Fig. 1 Three-phase cascaded H-bridge (CHB) inverter

Table 1 Switching states for nine-level inverter

S_{1A}	S_{2A}	S_{3A}	S_{4A}	S_{5A}	S_{6A}	S_{7A}	S_{8A}	Voltage level
ON	ON	OFF	OFF	ON	ON	OFF	OFF	4E
OFF	ON	OFF	ON	ON	ON	OFF	OFF	3E
OFF	OFF	ON	ON	ON	ON	OFF	OFF	2E
ON	ON	OFF	OFF	OFF	ON	OFF	ON	E
OFF	ON	OFF	ON	OFF	ON	OFF	ON	0
OFF	OFF	ON	ON	OFF	ON	OFF	ON	$-E$
ON	ON	OFF	OFF	OFF	OFF	ON	ON	$-2E$
OFF	ON	OFF	ON	OFF	OFF	ON	ON	$-3E$
OFF	OFF	ON	ON	OFF	OFF	ON	ON	$-4E$

The CHB inverter can operate in asymmetric and symmetric modes. Symmetric CHB uses a number of switches compared with asymmetric CHB to get the same number of output voltage levels. Suppose in a single phase having n-H-bridges ($n \geq 2$), the number of per phase voltage levels if all DC sources are same (symmetric mode) is 2n+1, if DC sources are in the ratio of 1:2:4:…: 2n-2 (binary), then the number of per phase voltage levels is $2^{2n+1} - 1$, and if DC sources are in the ratio of 1:3:6:…: 3n-3 (trinary), then the number of per phase voltage levels is 3^n. The circuit diagram for three-phase cascaded H-bridge inverter is shown in Fig. 1. The switching logic for nine-level for CHB inverter operating in asymmetric mode is given in Table 1.

To control these power electronic converters, a better modulation control strategy is required. A lot of modulation control schemes [8,9] have been introduced to control CHB MLI: space vector modulation (SVM) method and sinusoidal pulse width modulation (SPWM) [10]. In the last few years, so many SPWM and SVM techniques are used to control voltage source converter. Compared with SPWM, SVM technique provides better DC bus utilization and has the tendency to minimize switching loss by proper selection of switching states. As a consequence, SVM scheme remains an accepted option for applications. The SVM realization for two-level VSI is an established method, though applying the same scheme to the MLIs is difficult. Actually, finding a new simple SVM technique for multilevel inverter is a significant area in the research point of view in the recent years.

Implementation of SVM requires mainly identifying the location of V_{ref} in which sector lies, selecting three nearest space vectors with respect to V_{ref} location followed by computation of dwell times and then producing gating pulses to the inverter by selecting optimum switching states. The SVM technique realization using a lookup table approach is complex to realize multilevel inverter. A simplified SVPWM method is presented in [11] on three-level inverter, but it becomes complex with the increase in levels of the inverter. In [12–14], proposed techniques are based on reduction in number of two-level hexagons for MLIs like five- and seven-level inverter and the drawback of this method is it requires 3D lookup tables, and a series technique on space vector modulation is presented in [15] on 13-level CHB inverter. A modified SVPWM for nine-level inverter is presented in [16,17], based on decomposition of higher-level hexagons into lower-level hexagons with lookup tables. The complexity of this method is increasing with the increase in the inverter levels. So, it is not the generalized SVPWM algorithm. In [18] and [19], SVM scheme is presented on two-level inverter by selecting a suitable switching sequence based on reference voltage and its angle, line current ripple and switching losses are minimized in motor drives. A sigma–delta-based PWM approach in [20] is presented on three-level inverter by cascading two

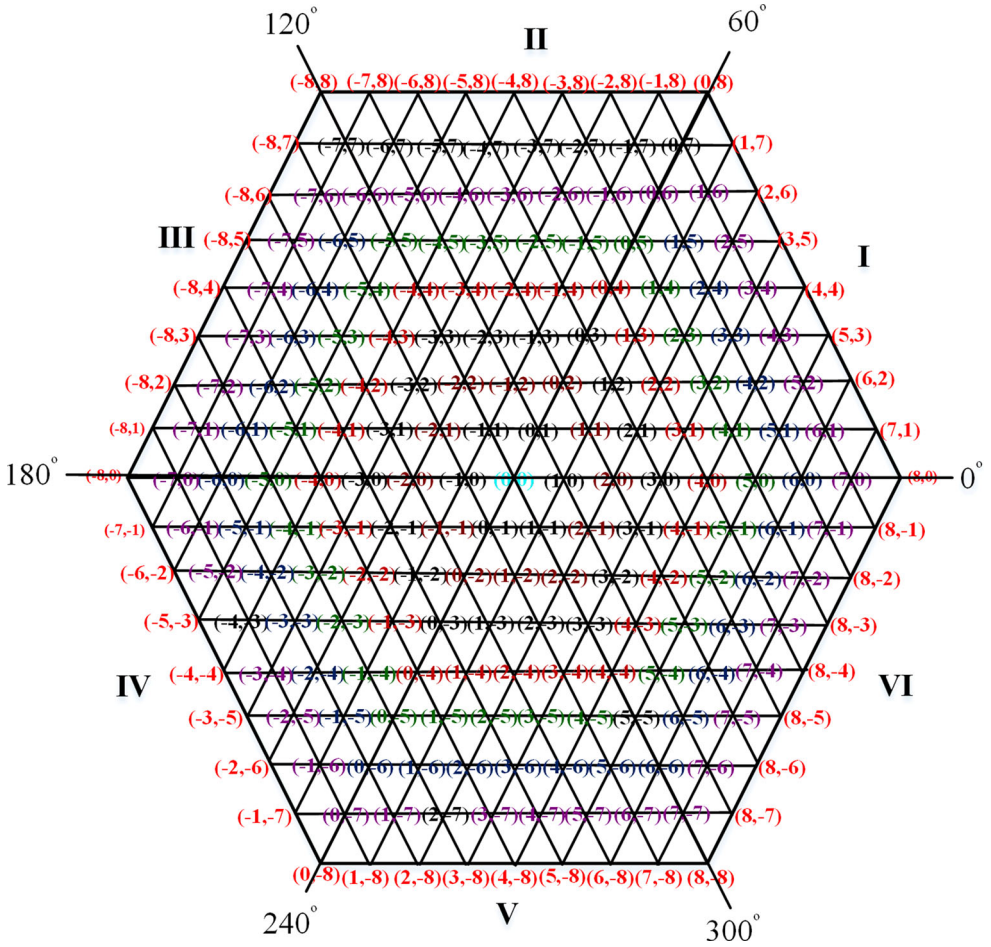

Fig. 2 Nine-level space vector diagram (SVD)

two-level inverters on IM. In [21] and [22], proposed mapped SVM hybrid techniques for MLI. They split the MLI into lower-level inverter groups. The drawback of this method is that redundant switching is not available.

For more than five levels, the conventional-based SVM techniques are hard to realize for different inverter topologies. Some adapted techniques were presented to realize SVM for any MLI. One such technique is a 60°-based SVM approach. In this paper, an improved SVPWM algorithm has been presented for multilevel inverter. Here, the proposed SVPWM method is explained for nine-level asymmetric CHB inverter. The presented method minimizes the complexity and no need of any look up table to implement SVPWM without affecting the output voltage profile. Simulations for nine-level asymmetric CHB inverter are compared with the THIPWM and SPWM at different modulation indices and validated with experimental results. Simulation and experimental results for dynamic variation in M value on nine-level CHB are presented.

2 Proposed SVPWM Technique

Generally for $(N + 1)$-level CHB, multilevel inverter has a total of $(N + 1)^3$ inverter switching states. It has N layers and $6N^2$ triangles in the space vector diagram (SVD). For nine-level inverter has 729 switching states. It has eight layers and 512 triangles in SVD. Figure 2 shows the nine-level inverter space vector diagram (SVD) in terms of r–s coordinate system.

2.1 The *r*–*s* Coordinate Axis System

For the generation of reference voltage V_{ref}, initially it is required to transform from three-phase quantity (a–b–c) to two-phase quantity (d–q).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & -1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}, \tag{1}$$

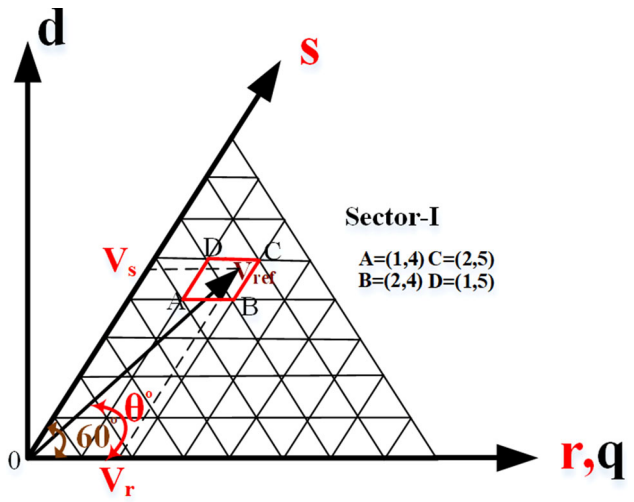

Fig. 3 Decomposing of V_{ref} in sector I in r–s coordinate axis system

where $V_{a,}\, V_b$ and V_c are phase variables

$$\overline{V}_{\text{ref}} = \overline{V}_d + j\overline{V}_q. \tag{2}$$

Figure 3 depicts the decomposition of V_{ref} into 60° spaced r–s coordinate system. For a $(N+1)$-level inverter, components of V_r and V_s are mathematically expressed as

$$\begin{aligned} V_r &= \frac{2NM}{3}\sin(60-\theta), \\ V_s &= \frac{2NM}{3}\sin(\theta), \end{aligned} \tag{3}$$

where M is modulating index and θ is the angle made by V_{ref} with respect to r-axis

$$M = \frac{\sqrt{3}V_{\text{ref}}}{V_{dc}}, \tag{4}$$

where V_{dc} is the DC bus voltage of first H-bridge cell (E_1)

The benefit of using this r–s transformation is that every space vector is having numeral coordinates with no redundancies in space vectors.

2.2 Determination of the Three Nearest Space Vectors (TNSVs)

The decomposition of reference vector in the r–s system and r–s axis along with d–q axis system is shown in Fig. 3. The (r, s) are the space vectors in r–s plane and are expressed in terms of components V_r and V_s as

$$\begin{aligned} r &= \text{floor}(V_r), \\ s &= \text{floor}(V_s). \end{aligned} \tag{5}$$

The selection of three nearest space vectors (r_1, s_1), (r_2, s_2) and (r_3, s_3) is done as follows

$$\begin{aligned} &\text{when } (V_r + V_s) \le (r + s + 1) \text{ then TNSVs are} \\ &\qquad (r_1, s_1) = (r, s), \\ &\qquad (r_2, s_2) = (r, s+1), \\ &\qquad (r_3, s_3) = (r+1, s), \end{aligned} \tag{6}$$

$$\begin{aligned} &\text{when } (V_r + V_s) > (r + s + 1) \text{ then TNSVs are} \\ &\qquad (r_1, s_1) = (r, s+1), \\ &\qquad (r_2, s_2) = (r+1, s), \\ &\qquad (r_3, s_3) = (r+1, s+1). \end{aligned} \tag{7}$$

The mathematical interpretation of calculating TNSVs Eqs. (6) and (7) is discussed by considering the V_{ref} location as shown in Fig. 2. Let the components obtained from Eq. (3) for an instance in (r, s) space are $V_r = 1.8$ and $V_s = 4.8$. Then from Eq. (5) the space vector $(r, s) = (1, 4)$; from Eq. (7), the TNSVs are $D = (r_{1,}s_1) = (1, 5)$, $B = (r_{2,}s_2) = (2, 4)$ and $C = (r_{3,}s_3) = (2, 5)$.

The above method is very simple to determine the nearest three vertices of a triangle, i.e., TNSVs based on V_{ref} location on r–s plane. If $(V_r + V_s) > N$, this is the case of over

Table 2 Number of switching states based on $(r + s)$ value

$(r + s)$ Value	Switching states	Example
0	9	(0,0): [4,4,4] [3,3,3] [2,2,2,] [1,1,1,] [0,0,0][−1,−1,−1] [−2,−−2,−2] [−3,−3,−3] [−4,−4,−4]
1	8	(1,0): [4,3,3,] [3,2,2,] [2,1,1,] [1,0,0,] [0,−1,−1] [−1,−2,−2] [−2,−3,−3] [−3,−4,−4]
2	7	(2,0): [4,2,2,] [3,1,1] [2,0,0] [1,−1,−1] [0,−2,−2] [−1,−3,−3] [−2,−4,−4]
3	6	(3,0): [4,1,1] [3,0,0,] [2,−1,−1] [1,−2,−2] [0,−3,−3] [−1,−4,−4]
4	5	(4,0): [4,0,0] [3,−1,−1] [2,−2,−2] [1,−3,−3] [0,−4,−4]
5	4	(5,0): [4,−1,−1] [3,−2,−2] [2,−3,−3] [1,−4,−4]
6	3	(6,0): [4,−2,−2] [3,−3,−3] [2,−4,−4]
7	2	(7,0): [4,−3,−3] [3,−4,−4]
8	1	(8,0): [4,−4,−4]

Table 3 Correlation between switching states in different sectors

Sector no.	Phase A	Phase B	Phase C
I	S_a	S_b	S_c
II	$-S_b$	$-S_c$	$-S_a$
III	S_c	S_a	S_b
IV	$-S_a$	$-S_b$	$-S_c$
V	S_b	S_c	S_a
VI	$-S_c$	$-S_a$	$-S_b$

modulation. In this case, the original V_r and V_s values are multiplied by a factor $N/(V_r + V_s)$ obtained resultant values are considered as new V_r and V_s and then consequent steps are same as normal SVM.

2.3 Dwell Time Calculations

The calculation of dwell times of each space vector is simple. For a reference vector (V_{ref}), the TNSVs are (r_1, s_1), (r_2, s_2) and (r_3, s_3) and their corresponding dwell times are t_1, t_2 and t_3, respectively. These are based on volt-time balancing as follows:

$$\begin{aligned} r_1t_1 + r_2t_2 + r_3t_3 &= V_rT_s, \\ s_1t_1 + s_2t_2 + s_3t_3 &= V_sT_s, \\ t_1 + t_2 + t_3 &= T_s, \end{aligned} \tag{8}$$

where T_s is sampling period. There is no need to calculate 3x3 inverse matrixes to obtain dwell times. Let us consider, c= $(r_1s_2 + r_2s_3 + r_3s_1) - (r_1s_3 + r_2s_1 + r_3s_2)$ then dwell

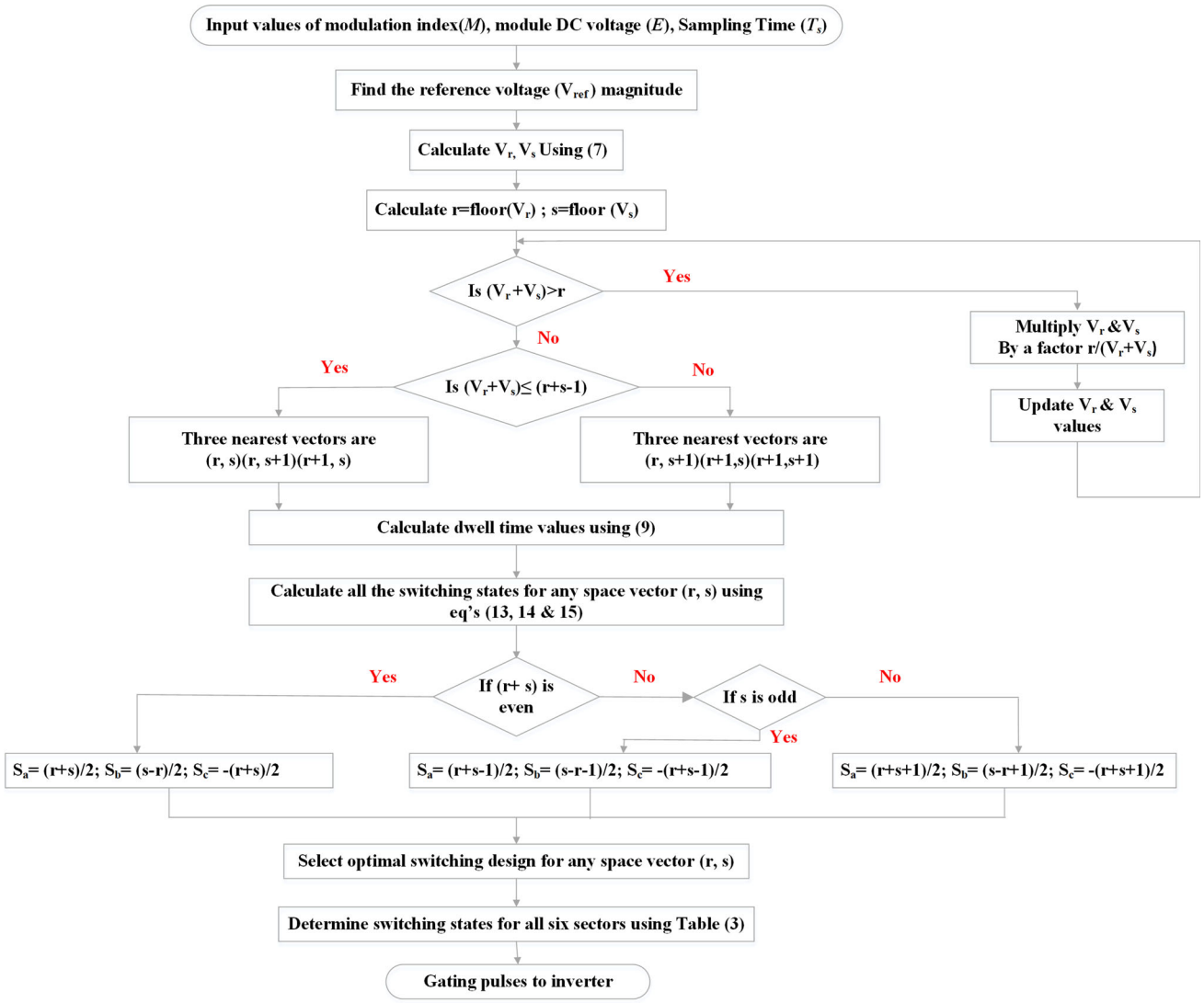

Fig. 4 Flowchart of the proposed algorithm

Table 4 Simulation parameters

S. no	Parameter	Value
1	DC voltage (E_1)	60 V
2	DC voltage (E_2)	180 V
3	Resistive load (R)	110 Ω/ph
4	Inductive load (L)	120 mH ($X_L = 37.68\,\Omega$)
5	Sampling time (T_s)	2100 Hz
Three-phase IM (1 HP)	Stator resistance (R_s)	14.05 Ω
	Stator inductance (L_s)	0.76744 H
	Rotor resistance (R_r)	8.3 Ω
	Rotor inductance (L_r)	0.76744 H
	Mutual inductance (L_m)	0.724 H
	Rotor inertia (J)	0.0088 Kg m^2
	Friction coefficient (B)	0.0001
	Number of poles (P)	4

times can be calculated as follows

$$\begin{aligned} t_1 &= ((r_2 s_3 + r_3 s_3 + V_r s_2) - (r_1 s_3 + r_3 s_2 + V_r s_3))/c, \\ t_2 &= ((r_1 V_s + r_3 s_1 + V_r s_3) - (r_1 s_3 + r_3 s_1 + V_r s_1))/c, \\ t_3 &= ((r_1 s_2 + r_2 V_s + V_r s_1) - (r_1 V_s + r_2 s_1 + V_r s_2))/c. \end{aligned} \tag{9}$$

2.4 Relationship Between Space Vectors (SV) and Switching States

In multilevel inverters, every space vector (r, s) is represented by more than one switching states. For an illustration of $(N + 1)$ level inverter, the number of possible switching states for a space vector (r, s) can be calculated as

$$N_{sw} = N - (r + s) + 1. \tag{10}$$

The maximum number of possible switching instants for a space vector (r, s) is given in Table 2. In general, for an SV (r, s) all the inverter switching states are found as follows for phase a.

$$S_a = \begin{cases} (r+s) - (N/2) \\ (r+s) - (N/2) + 1 \\ (r+s) - (N/2) + 2 \\ \vdots \\ N/2. \end{cases} \tag{11}$$

Similarly, inverter switching states for phase b and phase c are

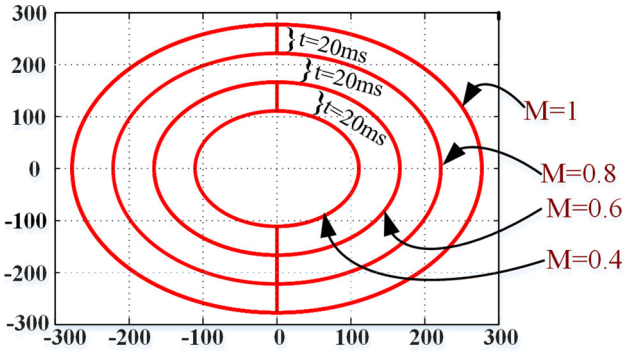

Fig. 5 The trace of V_{ref} for dynamic changes in M value

$$\begin{aligned} S_b &= S_a - r, \\ S_c &= S_b - s = S_a - (r + s). \end{aligned} \tag{12}$$

For instance, space vector (1,0) has eight switching states, such as [4,3,3,] [3,2,2,] [2,1,1,] [1,0,0,] [0,−1,−1] [−1,−2,−2] [−2,−3,−3] [−3,−4,−4]. Any switching instants in the above instance give the same phase angle and magnitude of output voltage. As CHB inverter level increases, the number of redundant switching instants to a space vector (r, s) increases.

2.5 Determination of Switching States

For any space vector (r, s): Category I: If the sum of r and s value is an even number, switching state can be expressed as

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \begin{bmatrix} (r+s)/2 \\ (s-r)/2 \\ -(r+s)/2 \end{bmatrix}. \tag{13}$$

Category II: If the sum of r and s values is an odd quantity and s is an odd quantity, the switching state can be expressed as

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \begin{bmatrix} (r+s-1)/2 \\ (s-r-1)/2 \\ (-(r+s+1)/2 \end{bmatrix}. \tag{14}$$

Category III: If the sum of $r$and s values is an odd quantity and $r$is odd quantity, the switching states are obtained as

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \begin{bmatrix} (r+s+1)/2 \\ (s-r+1)/2 \\ (-(r+s-1)/2 \end{bmatrix}. \tag{15}$$

2.6 Switching Sequence Design

To decrease the number of switching instants as per sampling period, a clever switching sequence has to be designed

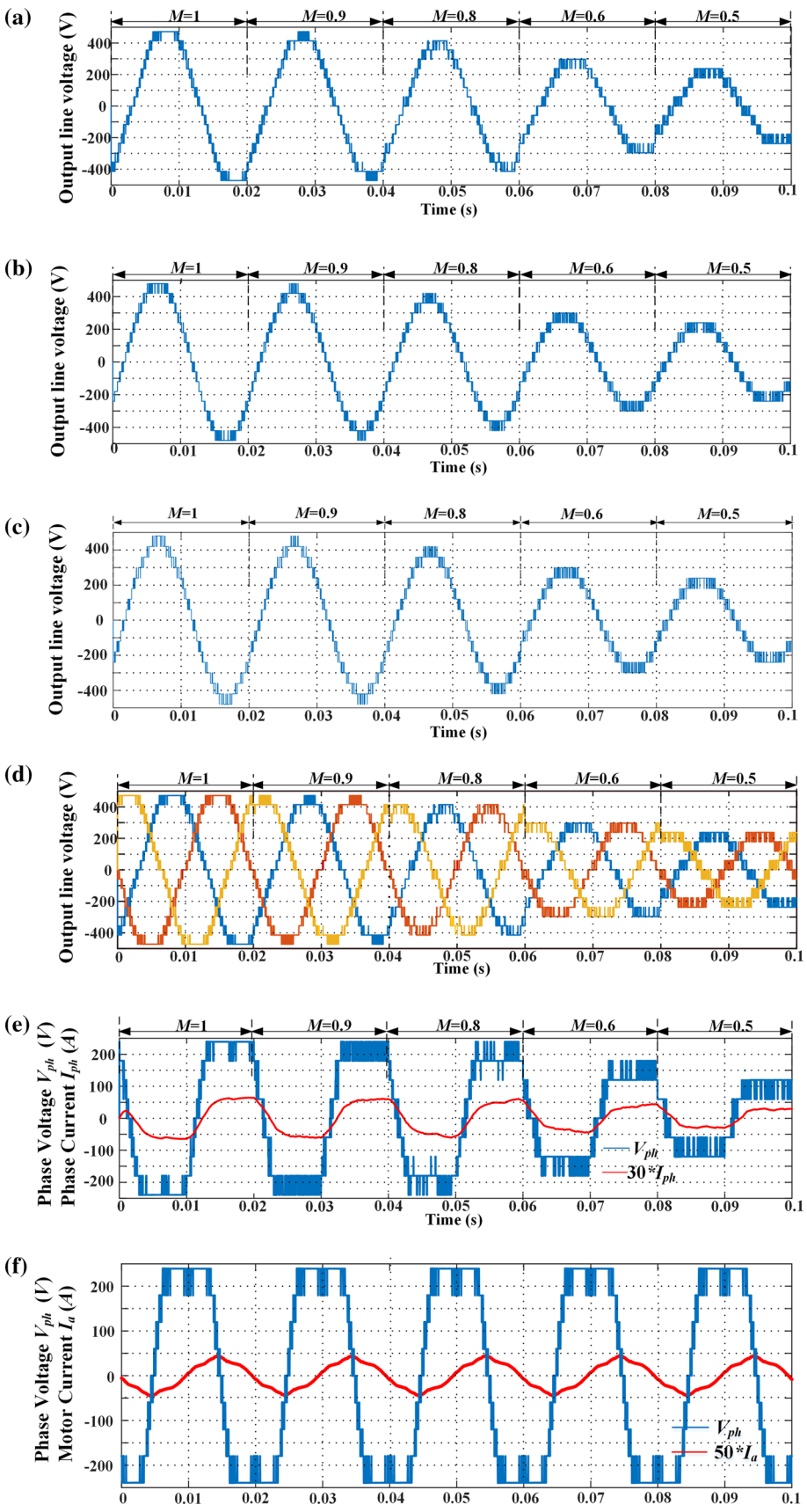

Fig. 6 Asymmetric mode nine-level inverter simulation results. **a** Line voltage using SPWM technique, **b** line voltage using THIPWM technique, **c** line voltage using proposed SVPWM technique, **d** three-phase line voltage using proposed SVPWM technique, **e** phase voltage and phase current using proposed SVPWM technique for RL load and **f** phase voltage and phase current using proposed SVPWM technique for IM load

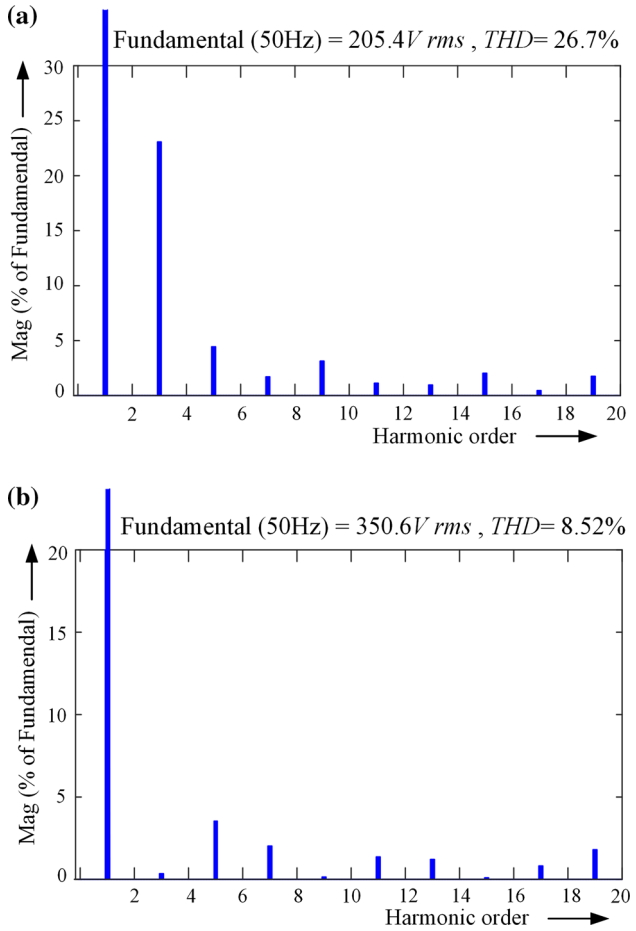

Fig. 7 Frequency spectra at unity modulation index using proposed SVPWM technique: **a** phase voltage and **b** line voltage

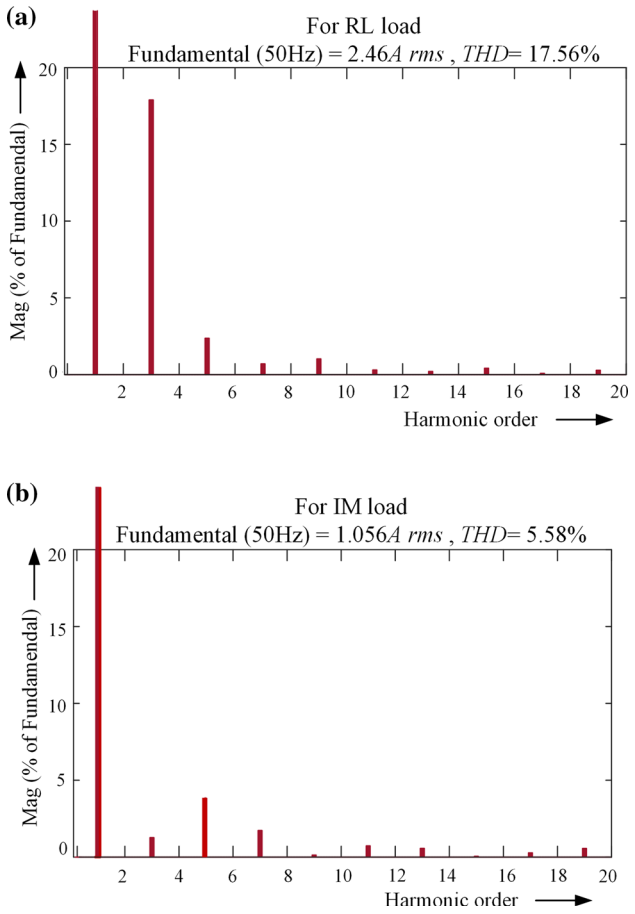

Fig. 8 Frequency spectra of load current at unity modulation index using proposed SVPWM technique: **a** RL load and **b** induction motor load

in SVM, which means there is only one voltage level transition when it moves from one switching instant to another switching instant. Here, cascaded H-bridge inverter is used, so there is no need of balancing the capacitors as like to the neutral point clamped inverters with the help of redundant switching states. Let us consider when reference vector V_{ref} lies in a triangle with (r_1, s_1) (r_2, s_2) and (r_3, s_3) which are the vertices (SVs) of a triangle, then based on the value of (r_1, s_1), seven-segment switching sequence is designed for the $V_{ref.}$ Let us consider, if the SV (r_1, s_1) belongs to category I, then switching sequence is as follows:

$$
\begin{aligned}
&(r_3, s_3) \times t_0/4 \rightarrow (r_1, s_1) \times t_1/2 \\
&\rightarrow (r_2, s_2) \times t_2/2 \rightarrow (r_3, s_3) \times t_0/2 \\
&\rightarrow (r_2, s_2) \times t_2/2 \rightarrow (r_1, s_1) \times t_1/2 \\
&\rightarrow (r_3, s_3) \times t_0/4.
\end{aligned}
$$

If SV (r_1, s_1) belongs to category II, then switching sequence is as follows:

$$
\begin{aligned}
&(r_1, s_1) \times t_0/4 \rightarrow (r_3, s_3) \times t_1/2 \\
&\rightarrow (r_2, s_2) \times t_2/2 \rightarrow (r_1, s_1) \times t_0/2 \\
&\rightarrow (r_2, s_2) \times t_2/2 \rightarrow (r_3, s_3) \times t_1/2 \\
&\rightarrow (r_1, s_1) \times t_0/4.
\end{aligned}
$$

If SV (r_1, s_1) belongs to category III, then switching sequence is as follows:

$$
\begin{aligned}
&(r_1, s_1) \times t_0/4 \rightarrow (r_2, s_2) \times t_1/2 \\
&\rightarrow (r_3, s_3) \times t_2/2 \rightarrow (r_1, s_1) \times t_0/2 \\
&\rightarrow (r_3, s_3) \times t_2/2 \rightarrow (r_2, s_2) \times t_1/2 \\
&\rightarrow (r_1, s_1) \times t_0/4.
\end{aligned}
$$

Based on correlation between switching states in different sectors given in Table 3, the switching instants for different sectors are to be selected. Hence, it is very easy to design the switching pattern for any reference vector V_{ref} in the $(N+1)$-level SVD. The flowchart for the presented improved SVPWM technique is shown in Fig. 4.

Table 5 Comparison of THD and RMS value of nine-level inverter line voltage

Modulation index (M)	SPWM		THIPWM		SVPWM (proposed)	
	THD%	V_1 (RMS)	THD%	V_1 (RMS)	THD%	V_1 (RMS)
1.0	9.78	293.8	8.68	338.9	8.52	350.6
0.9	10.03	264.4	9.81	305.5	9.13	323.2
0.8	10.75	235.1	10.07	271.5	9.30	294.2
0.6	13.26	176.2	12.30	230.6	10.70	217.2
0.4	21.68	117.5	17.31	135.7	16.38	137.5
0.2	42.16	58.72	38.43	67.77	41.73	58.04

Table 6 Comparison of output line voltage THD at $M = 1.0$ of different sampling frequencies using proposed technique and techniques presented in [13–16]

Inverter	Modulation scheme	Sampling frequency 600 Hz	Sampling frequency 900 Hz	Sampling frequency 2100 Hz
Nine levels	MSVPWM [16]	9.12	8.91	8.65
	Proposed SVM	8.97	8.74	8.52
Seven levels	SSVM [13]	12.24	11.92	12.71
	FSVM [13]	17.08	16.24	13.44
	g–h Coordinate system [14]	12.76	12.4	12.05
	Series SVM [15]	13.28	13.49	–
	Proposed SVM	11.76	11.24	10.02
Five levels	SSVM [12]	19.4	18.53	20.48
	FSVM [12]	21.09	20.89	20.69
	g–h Coordinate system [14]	18.69	18.02	18.4
	Series SVM [15]	20.82	20.14	–
	Proposed SVM	18.62	18.04	18.20

Table 7 Phase current THD for different values of modulation index

Modulation index (M)	Phase current THD%
1.0	17.56
0.9	19.58
0.8	20.27
0.6	23.65
0.5	26.63

Table 8 Switching losses for three different modulation schemes

Modulation scheme	Switching losses (W)
SPWM	5.86
THIPWM	6.33
SVPWM (proposed)	5.21

3 Results and Discussion

3.1 Simulation Results

Simulation results for proposed improved SVM are shown for nine-level CHB inverter at different M values from 0.4 to 1.0, and the results are compared with the results presented in [13–16], SPWM and THPWM schemes. The sampling frequency for simulation is 2.1 kHz. During asymmetric mode operation, first-bridge DC supply (E_1) is 60 V and for a second bridge, DC supply (E_2) is 180 V. A three-phase star-connected RL load is considered, whose values are 110Ω and 120 mH per phase. The parameters used for simulation are given in Table 4. The locus of reference voltage V_{ref} for variation of M value is shown in Fig. 5.

In dynamic variation of M, its value is kept constant for one fundamental cycle. Figure 6 shows the dynamic behavior of the inverter output voltage with different M values. The behavior of nine-level inverter line voltage with M varies from 1 to 0.4 by using SPWM, THIPWM and proposed SVPWM techniques which are shown in Fig. 6a–c, respec-

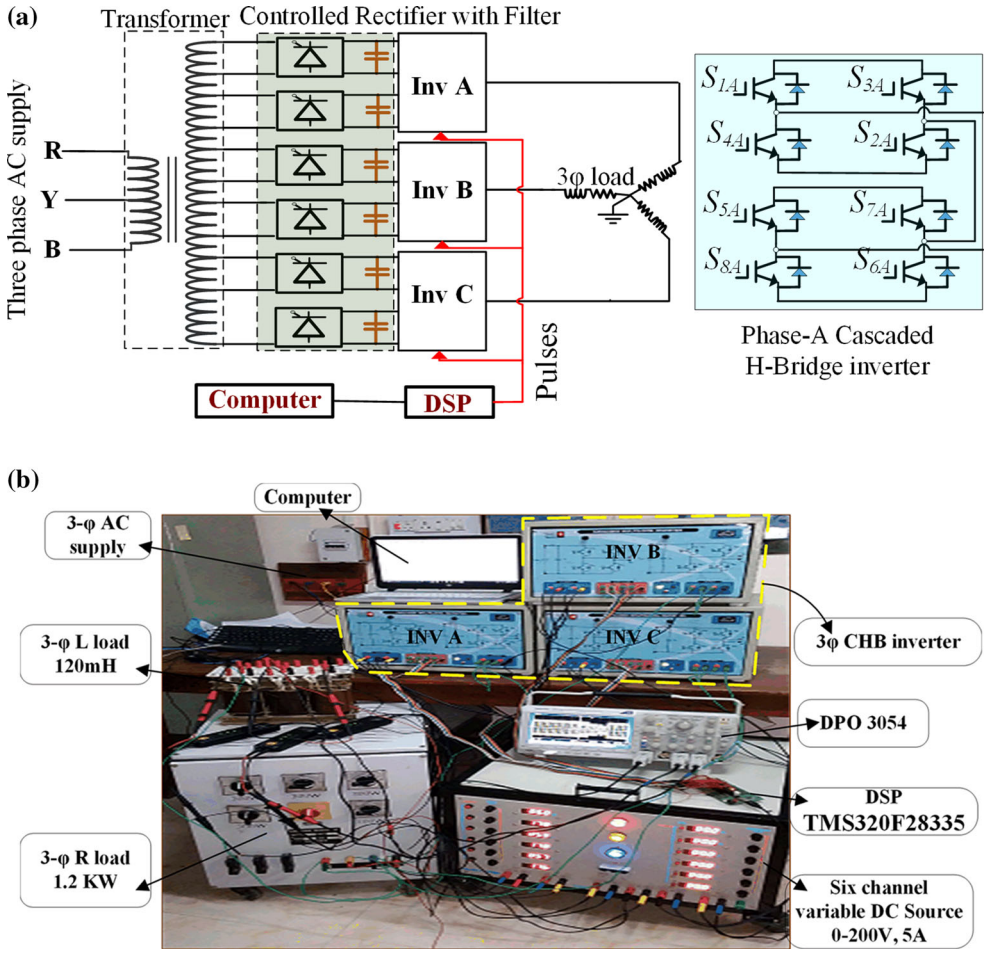

Fig. 9 Nine-level cascaded H-bridge inverter with DC sources: **a** schematic diagram and (b) prototype setup in the laboratory

tively. Figure 6d shows the nine-level three-phase line voltage at different values of M. Combined phase voltage and current for dynamic variation of the M with RL load and induction motor (IM) load are shown in Fig. 6e and f. The ratings of the IM are given in Table 4.

The harmonic spectra for the nine-level phase voltage and line voltage are shown in Fig. 7a and b, respectively. Similarly, the harmonic spectra of load current with RL load and IM load are shown in Fig. 8a and b. For all M values, the proposed SVM algorithm results show satisfactory performance. The harmonic distortion obtained for the proposed method is lower compared with THIPWM & SPWM schemes, and output voltage fundamental component of the proposed method is higher compared with THIPWM & SPWM schemes.

Table 5 shows the fundamental component and THD% of line voltage using SPWM, THIPWM and proposed SVPWM techniques at different modulation indices for nine-level inverter. The proposed r–s-based SVPWM algorithm sampled at 600 Hz and 900 Hz in MATLAB simulation at $M = 1.0$ for comparison of recently presented SVPWM techniques in literature is given in Table 6. Thus, the proposed SVM scheme compared fine with existing SVM techniques. Nine-level phase current THD% with different M values is given in Table 7; due to the third harmonic content in the phase voltage waveform, its harmonic distortion value is somewhat high. The switching losses are calculated by incorporating the switch characteristics in the thermal model of IGBT in MATLAB software from the datasheet [23]. Table 8 shows the inverter switching losses using SPWM, THIPWM and proposed SVPWM techniques. The proposed SVPWM scheme gives lower switching losses due to optimum switching sequence design based on the available redundant switching states.

4 Hardware Results

The schematic circuit diagram for nine-level cascaded H-bridge inverter is shown in Fig. 9a. The transformer has six secondary tapings and is exited by a three-phase AC supply. By using thyristor-based rectifier with capacitive filter, AC to DC power conversion has been done and then the six inde-

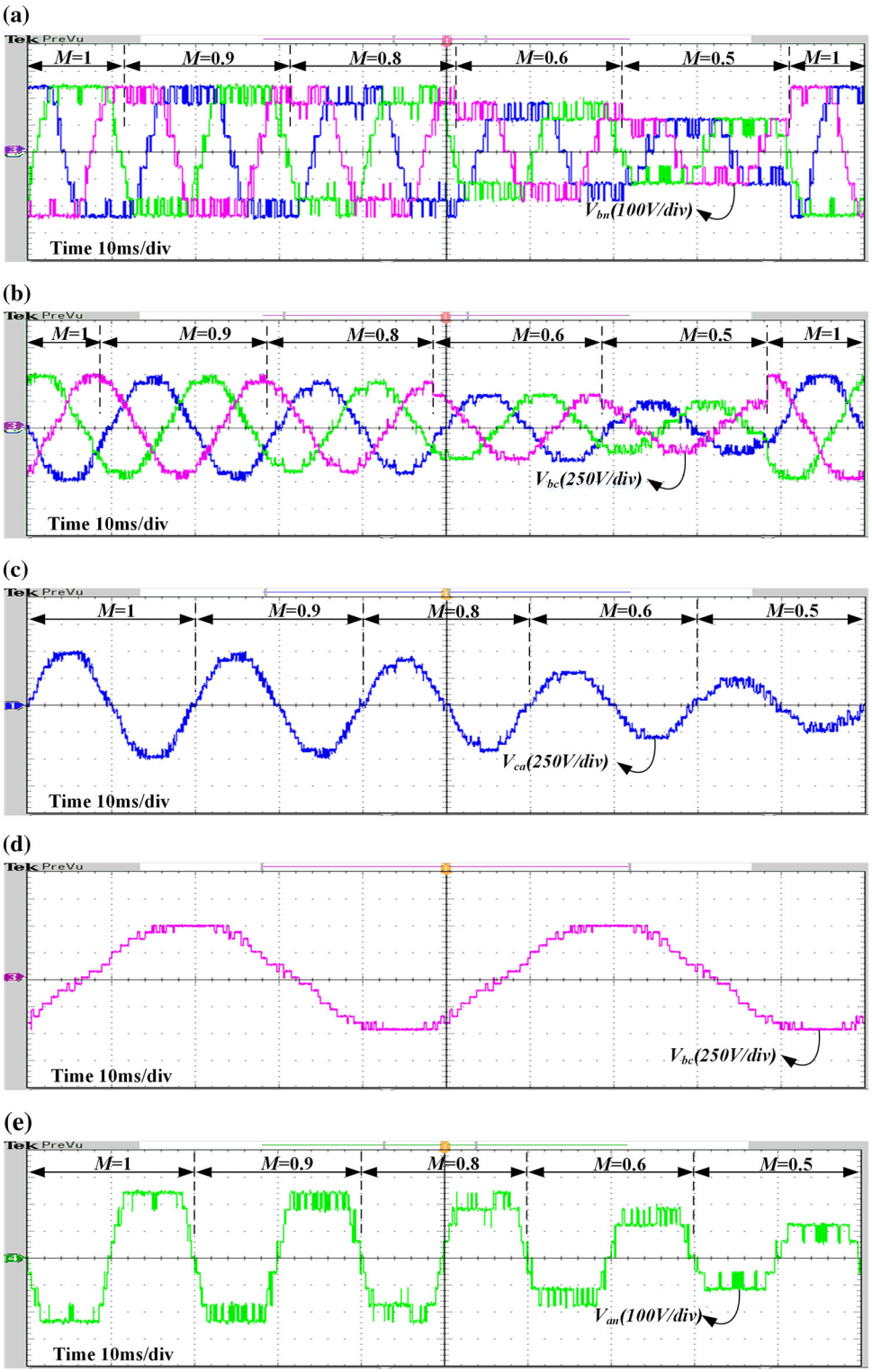

Fig. 10 Experimental results for asymmetric mode nine-level inverter: **a** three-phase voltage, **b** three-phase line voltage, **c** line voltage, **d** microscopic view of line voltage and **e** phase voltage

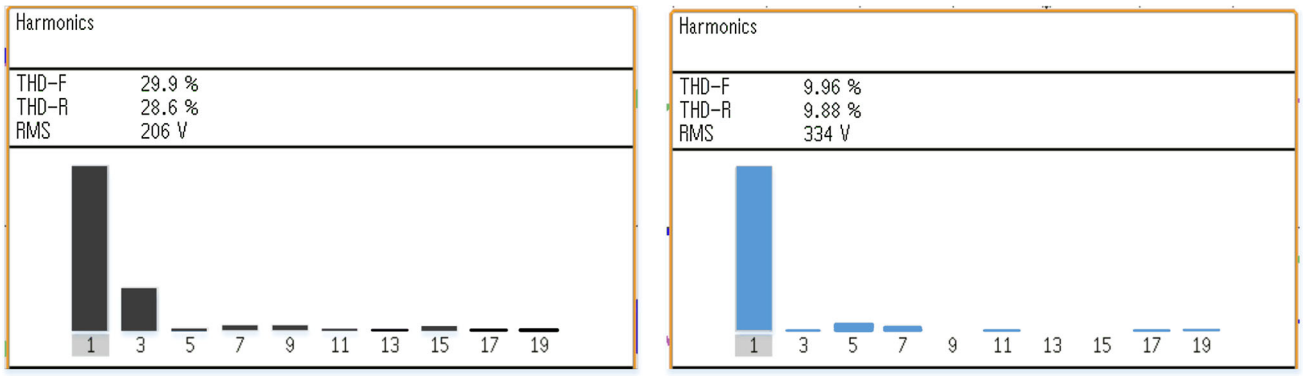

Fig. 11 Frequency spectra: **a** phase voltage and **b** line voltage

Table 9 Experimentally obtained THD value of line voltage for nine-level inverter

Modulation index (M)	Line voltage THD%
1.0	7.78
0.9	8.18
0.8	8.49
0.6	10.01

pendent variable DC sources are given to six H-bridges in the three-phase CHB inverter. To verify the simulation results, a three-phase CHB asymmetric nine-level inverter prototype has been set up in the laboratory, which is shown in Fig. 9b. Different parameters are considered as same as MATLAB simulation. The proposed SVPWM technique is developed with DSP TMS32F28335 platform. Real-time results for the prototype shown in Fig. 9b are presented in Fig. 9. Figure 10a and b shows a nine-level three-phase voltages and three-phase line voltages at different M values. The nine-level line voltage and its microscopic view at unity modulation index are shown in Fig. 10c and d. In Fig. 10d, it is clearly visible that waveform has 17 levels. Figure 10e shows the single-phase nine-level voltage at different modulation indices (M).

The harmonic spectrum of line voltage and phase voltage at unity modulation index for nine-level inverter is shown in

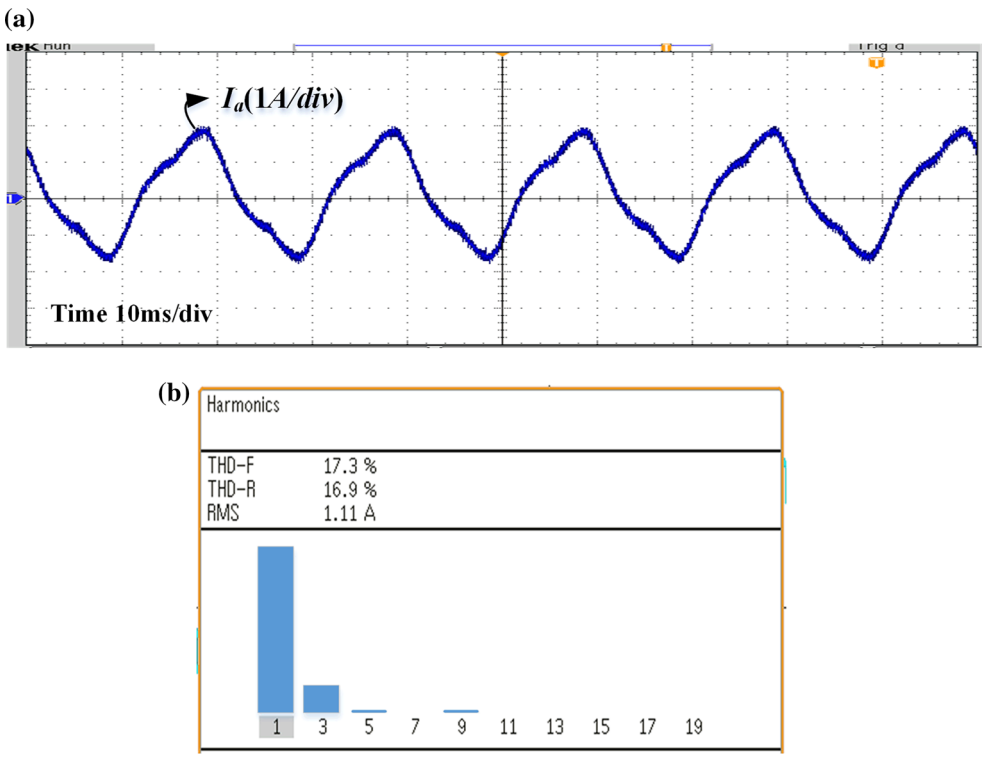

Fig. 12 Experimental results for asymmetric mode nine-level inverter with RL load: **a** load current waveform and **b** frequency spectra

Fig. 11a and b, respectively. The line voltage THD% values obtained at different modulation indices are given in Table 9. The load current waveform for nine-level inverter is shown in Fig. 12a, and its frequency spectrum is shown in Fig. 12b. Compared with simulation results, THD value obtained in experimental results is less, which is because the harmonic order considered for the simulation is infinity, whereas oscilloscope DPO 3054 is considered a maximum of 100th harmonic order for the calculation of output line voltage THD value.

5 Conclusion

In this paper, a new improved SVPWM algorithm is proposed. The proposed algorithm makes use of 60°-based *r*–*s* coordinate system. This method simplifies the identification of the triangle where the reference vector V_{ref} lies, finding of nearest three space vectors and their corresponding dwell time calculations. The proposed algorithm does not require any lookup tables. This method is easy to implement, gives minimum harmonic distortion in output voltage and can be generalized for any multilevel inverter. Simulation results for nine-level CHB inverter have been presented at the different modulation index values and compared with established SPWM & THIPWM schemes for validation. Experimental results are also shown for the presented algorithm and have been verified in real-time simulation system with DSP.

References

1. Rodríguez, J.; Bernet, S.; Wu, B.; Pontt, J.O.; Kouro, S.: Multilevel voltage-source-converter topologies for industrial medium-voltage drives. IEEE Trans. Ind. Electron. **54**(6), 2930–2945 (2007)
2. De, S.; Banerjee, D.; Siva Kumar, K.; Gopakumar, K.; Ramchand, R.; Patel, C.: Multilevel inverters for low-power application. IET Power Electron. **4**(4), 384–392 (2011)
3. Rodriguez, J.; Bernet, S.; Steimer, P.K.; Lizam, I.E.: A survey on neutral-point-clamped inverters. IEEE Trans. Ind. Appl. **57**(7), 2219–2230 (2010)
4. Huang, J.; Corzine, K.A.: Extended operation of flying capacitor multilevel inverters. IEEE Trans. Power Electron. **21**(1), 140–147 (2006)
5. Malinowski, M.; Gopakumar, K.; Rodriguez, J.; Perez, M.: A survey on cascaded multilevel inverters. IEEE Trans. Ind. Appl. **57**(7), 2197–2206 (2010)
6. Karasani, R.R.; Borghate, V.B.; Meshram, P.M.; Suryawanshi, H.M.; Sabyasachi, S.: A three phase hybrid cascaded modular multilevel inverter for renewable energy environment. IEEE Trans. Power Electron. **32**(2), 1070–1086 (2016)
7. Karasani, R.R.; Borghate, V.B.; Meshram, P.M.; Suryawanshi, H.M.: A modified switched-diode topology for cascaded multilevel inverters. J. Power Electron. **16**(5), 1706–1715 (2016)
8. Holmes, D.G.; Lipo, T.A.: Pulse Width Modulation for Power Converters: Principles and Practice. John Wiley & Sons, New York, USA (2003)
9. Holtz, J.: Pulse width modulation-a survey. IEEE Trans. Ind. Electron. **39**(5), 410–420 (1992)
10. Palanivel, P.; Dash, S.S.: Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques. IET Power Electron. **4**(8), 951–958 (2011)
11. Seo, J.H.; Choi, C.H.; Hyun, D.S.: A new simplified space vector PWM method for three-level inverters. IEEE Trans. Power Electron. **16**, 545–550 (2001)
12. Matsa, A.; Ahmed, I.; Chaudhari, M.A.: Optimized space vector pulse-width modulation technique for a five-level cascaded H-bridge inverter. J. Power Electron. **14**(5), 937–945 (2014)
13. Ahmed, I.; Borghate, V.B.: Simplified space vector modulation technique for seven-level cascaded H-bridge inverter. IET Power Electron. **7**(3), 604–613 (2014)
14. Ahmed, I.; Borghate, V.B.; Matsa, A.; Meshram, P.M.; Suryawanshi, H.M.; Chaudhari, M.A.: Simplified space vector modulation techniques for multilevel inverters. IEEE Trans. Power Electron. **31**(12), 8483–8499 (2016)
15. Rabinovici, R.; Baimel, D.; Tomasik, J.; Zuckerberger, A.: Series space vector modulation for multilevel cascaded H-bridge inverters. IET Power Electron. **3**(6), 843–857 (2010)
16. Hemanth Kumar, B.; Lokhande, M.M.; Karasani, R.R.; Borghate, V.B.: A modified space vector PWM approach for nine-level cascaded H-bridge inverter. Arab. J. Sci. Eng. (2018). https://doi.org/10.1007/s13369-018-3363-3
17. Hemanth Kumar, B.; Lokhande, M.M.: An enhanced space vector PWM for nine-level inverter employing single voltage source. IEEE Transportation Electrification Conference-India. 1–6 (2017) https://doi.org/10.1109/ITEC-India.2017.8333711
18. Prasad, J.S.S.; Narayanan, G.: Minimum switching loss pulse width modulation for reduced power conversion loss in reactive power compensators. IET Power Electron. **7**(3), 545–551 (2013)
19. Pavan Kumar Hari, V.S.S.; Narayanan, G.: Space-vector-based hybrid PWM technique to reduce line current distortion in induction motor drives. IET Power Electron. **5**(8), 1463–1471 (2012)
20. Jacob, B.; Baiju, M.R.: Simple multilevel inverter-based induction motor drive scheme using sigma-delta converter with space-vector quantiser. IET Power Electron. **5**(8), 1483–1490 (2012)
21. Massoud, A.M.; Finney, S.J.; Cruden, A.; Williams, B.W.: Mapped phase-shifted space vector modulation for multi-level voltage-source inverters. IET Power Electron. **1**(4), 622–636 (2007)
22. Massoud, A.M.; Finney, S.J.; Williams, B.W.: Mapped hybrid spaced vector modulation for multilevel cascaded-type voltage source inverters. IET Power Electron. **1**(3), 318–335 (2008)
23. SEMIKRON IGBT Modules SEMITRANS-2 datasheet, SEMIKRON Co. Ltd.