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RESEARCH ARTICLE - ELECTRICAL ENGINEERING

A 10-Bit Differential Ultra-Low-Power SAR ADC with an Enhanced MSB Capacitor-Split Switching Technique

Sreenivasulu Polineni[1] · M. S. Bhat[1] · Arulalan Rajan[1]

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Abstract
A fully differential energy-efficient switching scheme for binary-weighted capacitor digital-to-analog converter (DAC) is presented. It is observed that the proposed switching scheme reduces energy consumption of DAC by 97% and the capacitance area by 50% over the conventional ones. The effect of supply and common mode voltage variations on the linearity of successive approximation register (SAR) analog-to-digital converter (ADC) is reduced. Moreover, with this switching scheme, one can achieve the same dynamic range as the conventional one, with half the supply voltage as compared to the existing schemes. This makes the proposed switching method suitable for ultra-low-voltage SAR ADCs, which are widely used in biomedical applications. The proposed method is modelled using MATLAB. The results show that the nonlinearity (INL and DNL) caused by capacitor mismatch is reduced. The circuit-level implementation of 10-bit SAR ADC is simulated using UMC 90nm CMOS 1P9M process technology.

Keywords SAR ADC · Binary-weighted DAC · Capacitor · Switching technique · Input common mode range · Switching energy per conversion · Energy efficiency · Mismatch · INL · DNL

1 Introduction

Biomedical sensors and large-scale wireless sensor networks require moderate speed, moderate resolution as well as low-energy-consuming ADCs. State of the art suggests that SAR ADC is the most appropriate one for energy-efficient applications by virtue of its characteristics like conversion accuracy, ultra-low-power consumption, simple design and amenability for technology scaling. Basically, SAR ADC consists of a comparator block, feedback DAC and SAR control logic. Among these, the feedback DAC consumes more energy compared to the dynamic comparator and the digital control logic. In general, this feedback DAC is made up of two identical binary-weighted capacitor arrays in differential manner. The area and energy consumption of binary-weighted capacitive DAC scales exponentially with ADC resolution. Conventional binary-weighted capacitor array [1] has 2^{N+1} unit capacitances, where N is the resolution of ADC. On the other hand, conventional binary switching scheme is pronounced as inefficient, because most of the energy drawn from supply voltage is wasted, when the capacitors switch between V_{ref} and Gnd. Various switching schemes reported in the literature attempt to minimize the energy consumption as well as the capacitor spread.

The novel switching method proposed in [2] is found to reduce switching energy by 37.5% compared to the conventional architecture. In this, the MSB capacitor ($2^N C$) is split into sub-array (as $2^{N-1}C + 2^{N-2}C + \cdots + 2C + C + C$) and the charge is reused in subsequent cycles. The energy saving switching scheme proposed in [3] achieves 56% reduction by saving energy in first two cycles of conversion. Monotonic switching [4] came up with impressive energy efficiency of 81%. Further, several switching techniques reported in [5–9] claimed energy efficiency in the range of 87–96% by employing additional reference voltages. However, there is further scope for energy saving, which is discussed in the following sections.

✉ Sreenivasulu Polineni
ec15fv04.sreenivasulu@nitk.edu.in

M. S. Bhat
msbhat@ieee.org

Arulalan Rajan
perarulalan@gmail.com

[1] Department of Electronics and Communication Engineering, National Institute of Technology, Surathkal, Karnataka 575025, India

Some of the major drawbacks in the existing techniques are discussed here. Firstly, it is a known fact that the accuracy of voltage references determine the DAC linearity. However, the process, voltage, temperature (PVT)-independent reference voltages generation is complex and requires additional power and area. Secondly, the common mode voltage of differential DAC outputs (i.e. inputs of comparator) varies. The power consumption, nonlinearity and the design complexity of the comparator increase with input common mode voltage range (ICMR). Currently, SAR ADCs employ dynamic comparators [10] owing to their ultra low energy per conversion and simple architecture. Basically, as the common mode voltage decreases, the input transistors of the dynamic comparator operate at lower currents. This leads to longer decision time, i.e. comparator speed decreases because the output nodes charge and discharge at slower rates. This reduction in currents can be compensated by increasing transistor sizes. However, larger transistors introduce additional parasitics at all nodes. Hence, the comparator power consumption increases and the speed saturates.

The present work proposes a fully differential switching scheme using single reference voltage, which achieves DAC linearity with a constant common mode voltage. The proposed design incorporates simple SAR logic to minimize the design complexity and power consumption. Section 2 explains the working principle of the proposed switching method for binary-weighted DAC. Section 3 discusses the MATLAB modelling of the proposed scheme, and Sect. 4 discusses the circuit-level implementation of a 10-bit SAR ADC. Section 5 discusses the simulation results and comparison with existing schemes. Section 6 concludes the paper.

2 Enhanced MSB Capacitor Split Technique

The proposed switching scheme is based on fully differential MSB capacitor split technique using a single reference voltage V_{cm}. Flow chart in Fig. 1 illustrates the proposed SAR conversion method. The total capacitance required for proposed N-bit DAC is $2^N C$, and each differential node has $2^{N-1}C$, where C is unit capacitor. The value of this unit capacitance is decided by factors like noise and mismatch, depending on the required conversion precision, type of capacitor, fabrication process and technology. The circuit-level realization for 10-bit SAR ADC is shown in Fig. 2. As one can observe, the MSB capacitor (i.e. largest capacitor $2^{N-2}C$) at each node is split into array of binary-weighted capacitors (as $2^{N-3}C + 2^{N-4}C + \cdots + 2C + C + C$) to take advantage of MSB capacitor split technique [2].

In the proposed scheme, initially, the differential inputs are V_{ip} and V_{im} sampled only on LSB capacitor arrays of DACP and DACN respectively, by connecting in a fashion as shown in Fig. 2. At the time of start conversion, MSB capac-

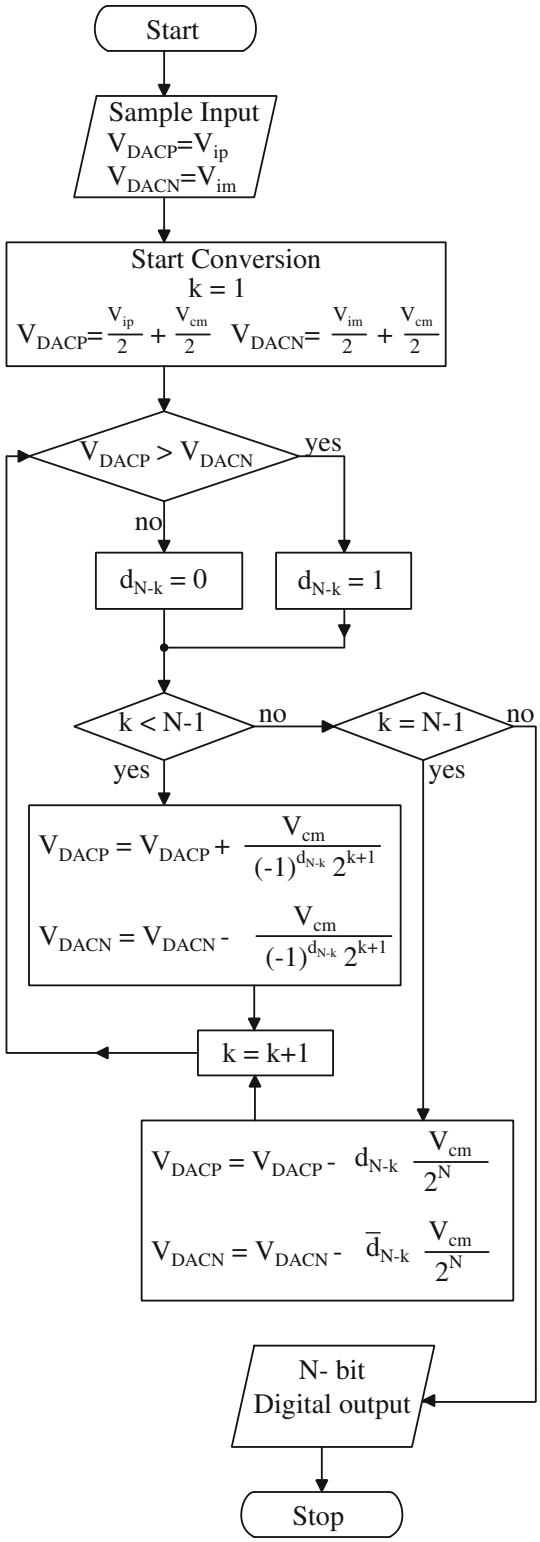

Fig. 1 Flow chart of proposed DAC conversion method

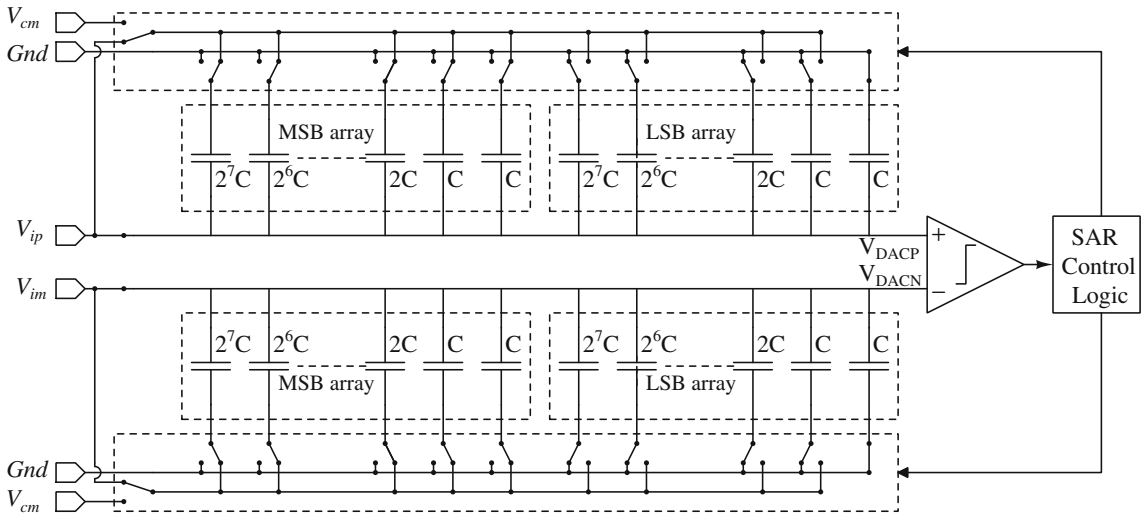

Fig. 2 Proposed 10-bit SAR ADC architecture

itor arrays ($2^{N-2}C$) of both DACP and DACN are connected to V_{cm}. As a result, the voltages on DACP and DACN are settled as shown in Eqs. 1 and 2 respectively

$$V_{\text{DACP}} = \frac{V_{\text{ip}}}{2} + \frac{V_{\text{cm}}}{2} \tag{1}$$

$$V_{\text{DACN}} = \frac{V_{\text{im}}}{2} + \frac{V_{\text{cm}}}{2}, \tag{2}$$

where V_{cm} is the common mode voltage of differential input signals V_{ip} and V_{im}. This division of input signals by a factor of two along with the differential comparison enables the use of V_{cm} as supply voltage for DACs. Moreover, the net charge drawn from supply voltage is zero. Thus, the energy consumed in the first switching step is zero as given by Eq. 4.

$$\begin{aligned}\Delta q &= \overbrace{2^{n-2}C\left(\frac{V_{\text{cm}}}{2} - \frac{V_{\text{ip}}}{2}\right)}^{q_{\text{DACP}}} \\ &\quad + \overbrace{2^{n-2}C\left(\frac{V_{\text{cm}}}{2} - \frac{V_{\text{im}}}{2}\right)}^{q_{\text{DACN}}} \\ &= 2^{n-2}C\left(V_{\text{cm}} - \frac{V_{\text{ip}} + V_{\text{im}}}{2}\right) \\ &= 0 \qquad \left(\because V_{\text{cm}} = \frac{V_{\text{ip}} + V_{\text{im}}}{2}\right)\end{aligned} \tag{3}$$

$$\therefore E_{1_{\text{st}}\text{cycle}} = \Delta q \cdot V_{\text{cm}} = 0. \tag{4}$$

The comparator output is

$$d_{N-1} = \begin{cases} 0 & \text{if } V_{\text{DACP}} \leq V_{\text{DACN}} \\ 1 & \text{otherwise} \end{cases}. \tag{5}$$

The next switching transition is controlled by comparator output d_{N-1}. If d_{N-1} is low, the capacitor $2^{N-3}C$ in DACP LSB sub-array switches to V_{cm} and the capacitor $2^{N-3}C$ in DACN MSB sub-array switches to Gnd. On the other hand, if d_{N-1} is high, the capacitor $2^{N-3}C$ in DACN LSB sub-array switches to V_{cm} and the capacitor $2^{N-3}C$ in DACP MSB sub-array switches to Gnd. This changes the voltages V_{DACP} and V_{DACN} in the opposite manner, by the same amount, such that the common mode voltage is constant.

$$V_{\text{DACP}} = \frac{V_{\text{ip}}}{2} + \frac{V_{\text{cm}}}{2} + (-1)^{d_{N-1}}\frac{V_{\text{cm}}}{4} \tag{6}$$

$$V_{\text{DACN}} = \frac{V_{\text{im}}}{2} + \frac{V_{\text{cm}}}{2} - (-1)^{d_{N-1}}\frac{V_{\text{cm}}}{4}. \tag{7}$$

Here, each DAC draws $2^{N-5}CV_{\text{cm}}$ charge from the supply voltage. Thus, the energy consumption in second cycle is given by

$$\begin{aligned}E_{2_{\text{nd}}\text{cycle}} &= 2.\left(2^{N-3}C\frac{V_{\text{cm}}}{4}\right)V_{\text{cm}} \\ &= 2^{N-6}CV_{\text{ref}}^2 \quad \left(\because V_{\text{cm}} = \frac{V_{\text{ref}}}{2}\right).\end{aligned} \tag{8}$$

The same process continues for subsequent cycles till the penultimate cycle, in which d_1 is determined. The proposed method uses terminating unit capacitor C in MSB array for determining LSB bit (d_0). If d_1 is low, the capacitor C in DACN alone switches to Gnd, else capacitor C in DACP switches to Gnd. As a result, the proposed switching method is able to achieve N-bit resolution by employing only $N-1$ bit DAC. Thus, this reduces the capacitor spread by a factor two. Figure 3 illustrates the proposed switching process throughout the conversion for all possible digital outputs,

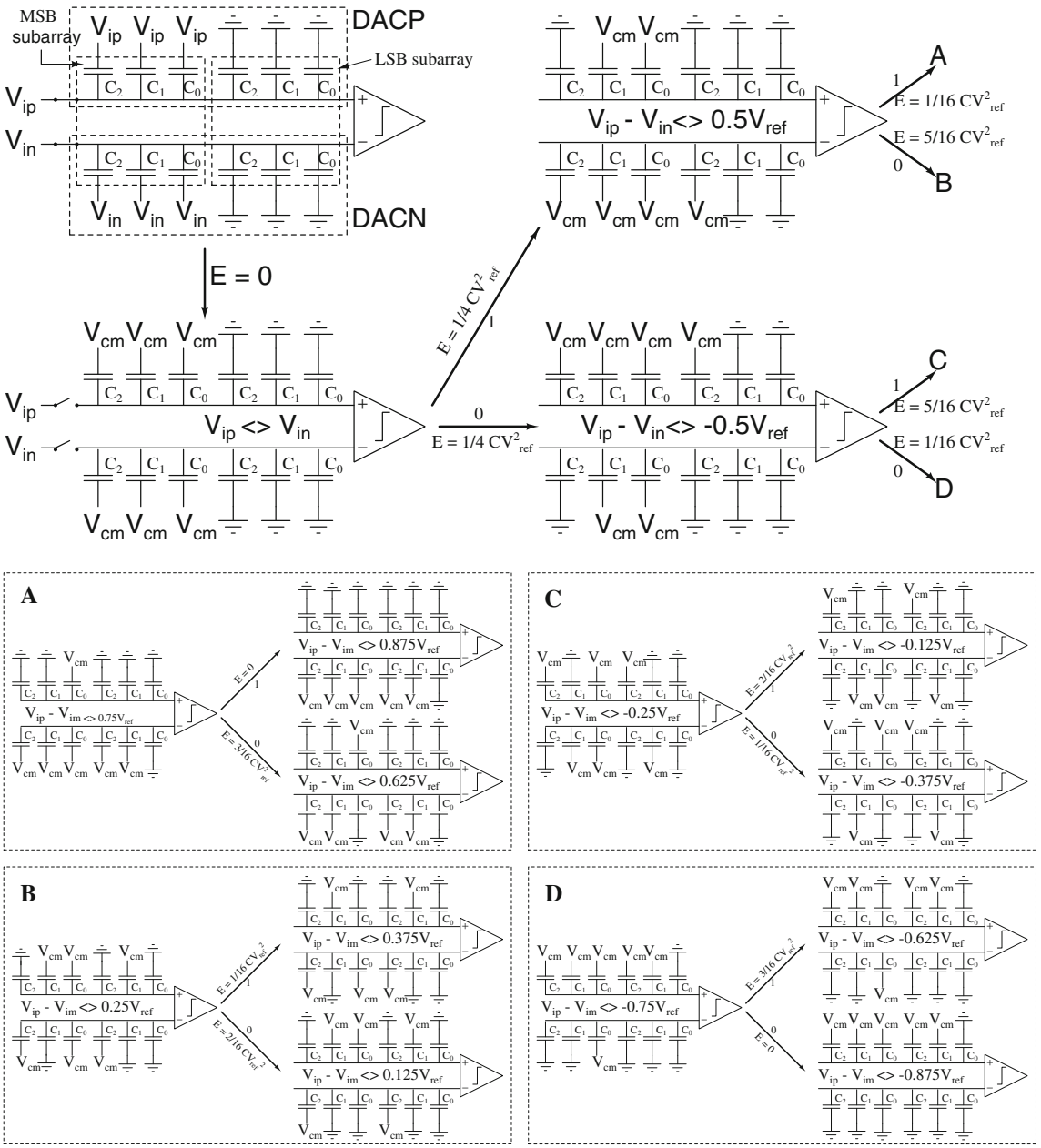

Fig. 3 Proposed switching scheme with 4-bit SAR ADC example

with the help of a 4-bit SAR ADC example. The energy consumed in each cycle depends on the comparator output. The energy consumption in each cycle is estimated analytically and validated using mathematical induction method.

$$E_{k_{\text{th}}\text{cycle}} = \left[2^{N-2} - 2^{N-k-1} - (-1)^{d_{N-k+1}} \cdot x_{k-1} \right] \cdot C \cdot \frac{V_{\text{ref}}^2}{2^{k+1}} \tag{9}$$

$$x_k = (-1)^{d_{N-k+1}} \cdot 2^{N-k-1} + x_{k-1},$$

$$\text{where } k = 2, 3, \ldots (N-1) \text{ and } x_1 = 0. \tag{10}$$

Equation 9 tells us that the energy consumption in each cycle depends on the comparator output in previous cycles. Ultimately, the total energy consumed per conversion depends on the output digital code. The relation between total energy consumption of DAC per conversion and digital output code (D) is obtained as follows:

$$E_{\text{total}} = \sum_{k=1}^{N-1} E_{k_{\text{th}}\text{cycle}}$$

$$= \sum_{k=2}^{N-1} [2^{N-k-3} - 2^{N-2k-2} - (-1)^{d_{N-k+1}} \cdot x_{k-1}] \cdot CV_{\text{ref}}^2,$$

$$\text{where } E_{1_{\text{st}}\text{cycle}} = 0. \tag{11}$$

$$E_{\text{total}} = \left(\frac{2^{N-4}}{3} - \frac{2^{-N}}{3} - \left[\frac{n(n+1)}{2} + 1 \right] \cdot 2^{-N+2} + n \cdot 2^{-1} \right) \cdot CV_{\text{ref}}^2, \tag{12}$$

$$\text{where } n = \left(2^{N-3} - \left\| \left\lfloor \frac{D}{4} \right\rfloor - 2^{N-3} + \left\lfloor \frac{D}{2^{N-1}} \right\rfloor \right\| \right), \tag{13}$$

where $\lfloor \ \rfloor$ is floor function.
$D = 0, 1, 2, \ldots, 2^N - 1$.
N is the resolution of ADC.

Assuming all codes are equiprobable, the average switching energy consumption for N-bit SAR ADC is obtained as

$$E_{\text{avg per\_code}} = \left(\sum_{i=1}^{N-2} (2^i - 1) 2^{N-2i-4} \right) \cdot CV_{\text{ref}}^2 = \left(\frac{2^{N-3}}{3} - \frac{2^{-N}}{3} - 0.25 \right) \cdot CV_{\text{ref}}^2. \tag{14}$$

The capacitive DAC energy consumption is not only restricted to switching energy but also includes reset energy (during the sampling inputs on capacitive DAC) and the energy consumed by parasitic capacitances. The majority of switching schemes presented in state of the art emphasizes on reducing switching energy since the switching energy dominates in early stage. Nowadays, the trend towards reduced switching energy techniques makes the contribution of reset and parasitic energy no more negligible. Here, in the proposed switching scheme, at the end of every conversion, the differential inputs V_{ip}, V_{im} are sampled on only half of the capacitors in DACP and DACN, respectively. Thus, the reset energy is calculated by Eq. 15.

$$E_{\text{reset}} = 2^{N-2} C V_{\text{ip}}^2 + 2^{N-2} C V_{\text{im}}^2 \tag{15}$$

$$E_{\text{reset\_max}} = 2^{N-2} C V_{\text{ref}}^2. \tag{16}$$

Here, the maximum reset energy occurs in two cases: (1) $V_{\text{ip}} = V_{\text{ref}}$, $V_{\text{im}} = 0$, (2)$V_{\text{ip}} = 0$, $V_{\text{im}} = V_{\text{ref}}$. For 10-bit SAR ADC, the reset energy is $256C\left(V_{\text{ip}}^2 + V_{\text{im}}^2\right)$ and the maximum reset energy is $256CV_{\text{ref}}^2$. Next, we look at the energy consumed by parasitic capacitances. There are 2^N unit capacitors in the proposed technique. Assuming that each unit capacitor is fabricated under same conditions, each unit capacitance has same bottom plate parasitic capacitance (C_{p}). In the first cycle of conversion, the bottom plates of both DACs MSB capacitors ($2^{N-2}C$) connected to V_{cm} i.$2^{N-1}C_{\text{p}}$ charged to V_{cm}. Later, in subsequent cycles, depending on the previous decision either DACP or DACN capacitors will be switched to V_{cm}. Thus, the capacitors $2^{N-3}C_{\text{p}}, 2^{N-4}C_{\text{p}}, \ldots C_{\text{p}}$ will be charged to V_{cm} during $N-2$ clock cycles and the total energy consumed by parasitic capacitances is calculated by Eq. 17. For 10-bit SAR ADC, the energy consumed by parasitic capacitance is $192C_{\text{p}}V_{\text{ref}}^2$. The value of parasitic capacitance C_{p} depends on fabrication process and type of capacitor and shielding techniques. With the improved quality of fabrication process and shielding techniques, one can restrict the value of C_{p} to less than 10% of unit capacitance value.

$$E_{\text{parasitic}} = 3 * 2^{N-2} C_{\text{p}} V_{\text{cm}}^2 = 3 * 2^{N-4} C_{\text{p}} V_{\text{ref}}^2. \tag{17}$$

The proposed switching scheme is built on single reference voltage V_{cm} instead of V_{ref} and V_{cm} since the variation mismatch between V_{ref} and V_{cm} causes nonlinearity in DAC. In general, V_{cm} is generated using low-dropout regulator (LDOs) and reference buffers from main supply voltage. The common mode voltage of differential DAC outputs is maintained constant to avoid the comparators input-dependent dynamic offset, which can cause nonlinearity in ADC. Thus, the linearity of ADC is improved compared to existing switching schemes.

3 Modelling using MATLAB

The proposed switching scheme and some of the previously reported switching schemes [7,11,12] have been realized using MATLAB for 10-bit SAR ADC. The switching energy consumed by the DAC for each output code is shown in Fig. 4. It is observed that, using the proposed switching method, the average energy per code consumed by 10-bit SAR ADC is $47CV_{\text{ref}}^2$ only.

Figure 4 shows that the switching schemes presented in [11,12] consume less energy than the proposed one, but they have issues due to variation in common mode voltage at the comparator inputs. This variation not only increases the design complexity of the comparator, but also results in increased power consumption and nonlinearity. The proposed switching scheme maintains constant common mode voltage by differential change in V_{DACP}, V_{DACN} voltages as shown in Fig. 5.

The mismatch between capacitors of DAC causes offset and nonlinearity in ADC transfer characteristics. In general,

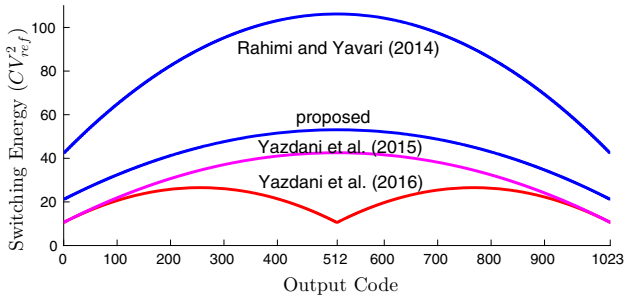

Fig. 4 Switching energy per each code

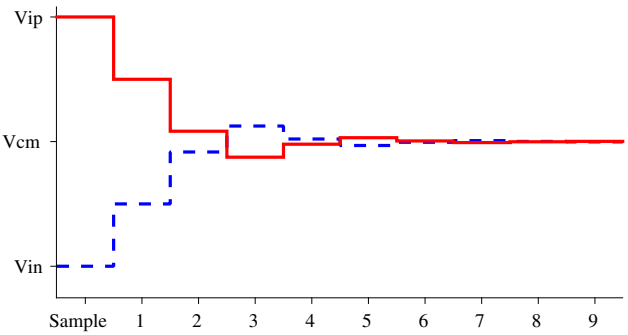

Fig. 5 V_{DACP}, V_{DACN} voltages variation during conversion

ADC nonlinearity is measured in terms of differential nonlinearity (DNL) and integral nonlinearity (INL). Thus, the random variation of step sizes given by differential nonlinearity (DNL) and the correlation between successive step sizes is specified by integral nonlinearity (INL). In the present work, the capacitive DACs are differential and the (comparison) reference levels depend on the precision of both DACs. Here, the complexity of detailed calculation of INL and DNL is high and, hence, the capacitors are modelled using Gaussian distribution with a specified mean and standard deviation in MATLAB. The capacitive DACs are built using those models, and the nonlinearities such as INL and DNL are calculated for each code. To measure the effect of capacitance mismatch for the proposed switching method, a 10-bit SAR ADC is implemented in MATLAB by including mismatch between capacitors. The DNL and INL per code are measured by assuming 1% standard deviation in $\frac{\Delta C_{\mathrm{u}}}{C_{\mathrm{u}}}$ since all fabrication technologies mention less than 1% capacitor mismatch. The DNL and INL per code are plotted for 100 runs as shown in Fig. 6. It can be seen that the conventional ADC has higher values of INL and DNL as compared to the proposed architecture. Table 1 compares the proposed switching scheme with those in [1,2,4–8,11,12].

4 Circuit-Level Implementation of SAR ADC

To validate the proposed switching scheme, a 10-bit SAR ADC is designed using UMC 90nm 1P9M CMOS process technology.

4.1 Capacitive DAC

The unit capacitor, denoted as C_{u} , should be kept as small as possible for energy saving because the DAC energy consumption is proportional to $C_{\mathrm{u}}V_{\mathrm{ref}}^2$. The thermal noise of a simple RC circuit (e.g. a sampling circuit) is given by kT /C, which imposes a lower bound on the minimum required capacitance to achieve a given signal-to-noise ratio. Therefore, the thermal noise is inversely proportional to unit capacitance C_{u}. With respect to matching, a smaller capacitance typically has a smaller area, which results in higher mismatch as given by Pelgroms' inverse-area mismatch model [15]. Thus, the mismatch also imposes another lower bound on unit capacitance. The SNDR degradation for different standard deviations is shown in Fig. 7. One can observe that with ideal capacitors SNDR is close to the ideal 61 dB and as the capacitor mismatch increases

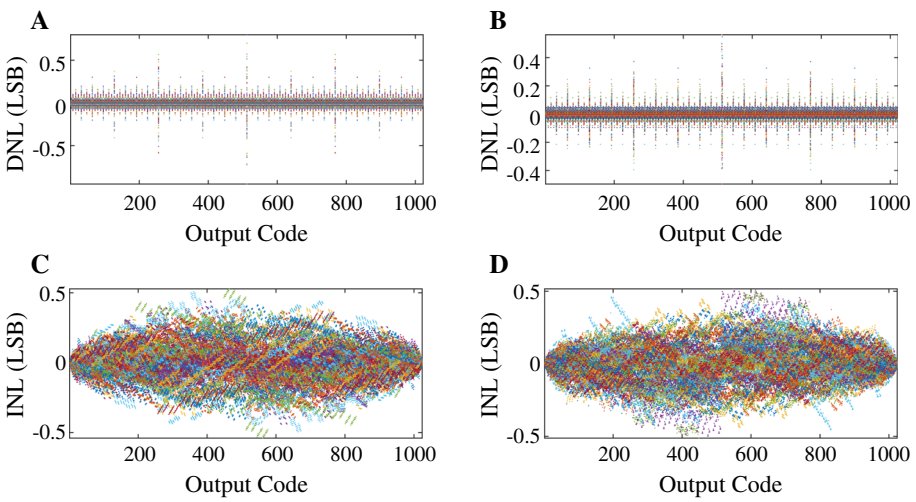

Fig. 6 Statistical distribution of nonlinearity in ADC due to mismatch between capacitors. **a** DNL for Conventional method. **b** DNL for Proposed method. **c** INL for Conventional method. **d** INL for proposed method

Table 1 Comparison of several switching schemes for 10-bit SAR ADC

Switching scheme	Average energy consumption (CV_{ref}^2)	Energy efficiency %	Supply voltages	Sensitivity to V_{cm} variation	Common mode voltage variation	Number of unit capacitors (c)
Conventional [1]	1363.33	Reference	V_{ref}	–	No variation	2048
Capacitor split [2]	852.33	37.48	V_{ref}	–	No variation	2048
Monotonic [4]	255.50	81.26	V_{ref}	–	0 to $\frac{V_{ref}}{2}$	1024
V_{cm} based [5]	170.17	87.54	V_{ref}, V_{cm}	No	No variation	1024
Trilevel [6]	42.41	96.89	V_{ref}, V_{cm}	Yes	$\frac{V_{ref}}{2}$ to V_{ref}	512
New trilevel [7]	84.9	93.7	V_{ref}, V_{cm}	Yes	No variation	512
[13]	15.8	98.8	V_{ref}, V_{cm}	Yes	Varying	512
[14]	15.8	98.8	V_{ref}, V_{cm}	Yes	Varying	512
[8]	42.17	96.91	V_{ref}, V_{cm}	Yes	0 to V_{ref}	512
[11]	31.875	97.66	V_{cm}	No	$\frac{V_{ref}}{2}$ to $\frac{5}{8}V_{ref}$	1024
[12]	21.20	98.44	V_{cm}	No	$\frac{V_{ref}}{4}$ to $\frac{V_{ref}}{2}$	1024
This work	42.417	96.89	V_{cm}	No	No variation	1024

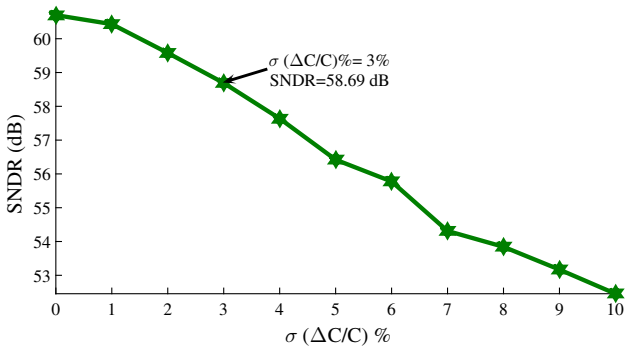

Fig. 7 SNDR versus capacitor mismatch standard deviation

SNDR starts degrading. The plot suggests that a mismatch of 3% is acceptable up to 3 dB SNDR degradation. In UMC 90 nm technology, 140 fF MOM (Metal-Oxide-Metal) capacitor guarantees 1% standard deviation of $\Delta C/C$.

4.2 Comparator

There are numerous architectures reported in the literature for latch-based comparators. Among all, strong ARM latch [10] is quite well known for its high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. It works at two phases, reset phase and regeneration phase. The differential outputs are initially pre-charged (reset) to the supply voltage. During the regeneration phase, the outputs discharge towards ground at unequal speed depending on the input voltages. When these nodes are low enough, one of the cross-coupled inverters is activated and initiates the regeneration. Finally,

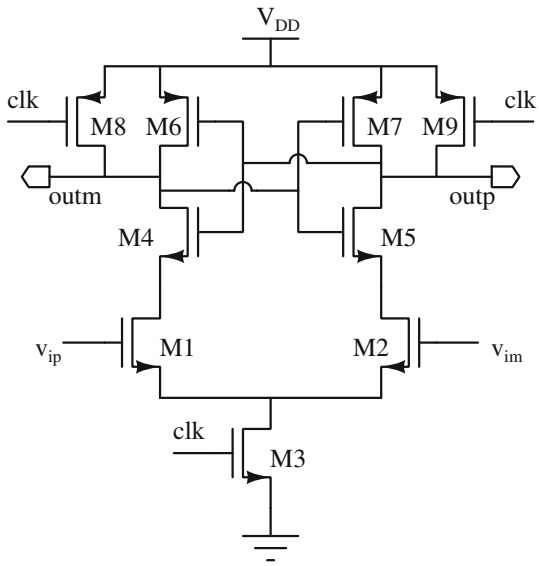

Fig. 8 Strong ARM dynamic comparator

one of the outputs is pulled towards ground, and another one is pulled up to the supply. The circuit diagram of strong arm comparator is shown in Fig. 8. It is optimized, and the transistor dimensions are scaled to get an absolute offset less than 100 μV. Table 2 shows the width (W) and length (L) of each transistor in comparator.

4.3 SAR Logic Controller

The proposed ADC utilizes a synchronous SAR logic; it generates the sample signal and the switch control signals for the

Table 2 Transistor sizes of strong arm comparator

Transistor	W (μm)/L(μm)
M_1, M_2, M_3	0.48/0.08
M_4, M_5	2.4/0.08
M_6, M_7	7.2/0.08
M_8, M_9	0.12/0.08

capacitive DAC. This SAR logic uses total 12 clock cycles for one sample conversion. The first two clock cycles are used for sampling the input on LSB DAC array, and the remaining 10 cycles are used for data conversion, each bit is determined sequentially. The detected bit decides the switch logic for capacitive DAC in next cycle. At the end of 12th cycle, the digital code is stored in parallel in parallel out (PIPO) register and a reset signal is generated with a small delay. The control logic is implemented using only 18 D-FFs.

5 Simulation Results

The SAR ADC is designed and simulated in ADEL using UMC 90 nm CMOS 1P9M process technology with supply voltage of 0.5 V. For testing dynamic characteristics, a sinusoidal signal of frequency 615 Hz and 1 V peak to peak is applied as input to SAR ADC. The sampling frequency is 10 kS/s, and the clock frequency (f_{clk}) is 120 kHz. Here, first two clock cycles are used to sample the input signal onto DAC capacitors. After that, the SAR ADC needs 10 cycles for conversion. At the end of the 12th clock cycle, the data are loaded into parallel in parallel out register and SAR logic controller is reset. Figure 9 shows the spectrum of SAR ADC output signal. It can be seen that the noise floor lies around 100 dB. It includes both noise and harmonics. The total harmonic distortion is 75.5322 dB. The proposed SAR ADC achieves 55.93 dB SNDR, which is equivalent to ENoB of 9 bits. The obtained spurious-free dynamic range for SAR ADC is 77.17 dB. The Walden figure of merit (FoMW) is calculated, and it is 65.1875 fJ/conv.

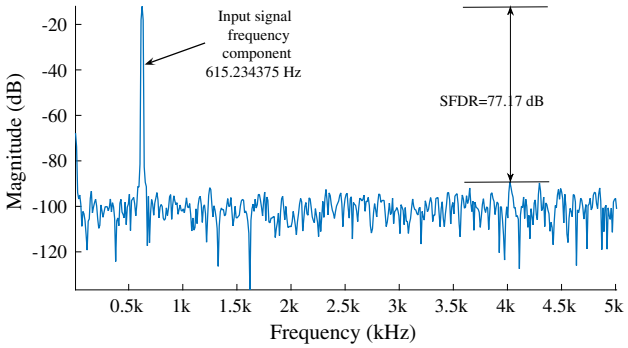

Fig. 9 Spectrum of SAR ADC output signal

Table 4 SAR ADC performance metrics

Performance metrics	Value
Process technology	UMC 90 nm
Resolution	10 bits
Supply voltage	0.5 V
Input signal bandwidth	1 KHz
Sampling frequency (f_s)	10 kS/s
SFDR	77.17 dB
THD	75.5322 dB
SNDR	55.93 dB
Average power consumption	337.66 nW
FoMW	65.1875 fJ/conv

Table 3 Switch logic

Clock cycle	Sample	DACP	DACN	D_{out}
1	1	000000000 11111111	000000000 11111111	–
2	1	000000000 11111111	000000000 11111111	–
3	0	000000000 11111111	000000000 11111111	D_9
4	0	$D_9$00000000 $D_9$1111111	$\overline{D_9}$00000000 $\overline{D_9}$1111111	D_8
5	0	$D_9D_8$0000000 $D_9D_8$111111	$\overline{D_9}$ $\overline{D_8}$0000000 $\overline{D_9}$ $\overline{D_8}$111111	D_7
6	0	$D_9D_8D_7$000000 $D_9D_8D_7$11111	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$000000 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$11111	D_6
7	0	$D_9D_8D_7D_6$00000 $D_9D_8D_7D_6$1111	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$00000 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$1111	D_5
8	0	$D_9D_8D_7D_6D_5$0000 $D_9D_8D_7D_6D_5$111	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$0000 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$111	D_4
9	0	$D_9D_8D_7D_6D_5D_4$000 $D_9D_8D_7D_6D_5D_4$11	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$000 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$11	D_3
10	0	$D_9D_8D_7D_6D_5D_4D_3$00 $D_9D_8D_7D_6D_5D_4D_3$1	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$00 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$1	D_2
11	0	$D_9D_8D_7D_6D_5D_4D_3D_2$0 $D_9D_8D_7D_6D_5D_4D_3D_2$	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$ $\overline{D_2}$0 $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$ $\overline{D_2}$	D_1
12	0	$D_9D_8D_7D_6D_5D_4D_3D_2D_1$ $D_9D_8D_7D_6D_5D_4D_3D_2$	$\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$ $\overline{D_2}$ $\overline{D_1}$ $\overline{D_9}$ $\overline{D_8}$ $\overline{D_7}$ $\overline{D_6}$ $\overline{D_5}$ $\overline{D_4}$ $\overline{D_3}$ $\overline{D_2}$	D_0

6 Conclusion

An energy-efficient, high-precision fully differential MSB capacitor-split switching scheme for feedback DAC in SAR ADC is presented. The proposed switching scheme utilizes single reference voltage V_{cm}(i.e. $0.5V_{ref}$) and improves the switching energy efficiency by 4x as compared to conventional one. The proposed switching scheme is 96.88% energy efficient and 50% capacitor area efficient than conventional switching scheme. Although the energy efficiency is marginally lower than those reported in [11,12], this architecture maintains a constant common mode voltage employing a single supply voltage whereby improving the ADC linearity. All these salient features make this design well suited for realization of low-power and high-resolution ADCs.

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